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Trellis based decoding architecture for non binary LDPC codes using modified Fano algorithm to achieve high throughput

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Abstract **-In this research work, the algorithm is proposed for the LDPC codes and new enhanced Trellis based architecture is implemented for testing the proposed codes. LDPC codes are used to detect and correct the error which occurs during the transmission. These codes are non-binary codes, where modified Fano algorithm is proposed to test the system. In order to increase the throughput, bidirectional recursion is used. Message compression technique is used to reduce the storage requirements and hence the area. The proposed architecture is designed and implemented using Cadence Virtuoso Spectre tool based on 180nm technology. This decoder can achieve a throughput of 38.12 Mb/s at clock frequency of 200MHz**

Index terms **– Fano algorithm, non binary low density parity check codes, Very Large scale Integration**

I INTRODUCTION

Today the communication has entered into our daily lives in many different forms; it is very difficult to lead a life without various appliances which plays a major role in communication. Communication is the process of conveying information through the exchange of thoughts, messages or information as by speech, visuals, signals, writing or behavior. Hence the need for efficient and reliable communication system has been rapidly rising in recent years. Hence several technologies have been developed in order to increase the long range communication and automatic data processing equipment. In recent years the need for efficient and reliable communication system is rising rapidly. So several technologies has been developed to achieve such communication system. The design should have high throughput and provide effective data transmission with minimum error rate. Many channels have been subjected to noise, thus errors may be introduced when it is transferred from sender to the receiver. Hence several error controlling techniques have been introduced in order to detect and correct the error. One such technique is LDPC (Linear Density Parity Check). LDPC codes have the potential for highly parallel decoder implementation, and many high-throughput LDPC decoders were reported. For a channel decoder used in mobile communications, the ability to support various levels of correction capabilities and code rates is a mandatory requirement. When designing an efficient multimode decoder, we must first find the similarity among different modes and then implement the common parts as reusable hardware components. Flexibility can be achieved by controlling the data flow through these reusable components. Since it is difficult to design a flexible architecture such that most hardware resources can be reused in different modes using a fully parallel architecture, a memory based partially parallel architecture is widely adopted in multimode LDPC decoder designs. Trellis modulation scheme is a modulation scheme which allows an efficient transmission of data over a band limited channels. It was first introduced by Gottfried and Ungerboeck.

II RELATED WORK

[1] Magnetic Recording channels (MRC) are subjected to media defects and thermal noise. Binary LDPC codes cannot accommodate the impairment caused in magnetic recording channels (MRC). Hence this problem can be overcome by the use of both binary LDPC codes and Reed Solomon codes on MRC [2] LDPC codes are designed with architecture having embedded structural regularity features. This results in a regular and scalable message transport network with reduced control overhead. However memory overhead problem has been reduced to 75% by using turbo decoding algorithm. [3] An efficient VLSI architecture is proposed for non-binary min-max decoder. Non-binary LDPC codes is an extension of binary LDPC codes which results in a better performance. The codes which is constructed over Galois Field GF (q) is known as non-binary LDPC codes. [4] in order to reduce memory size and complex routing, shifting and symmetry properties are performed. [5] this sorts out the limited number number of variable to check node (v to c) and check node to variable (c to v) message. This reduces the computation complexity and memory required for storing intermediate message. [6] a simplified min-sum decoding algorithm for non-binary LDPC codes is proposed, which shows a small

performance loss over additive white Gaussian Noise (AWGN) channel and independent Rayleigh fading channel.[7] here the codes are constructed based on circulant permutation matrices and multi-fold array dispersion, which perform well over AWGN channel. Berlekamp-Massey algorithm is proposed to avoid burst errors hence it performs well in flat fading channel. [8] message passing algorithm is proposed for non-binary LDPC codes which results in effective trade-off between error performance and decoding complexity. This method is effective for LDPC codes which are constructed based on finite geometrics and finite fields.[9] Non-binary LDPC code results in degraded throughput and long latency. Skimming algorithm is proposed for a low variable processing node. This architecture is implemented over $(2,d_c)$ non binary LDPC decoders. [10] Extended Min-Sum [EMS] decoder is proposed for non-binary LDPC codes. Here in this case the vector message of the decoder is truncated in order to reduce the memory required which further reduces the order of complexity. [11] Shuffled schedule of min – max decoding algorithm is implemented for quasi –cyclic codes, which further hike the throughput with improved check and variable node processing.[12] AA (Architecture Aware)- LDPC (Low density Parity check codes)-Convolutional Code (CC) uses parallelization in both iterations and node dimensions. In order to reduce area MPD is used which requires only a few iterations to achieve good performance. Memory is used instead of register to minimize the cost. The permutation network is used to avoid collision in memory access and difficulty in exchanging information between iterations. [13] variable nodes are divided into groups. FIFO based check node memory is used. With the help of this technique the number of quantization bits and memory size can be reduced without degradation in error performance.

III TRELLIS BASED DECODING ARCHITECTURE USING MODIFIED FANO ALGORITHM

A. Algorithm Description

Algorithm is proposed for trellis based decoding architecture for non binary LDPC (Low density Parity Check Codes).Consider the constraint length of k and code rate r = k/n of discrete memory less channel. The bit metric can be defined as follows

$$\psi_{ij} = log_2 \left(\frac{p\left(\frac{\psi_{ij}}{\delta_{ij}}\right)}{p(\psi_{ij})}\right) - r \qquad (1)$$

Where ψ_{ij} denotes the number of bits received at the output.

δ_{ij} denotes the i_{th} bit of the binary level on j_{th} branch of the tree

The branch metric can be defined as follows

$$\psi_{ij} = \prod_{i=1}^{n} \psi_{ij} \qquad (2)$$

Now the value of ψ_{ij} is substituted from the equation 1. Hence the equation becomes as follows

$$\psi_j = \prod_{i=1}^{n} [\, log_2 \left(\frac{p\,\psi_{ij}/\delta_{ij}}{p(\psi_{ij})}\right) - r] \qquad (3)$$

Consider that the decoder has travelled a path with l branches; hence the Fano path metric can be defined as

$$£(l) = \sum_{j=1}^{l} \psi_j \qquad (4)$$

Substituting the values of ψ_j the equation becomes

$$\prod_{j=1}^{i} \prod_{j=1}^{n} [\, log_2 \left(\frac{p\,\psi_{ij}/\delta_{ij}}{p\,\psi_{ij}}\right) - r] \qquad (5)$$

where l = 1, 2, 3

This equation is modified for writing to (l +1) branches

$$£(l+1) = \prod_{j=1}^{i} \psi_j + \psi_{l+1} \qquad (6)$$

The first term represents the path metric of l branches and second term determines the branch metric of last branches

This can be further reformulated as follows

$$£(l+1) = £(1) + \psi_{l+1} \qquad (7)$$

This can be used during bidirectional recursion, by adding or subtracting the corresponding branch metric

The bidirectional recursion increases the convergence

speed of the system.

Algorithm: Modified Fano Algorithm for non-binary decoding architecture

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Step 1 (initialization)

At initial condition £ = 0 and t=0

It looks for which node to travel

Step 2 (forward recursion)

When £ > t

It moves in the forward direction until it reaches the end of the tree, the path metric satisfies the following condition

$£_F$ (l + 1) >= t1

Step 3 (backward recursion)

When £ < t

It moves in backward direction and look for the end of the node, the path metric satisfies the following condition

$£_R$ (l + 1) < t1

Step 4 (end of the process)

After performing the bidirectional recursion it again come back to initial condition and the above step is repeated.

1V TRELLIS BASED DECODING ARCHITECTURE

In this section the decoding architecture for non binary decoding architecture is presented. The proposed decoding architecture consists of permutation network, message compression and decompression unit, forward and backward memory unit and low pass filter.

A. Permutation network

Permutation network is used to avoid collisions during access from the memory and difficulty in exchanging information between iterations.

B. Adder

The usage of adder in decoding architecture consumes less voltage and provides full voltage swing at a low supply voltage. It has improved power delay product and better noise immunity. The inputs are fed to the adder and then it is given to the permutation network for further processing

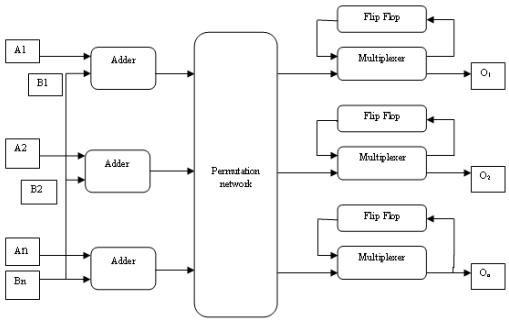

Fig 1 Architecture of NBC permutation network

C. Flip-flop

Flip-flop consume high energy in any circuit, however it is avoided in this decoding architecture by deactivating the clock individually when flip-flops do not have to change their value. Flip – flops are used to store the data. Here it stores the output from the multiplexer and can be retrieved when it is required for further operation.

D. Multiplexer

Multiplexing technique is used to reduce the number of electrical connection in the matrix. Here the driver signals are applied to a group of rows and columns at a time, which switch to a single output.

E. Message compression and decompression unit

Message compression is a technique, which is adopted in decoding architecture in order to reduce the size of data to save space or transmission time. It is performed over the entire transmission unit. When compression is performed over the data, it can remove extra space characters and substitutes smaller bit strings for repeated character. This results in reduction of 50% of its original size.

F. Memory unit

Edge triggered latch is used for storage in decoding architecture, this results in smaller area, less clock loading and power delay product. It stores the data and data can be retrieve during forward and backward recursion.

G. Low pass filter

Low pass filter allows low frequency signals to pass through it, it attenuates the amplitude of the signal which has a frequency higher than cut-off frequencies. Here the frequency achieved is 200MHZ.

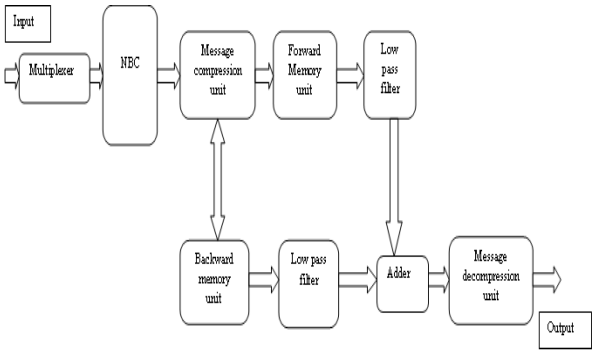

Fig 2 Trellis based decoding architecture

V PERFORMANCE EVALUATION

In this section we show the implementation results for the proposed decoder. This architecture is implemented using cadence virtuoso tool based on 180nm technology.

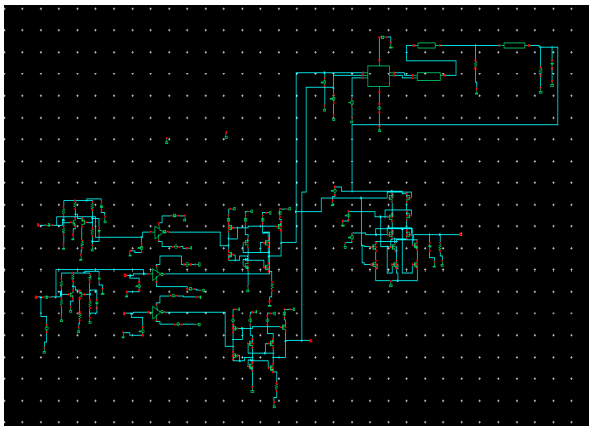

Fig 3 decoding architecture

The figure shows the overall decoding architecture, which is designed using cadence tool in 180nm Technology, which consists of permutation network, message compression and decompression unit, forward and backward memory unit and filter circuits

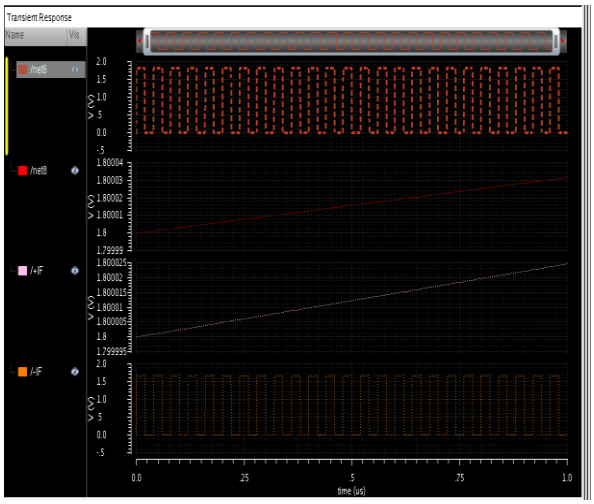

Fig 4 transient response of decoding architecture

The figure shows the transient response of the decoding architecture. It is analyzed to determine the response of system to change from equilibrium state.

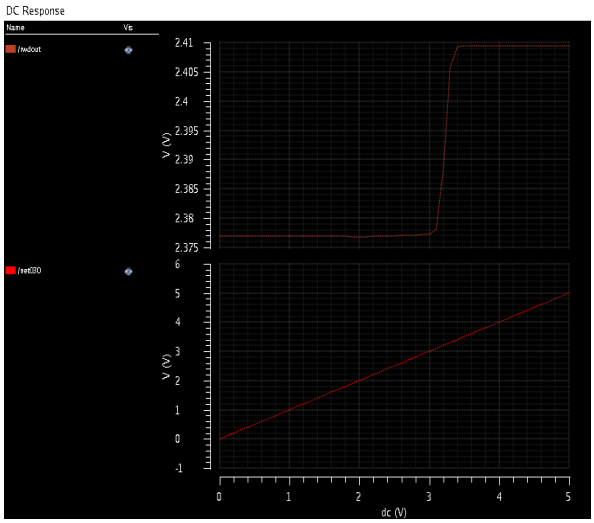

Fig 5 DC response of decoding architecture

The Figure shows the DC response of decoding architecture to determine the operation of the system

The throughput of decoding architecture can be calculated as follows:

$$Throughput = \frac{N*\log_2(q)*f_{clk}}{N_c*N_{it}}$$

Where N_c is the number of clock cycles required to execute one decoding iteration, f_{clk} is the clock frequency and N_{it} is the number of iterations. In our design a throughput of 38.12 Mb/s is achieved.

TABLE 1 COMPARISON TABLE OF DECODING ARCHITECTURE

parameter	**Existing method [1]**	**Existing method [2]**	**Proposed work**
Technology	**90nm**	**90nm**	**180nm**
Algorithm	Trellis based Max product	Selective input Min-max	Trellis Fano algorithm
Frequency	200 MHz	260 MHz	200 MHz
Iterations	3.5	15	2
Total clock cycles	2570	37500	1492
Throughput	32.33	8.84	38.12
Area	40mm^2	N/A	36mm^2

Table 1 shows the comparison chart of various existing decoder with the proposed decoder

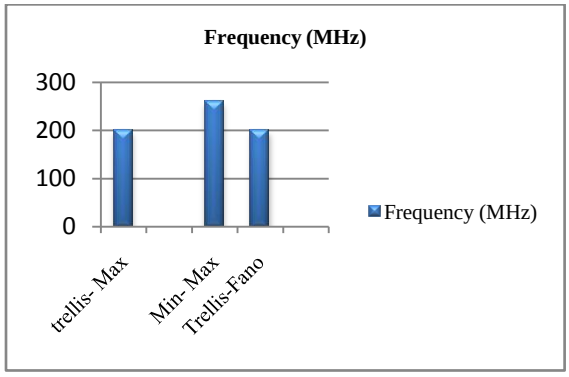

Fig 6 Comparison chart for frequency analysis

Fig 6 shows the comparison chart for frequency analysis. The trellis Fano algorithm has frequency of 200MHz and Trellis based max product has frequency of 200MHz and selective min max algorithm has a frequency of 260 MHz

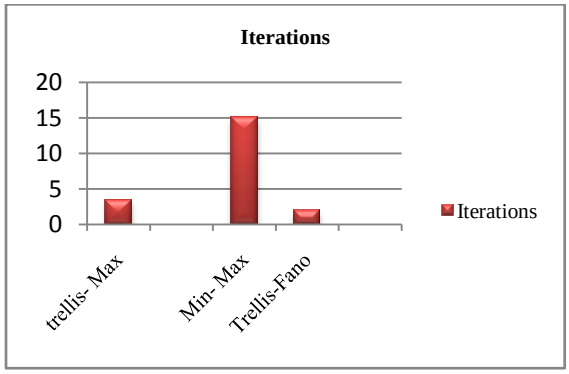

Fig 7 Comparison chart for number of iterations

Fig 7 shows the comparison chart for number of iterations. The trellis Fano algorithm has iteration of 2 and Trellis based max product has iteration of 3.5 and selective min max algorithm has an iteration of 15

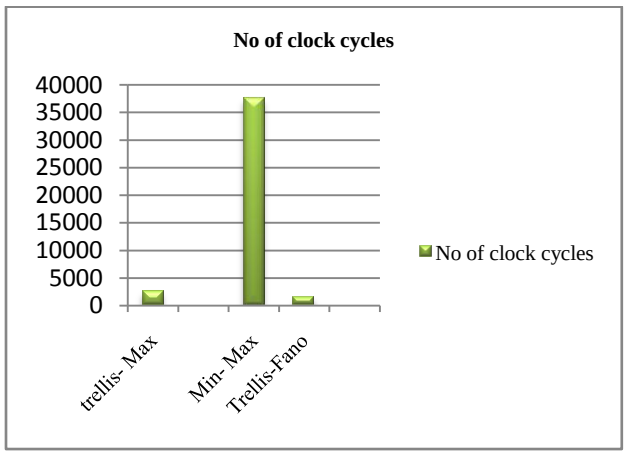

Fig 8 Comparison chart for number of clock cycles

Fig 8 shows the comparison chart for number of clock cycles. The trellis Fano algorithm has clock cycle of 1492 and Trellis based max product has clock cycle of 2570 and selective min max algorithm has a clock cycle of 37500

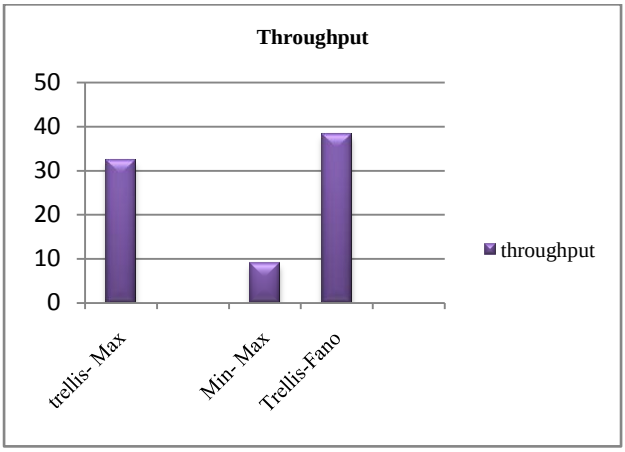

Fig 9 Comparison chart for throughput analysis

Fig 9 shows the comparison chart for throughput analysis. The trellis Fano algorithm has a throughput of 38.12 Mb/s and Trellis based max product has throughput of 32.33 Mb/s and selective min max algorithm has a throughput of 8.84

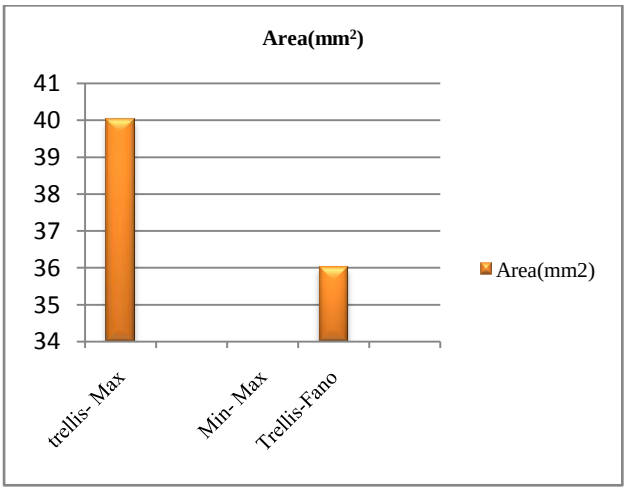

Fig 10 Comparison chart for area

Fig 10 shows the comparison chart for area. The trellis Fano algorithm has an area of 36mm^2 and Trellis based max product has an area of 40mm^2

VI CONCLUSION

In this paper, Fano algorithm is proposed for the LDPC codes and a new enhanced trellis based decoding architecture is designed to test the proposed codes. Bidirectional recursion is adopted to increase the throughput and message compression technique is

performed to reduce the area. The entire design is implemented in Cadence Virtuoso Spectre tool using 180 nm technology

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