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Soft Error Modeling for Low Power Applications

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***Abstract*— As technology is scaling down, circuit reliability issues are major concerns because digital circuits are more susceptible to external noise sources. Soft Error is one such source which changes the voltage of internal nodes of the circuit. Hence it is necessary to design soft error (SE) immune digital circuits. In this paper, we proposed a novel SE immune latch circuit and various sense amplifier Flip Flops. Comparison on parameters of the various sense amplifiers is done. These have been designed on Conditional pre-charging and dual-edge triggering mechanism. These circuits exhibit both low power and transition time, and high speed properties.**

***Index terms* - High performance, low power, Soft error, Transition time**

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I. INTRODUCTION

A. Soft error

Reliability and Yield is the current and future challenges for cutting-edge and leading edge-technologies. Technology scaling along with new materials results in an increase of reliability problems .Soft Error is one of the parameter which reduces reliability of the circuit. It is caused when particles or neutrons traversing through bulk might create minority charge carriers which get collected in drain or source terminal and hence change the terminal voltage. Even though soft-errors cannot cause permanent damage of the circuit but these fault charge collection can change the voltage value of the circuit hence the circuit should be addressed to be soft-error free. This charge collection might result in a transient fault (TF) and consequently when it is latched by a latch or memory cell then it results in Soft Error (SE). The rate at which the device experiences soft error is called soft error rate (SER). Therefore many soft-error immune or tolerant circuits have been proposed, but other design parameters such as area, power and delay are also important. Hence it is important to design low cost SE immune circuit.

B. Effect of regular latch

Figure 1 shows a regular latch, CLK is global clock and D is the data input. When CLK is 1, D to Q is a transparent path. The latch is in transparent mode. When CLK is 0, voltage at node Q is maintained through I3 and the transmission gate. The latch works in latch mode. As explained earlier any high energy neutron or alpha-particles strikes node ln1 then there are high probability that the node develop a voltage and flips its logic. Consequently it will flip the output logic also. This flip is dependent on the critical charge (Qcrit) on node ln1 which is an important parameter in determining soft error. Hence it is a strict requirement to design a circuit which is soft error immune. For low power application, the supply voltage is reduced; therefore, the circuits are more susceptible to SE. And there is no solution purposed before for SE immune latch circuit with low supply voltage

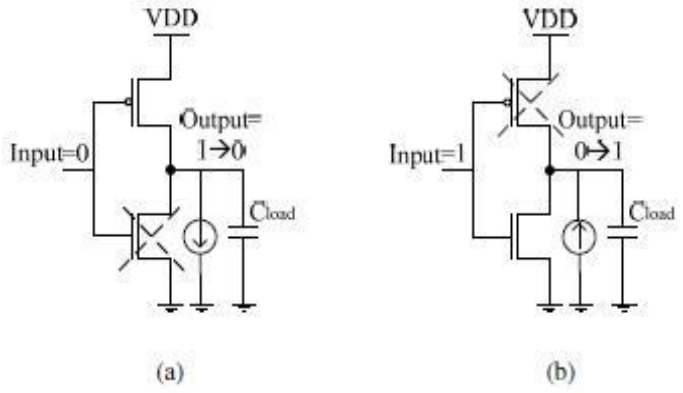


Figure 1. SE modeling [1] of (a) negative and (b) positive glitches.

II. RELATED WORK

In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop .With the recent trend in frequency scaling and deep pipelining, this clocking system power may be even more pronounced. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in both clock distribution networks and flip-flops. Moreover, because of the tight timing budget at high frequency operation, the latency of the flip-flops should be minimized. Hence, the ability to achieve a design that ensures both power consumption and small latency is essential in modern VLSI technology. The dual-edge triggering is an important technique to reduce the power consumption in the clock distribution network. By utilizing dual-edge triggering, the flip-flop is capable of sampling Data on both rising and falling edges of the clock so that only half the clock frequency is needed to obtain the same data

throughput of single edge-triggered flip-flops (SETFFs). Recently, several low-power high-speed DETFF structures have been proposed. In this work, we extensively studied the operation of existing flip-flop architectures, analyzed their weaknesses and proposed new sense-amplifier based flip-flop circuits (hereinafter, referred to as a "SAFF" circuit) due to its differential characteristics, fast operation speed, and low-power consumption. This SAFF circuit is implemented by various approaches within digital circuits such as microprocessors, digital signal processing units, and the like. The first flip-flop achieves substantial power reduction by concurrently incorporating dual-edge triggering and conditional pre-charging. It also minimizes the latency by making use of a fast symmetrical latch. By using our first proposed design as the baseline circuit, we developed a novel clock gating flip-flop circuit to further reduce the power dissipation and at low input switching activity, the second proposed design promises an even greater amount of power savings.

As proposed in hardening of cells can be achieved in two ways, the first category is SEU immune circuits irrespective of the size of the transistors and capacitance of cell nodes an example would be DICE cell. The second category of circuits is achieved by increasing the capacitance of the sensitive node.

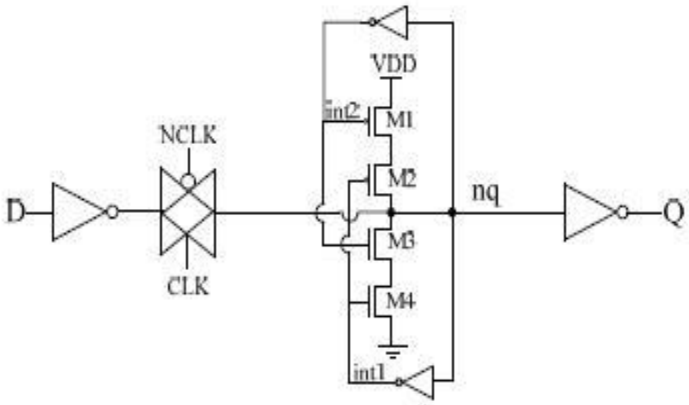


Figure 2. Existing hardened latch [2].

Figure 2 shows a latch with different type of feedback loop. Instead of increasing the critical charge node capacitance it uses an alternative feedback loop which splits the two inverters in the normal functional mode. The feedback loop consists of series of transistor which is biased by different inverters and increases the critical charge on int1 and int2 node. If there is any TF at these two nodes, it will not affect nq node since the series transistors is driven by different inverters. However if SE occurred at node nq, then int1 and int2 will flip at the same time. Therefore, node nq cannot recover to its previous state

Figure 3 shows a Schmitt trigger based hardened latch design proposed in [4]. By implementing this scheme the critical charge at nq is improved due to the hysteresis effect of the Schmitt trigger buffer. However, the Qcrit is increased at the cost of delay due to the Schmitt trigger buffer. In [4], the authors proposed another Schmitt Trigger inverter based hardened latch, which is shown in Fig. 4. When CLK is 1, it is in transparent mode. Suppose ln1 is high then nq is low and t1 is discharged to zero. Hence if any SE occurs on ln1 node, t1 or t2 need to be charged or discharged first, which protect node nq from flipping. However, if SE occurred on nq, then all the internal nodes will flip. Moreover, the speed of the circuit is impacted by the Schmitt trigger inverter due to its hysteresis characteristic.

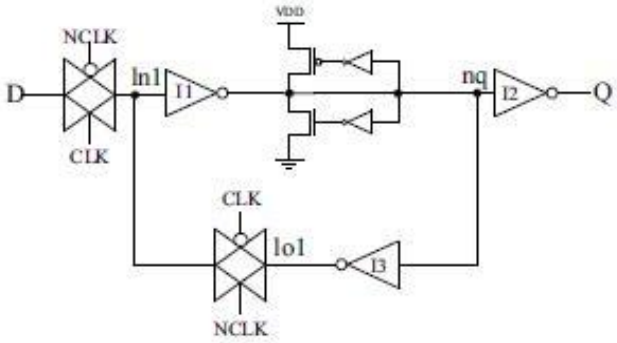


Figure 3. Hardened latch proposed in [4].

III.REVIEW OF THE STATE-OF-THE-ART DUAL-EDGE TRIGGERED FLIP-FLOPS

A.Static Output-Controlled Discharge Flip-Flop

The schematic diagram of the static output-controlled discharge flip-flop (SCDFF) is illustrated in Figure 4. SCDFF involves an explicit pulse generator and a latch that captures the pulse signal. The latch structure of SCDFF consists of two static stages. In the first stage, input D is used to drive the pre-charge transistor so that node X follows D during the sampling period. In addition, the conditional discharging technique is implemented by inserting a QB-controlled n-MOS in the discharge path, which prevents unnecessary discharging at node X as long as the input remains high. The major advantage of SCDFF is low power consumption and soft-edge property. However, a delay is always presented between Q and QB due to the single-ended nature of SCDFF.

B.Dual Edge Triggered Static Pulsed Flip-Flop

The dual-edge triggered static pulsed flip-flop (DSPFF) is shown in Figure 5. In its pulse generator, the four inverters are used to generate the inverted and delayed clock signals. These signals along with two n-MOS pass transistors create a narrow sampling window at both the rising and falling edges of the clock. Once the PULS signal is generated, both pass transistors, N1 and N2, are turned on to capture the inputs data so that either SB or RB will be discharged. A smaller delay can be obtained since DB and D are directly fed to the nodes, SB and RB, respectively. The p-MOS transistors, P1 and P2,

together with two weak n-mos transistors, N3 and N4, effectively avoid the floating of nodes SB and RB when the flip-flop is opaque, thereby providing a fully static operation.

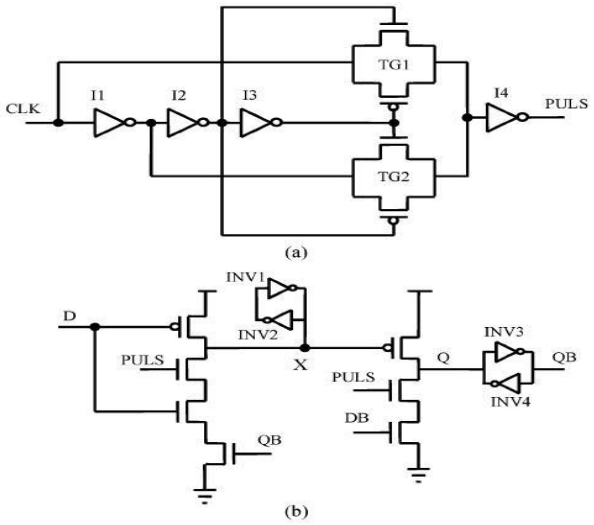


Figure 4. Static output-controlled discharge flip-flop (SCDFF): (a) dual pulse generator and (b) static latch.

The explicit pulse generator is simple and suitable for dual-edge triggering. The static feature of DSPFF eliminates unnecessary transitions. Symmetrical output delays can be obtained by carefully sizing the transistors' aspect ratios. However, the flip-flop latency may be degraded due to the large capacitive loads at the SB and RB nodes. On top of that, DSPFF suffers from high leakage current. This is caused by a high-voltage drop across either transistor N3 or N4, when they are off.

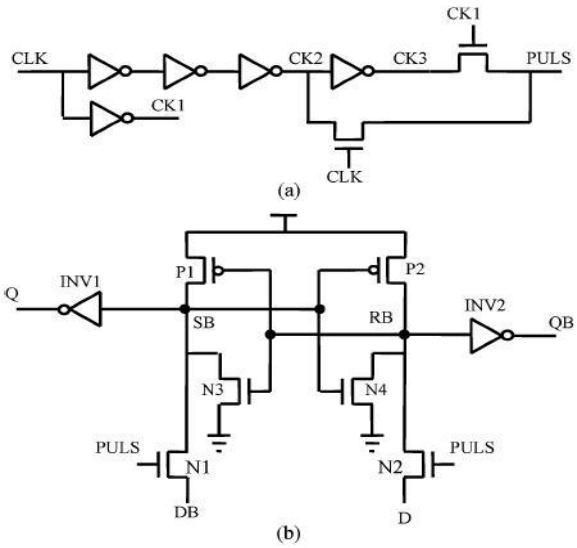


Figure 5 Dual edge-triggered static pulsed flip-flop (DSPFF): (a) dual pulse generator and (b) static latch

C.Adaptive Clocking Dual-Edge Triggered Sense Amplifier Flip-Flop

The schematic diagram of adaptive clocking dual-edge triggered sense amplifier flip-flop (ACSAFF) is presented in Figure 6. ACSAFF is an implicit dual-edge triggered sense amplifier flip-flop. It consists of three stages, i.e., the adaptive clock inverting stage, the front-end sensing stage and the Nikolic's latch stage. The adaptive clock inverter chain is designed to disable some internal clocked transistors when the data switching activity is low. The signal derived from node NC of the sensing stage is used to implement adaptive clocking. If input D is different from output Q, node NC will be pulled up, to turn on transistors N1 and N2. Consequently, the desired inverted and delayed signals, CLK3 and CLK4, will be produced so that a narrow transparent window is created on the rising or falling edges of the clock. Either SB or RB will be discharged during this transparent period, changing the output state in the latching stage. Once the output state is altered, the charging path of NC is blocked and NC will be discharged through either N3 and N4 or N5 and N6, thereby disabling the inverter chain. When D is the same as Q, node NC is low and the flip-flop is opaque. ACSAFF obtains great power reduction at low switching activity. Nevertheless, the adaptive clocking requires more transistors and hence causing the circuit to be more complex. This will lead to greater power consumption at high switching activity and the degradation of the flip-flop speed.

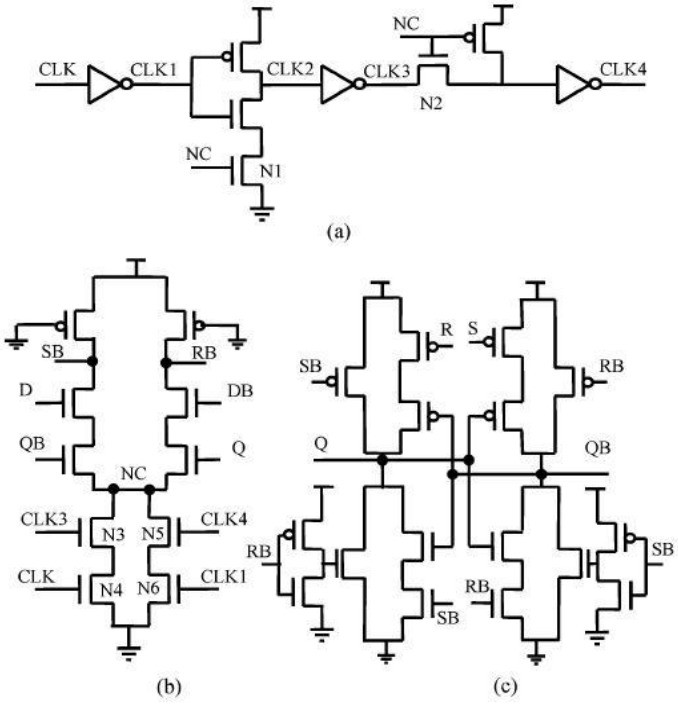


Figure 6. Adaptive clocking dual edge-triggered sense-amplifier flip-flop: (a) adaptive clocking inverter chain; (b) front end sensing stage; and (c) Nikolic's latch.

IV. OBJECTIVES & OVERVIEW OF THE PROPOSED MECHANISM

A. Hardened Latch Circuit

In this section a novel hardened latch design is proposed. CCMOS inverter shown in Figure 7 is based on stacked topology and is enabled by refresh signal. CCMOS inverters are used in feedback loop to bias the pull-up transistors and to avoid any TF that occurs in the loop. If any SE occurs on d1 or d1b, the CCMOS inverters will block the propagation path of the SE. When rf is 1, the CCMOS inverter is enabled and when rf is 0, the CCMOS inverter is disabled. So that any changes in the input or output will not affect the state of the circuit. The proposed latch design is based on two ideas: 1) pull-up and pull-down transistors are biased independently 2) restore the node after TF using a refresh signal. As the former point says to bias the paths independently, the data is applied to pull-up while the pull down path is driven by the drain of pull-up path as shown in Fig. 7. When CLK is 1, the circuit is in transparent mode, D and DB are applied to gates of M1 and M3. D1 is connected to input D through a TG enabled by CLK. Hence d1 takes the value of D during transparent mode. If D is 0, M3 switches on and node QB is pulled up to Vdd, which turns on M2. Q will be pulled down 0. In latch mode d1 is disconnected from D and value at d1 and d1b is kept by the loop which is completed by two CCMOS inverters. Therefore, the value of Q and QB are kept. Assuming SE occurs on d1 during latch mode, as explained earlier CCMOS is enabled by 'rf' signal. If rf=1 the circuit is refreshed and maintained the state. When rf=0 it is in high impedance state. When a TF occurs when rf=0 it is not latched since the circuit is not complete and eventually dies down.

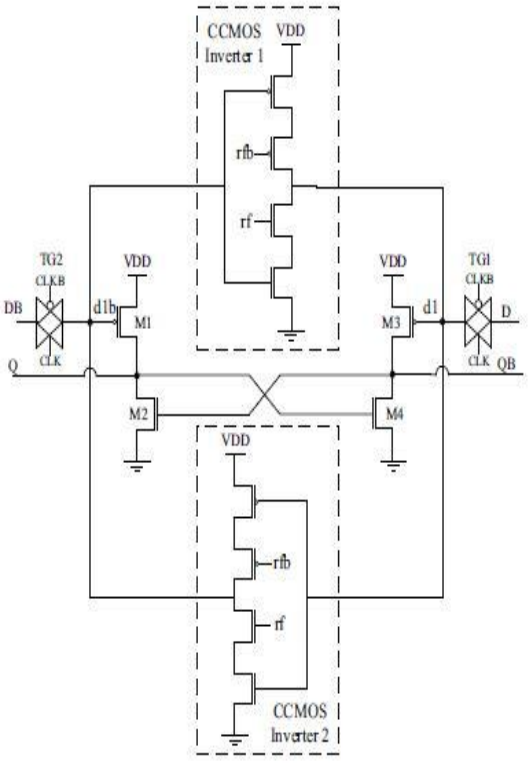


Figure 7.Proposed Hardened Latch Circuit.

B.Dual Edge Triggered Sense Amplifier Circuit

The schematic diagram of the proposed DET-SAFF is given in Figure 8. It consists of three stages: the pulse generating stage, the sensing stage and the latching stage. A simple pulse generator is used. The dual edge triggered pulse generator produces a brief pulse signal synchronized at the rising and falling clock edges. The pulse generator can be shared by multiple flip-flop circuits when a group of flip-flops are located closely. For a sense amplifier based flip-flop, in the evaluation phase as soon as D is low, SB will be set to high, and if D is high, RB will be set to high. Therefore, the conditional pre-charging technique is applied in the sensing stage of DET-SAFF, to avoid redundant transitions at major internal nodes. Two input controlled pMOS transistors, SP1 and SP2, are embedded in the pre-charge paths of nodes SB and RB, respectively.

In this case, if D remains high for n cycles, SB may only be discharged in the first cycle. For the following cycles, SB will be floating when PULS is low or fed to the low state DB when PULS is high.

As for RB, it only needs to be pre-charged in the first cycle and remains at its high state for the remaining cycles. Since the pre-charging activity is conditionally controlled, the critical pull down path of SB and RB is simplified, consisting of only one signal transistor. This helps to reduce the discharging time significantly. As such, the resulting sensing stage possesses low-power and high-speed features.

To further improve the operating speed, a fast symmetric latch is developed. Similar to the Nikolic's latch and Strollo's latch [14], the new latch makes use of SB and RB to pull up the output nodes. But the pull down path is modified. It composes a PULS-controlled n-MOS pass transistor, through which D (DB) is directly fed to the Q (QB) node. This topology significantly speeds up the high-to-low output transition because the output latch immediately captures the input value once the PULS signal is generated. On the other hand, the low-to-high latency will also be improved. This is because the output node will not only be charged by the pull-up transistors, LP1 and LP2, but also the pass transistors, LN1 and LN2. Note that the pass transistors cannot fully charge a node to high, but it can assist with the pull-up transition. The four inner transistors, LP3, LP4, LN3, and LN4, are of minimum sizes, serving the purpose of maintaining the output state when the flip-flop is opaque. For the proposed DETSAFF and previously mentioned dual edge designs, such as the

SCDFF and DSPFF, the power saving techniques are only applicable for the latch part of the flip-flops. As the switching activity of the clock signal is 1, the pulse generator will always be operating even when the input invokes no output changes. These unnecessary transitions cause a lot of power to be wasted, especially at low input switching activities.

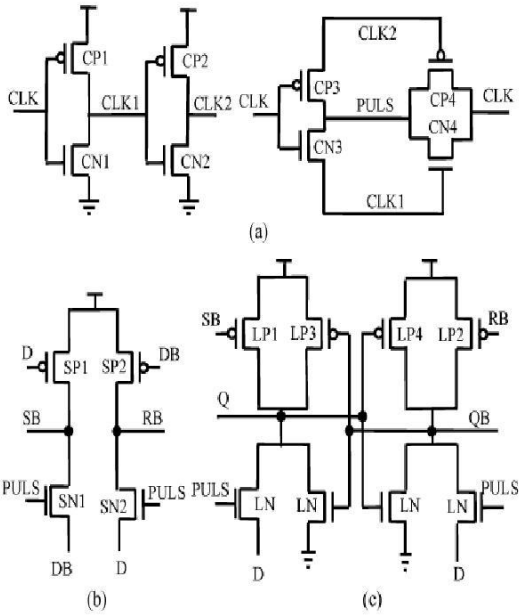
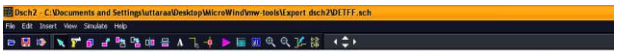
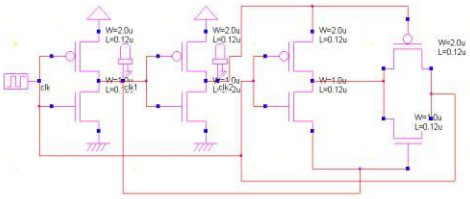


Figure 8 Proposed dual edge-triggered sense-amplifier flip-flop: (a) dual pulse generator; (b) sensing stage; and (c) symmetric latch.

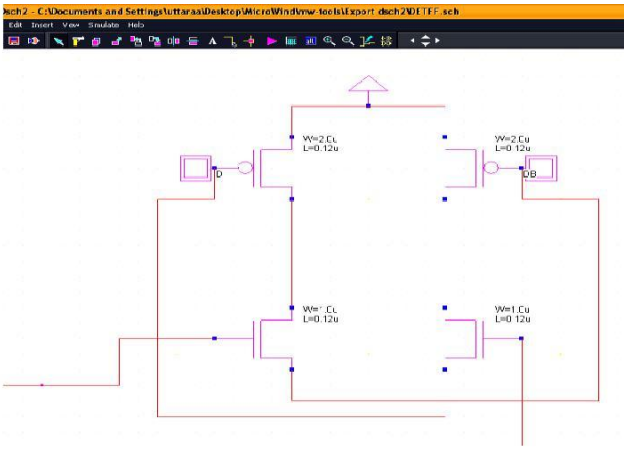
V. PERFORMANCE EVALUATION

A.Dual Pulse Generator Circuit

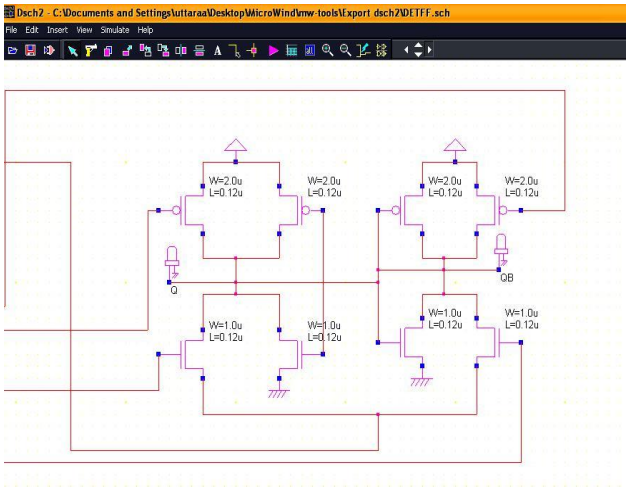




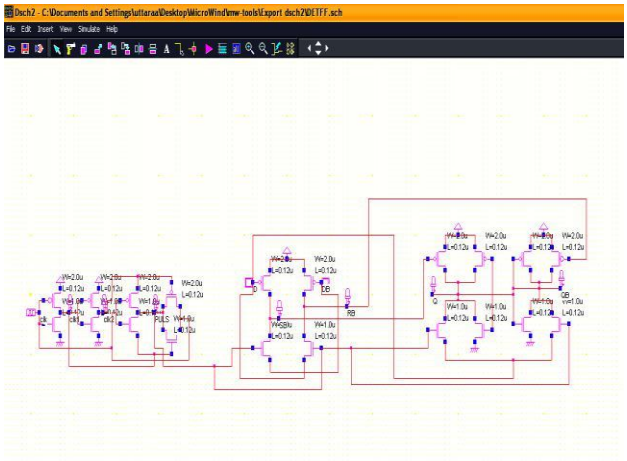
B.Sensing Stage



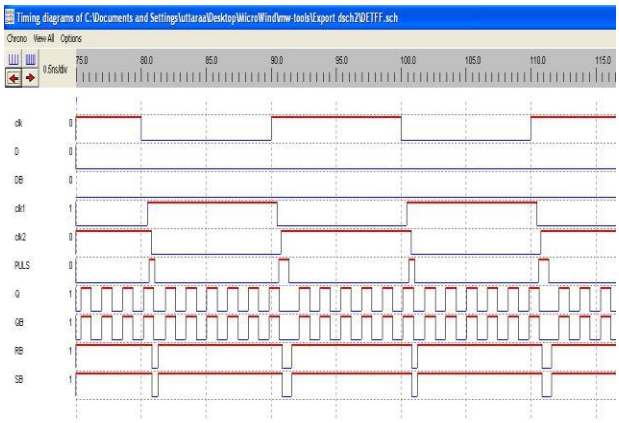
C.Symmetric Latch



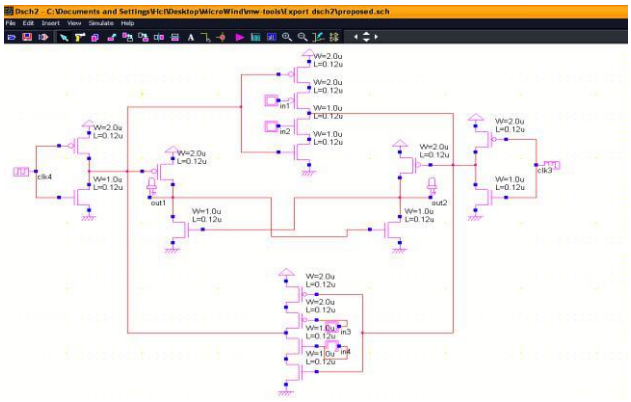
D.DET-SAFF full circuit



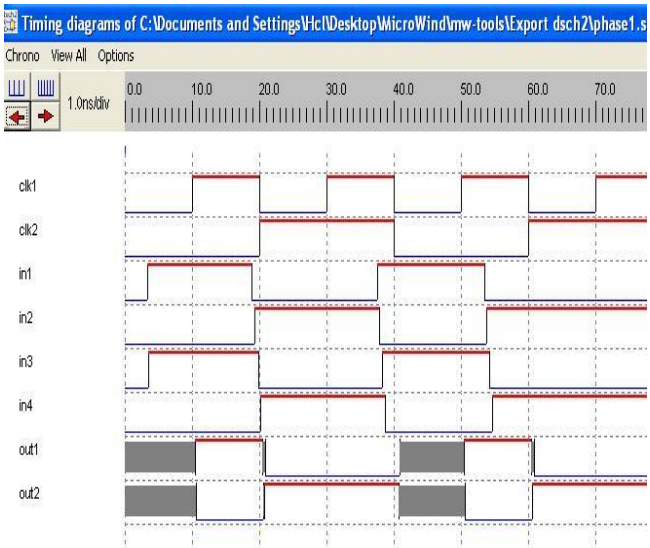
E.Timing Diagram



F.Proposed Schmitt Trigger method for soft error modeling



G.Timing Diagram



REFERENCES

[1]. Baumann.R, "Soft Errors in Advanced Computer Systems". *IEEE Design and Test of Computers* 22(3), 258–266 (2010)

[2]. Mitra.S, Zhang.M, Mak.T.M, Seifert.N, Zia.V, Kim. K.S, "Logic soft errors: a major barrier to robust platform design". *In: Proc. Int. Test Conference*, November 2005, pp. 687–696 (2010)

[3]. Gielen.G, De Wit.P, Maricau.E, Loeckx.J, Martin-Martinez.J, Kaczer.B, Groeseneken.G, Rodriguez.R, Nafria.M, "Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies,"

[4]. Cannon. E.H, Klein Osowski.A, Kanj.R, Reinhardt.D.D, Joshi.R.V, "The Impact of Aging Effects and Manufacturing Variation on SRAM Soft-Error Rate," Device and Materials Reliability, *IEEE Transactions on,* vol.8, no.1, pp.145-152, March 2008.

[5]. Berkeley Predictive Technology model website, http://www.eas.asu.edu/~ptm/.

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