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REDUCTION OF HARMONICS IN SINGLE PHASE CONVERTER WITH PFC

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ABSTRACT: This paper proposes a novel single stage converter based on a quasi-active PFC scheme. In this circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the low frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher frequency. In order to achieve low harmonic content, the input inductor is designed to operate in discontinuous current mode.

Keywords: Fly back converter, PFC cell, PSIM software.

1. INTRODUCTION

Conventional offline power converters with diode – capacitor rectifiers have resulted in distorted input current waveforms with high harmonic contents. To solve these problems, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improve the power factor is a two stage power conversion approach.

The two stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of the scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications.

In order to reduce the cost, the single stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed. These integrated Single stage PFC converters usually use a boost converter to achieve PFC in discontinuous current mode (DCM) operation. Usually the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode

(CCM) operation c voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current. Another technique based on parallel connection of this dither signal, however, the harmonic content can meet the regulatory standard by a small margin.

To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented, in which a high frequency ac voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current.

A new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values.

2. BLOCK DIAGRAM DESCRIPTION

FLYBACK CONVERTER:

Fly-back converter is the most commonly used SMPS circuit for low output power applications where the output voltage needs to be isolated from the input main supply. The output power of fly-back type SMPS circuits may vary from few watts to less than 100 watts. The overall circuit topology of this converter is considerably simpler than other SMPS circuits.

The coupling between the primary and secondary windings will not be ideal. The loss part of the circuit is to be kept in mind while designing for rated power. The designed input power ($\mathbf{P_{in}}$) should be equal to $\mathbf{P_o}/\eta$, where $\mathbf{P_o}$ is the required output power and η is the efficiency of the circuit. A typical figure for η may be taken close to 0.6 for first design iteration. Similarly one needs to counter the effects of the non- ideal coupling between the windings.

Due to the non-ideal coupling between the primary and secondary windings when the primary side switch is turned-off some energy is trapped in the leakage inductance of the winding. The flux associated with the primary winding leakage inductance will not link the secondary winding and hence the energy associated with the leakage flux needs to be dissipated in an external circuit (known as snubber). Unless this energy finds a path, there will be a large voltage spike across the windings which may destroy the circuit.

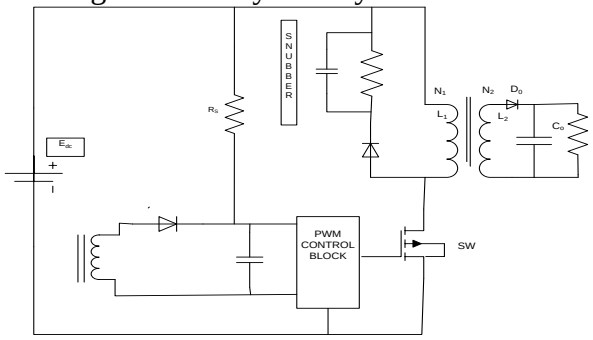


Fig. 2.2 Practical fly back converter

3. CIRCUIT DIAGRAM

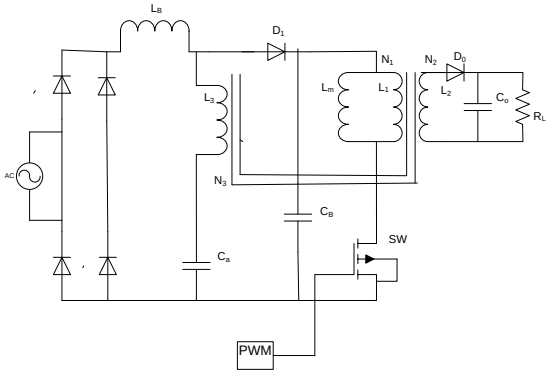


Fig. 3.1 Circuit diagram of Reduction of Harmonics in Single Phase Converter with PFC

3.1 CIRCUIT DESCRIPTION:

The circuit comprised of a bridge rectifier, a boost inductor $L_{B,}$ a bulk capacitor $C_{a,}$ in series with the auxiliary winding $L_{3,}$ an intermediate dc bus voltage capacitor $C_{B,}$ and a discontinuous input current power load, such as fly back converter.

The PFC cell is formed by connecting energy buffer(L_B) and an auxiliary winding (L_3) coupled to the transformer of the dc/dc cell, between the input rectifier and the low frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced.

The input inductor L_B operates in DCM such that a lower THD of the input current can be achieved. The quasi active PFC cell can be considered one power stage but without an active switch.

To simplify the analysis, the following assumptions have been made.

1) All semiconductors components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively.

2) The power transformer does not have the leakage inductances because of the ideal coupling.

3) All the capacitors are high enough so that the voltage across them is considered constant.
4) Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line
frequency.

3.2 PRINCIPLE OF OPERATION

It is assumed that both the input inductor L_B and the magnetizing inductance of the fly back converter operate in DCM. Therefore, currents i_{L_B}, i_m, and $i_2$are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage $V_{C_a}$is greater than the average rectified input voltage $|v_{in}|$. To ensure proper operation of the converter, the transformer's turns ratio should be $(N_1/N_3) \geq 2$ and the boost inductor $L_B < L_m$. In steady-state operation, the topology can be divided into four operating stages.

Stage 1 ($t_o - t_1$):

When the switch (SW) is turned on at $t = t_o$, diodes $D_1$and D_o are OFF, therefore, the dc-bus voltage V_{C_B} is applied to the magnetizing inductor L_m, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_o - t_1) \text{---------- (1)}$$

And since diode $D_1$is OFF, the input inductor $L_B$is charged by input voltage, therefore, the inductor current $i_{L_B}$is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = V_{in} \pm \frac{\left(\frac{N_3}{N_1}\right)V_{CB} - V_{Ca}(to - t_1)}{L_B} \text{--------} \quad (2)$$

where, $V_{in} = V_m |\sin\theta|$ is the rectified input voltage, $(t_o - t_1) = dT_S$ is the ON-time of the switch (SW).

Stage 2 ($t_1 - t_2$):

When the switch is turned OFF at $t = t_1$, output diode $D_o$begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarly, the diode $D_1$is also forward biased and the voltage across L_B now $V_{in} - V_{C_B}$. Therefore, the current $I_{L_B}$is linearly decreased to zero at $t = t_2$(DCM operation), and the energy stored in L_B is delivered to the dc bus capacitor C_B. Therefore

$$i_{LB} = \frac{V_{in} - V_{CB}}{L_B}(t_1 - t_2)$$

The capacitor (C_a) is also discharging its energy to the dc bus capacitor C_B and the current $i_3$reverse its direction. Therefore, the capacitor current is given by

$$i_{D1} = i_{C_B} = i_{L_B} + i_3.$$

At $t = t_3$, the magnetizing inductor releases all its energy to the load and the currents i_m and i_2 reach to zero level.

Stage 3 ($t_2 - t_3$):

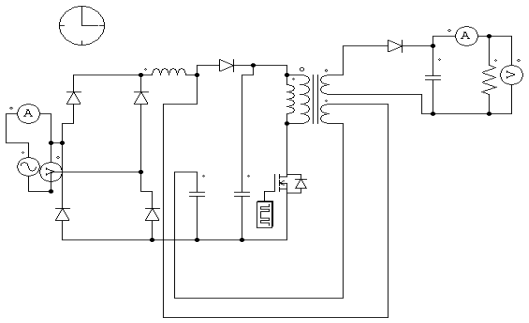
At this stage, the input inductor current i_{L_B}reaches zero and the capacitor C_a continues to discharge its energy to the dc bus capacitor C_B. Therefore, $i_{D1} = i_{C_B} = i_3$. At $t = t_3$, the magnetizing inductor releases all its energy to the load and the currents i_m and i_2 reach to zero level because a DCM operation is assumed.

Stage 4 ($t_3 - t_4$):

This stage starts when the currents i_m and $i_2$reach to zero. Diode D_1still forward biased, therefore, the capacitor C_a still releasing its energy to the dc bus capacitor C_B. This stage ends when the capacitor C_a is completely discharged and current $i_3$reaches zero. At $t = t_5$, the switch is turned on again to repeat the switching cycle.

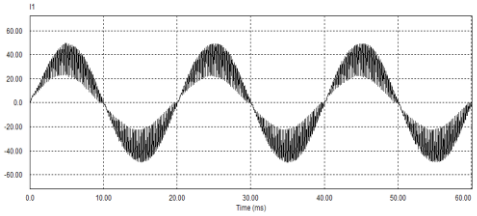
4. SIMULATION CIRCUIT

4.1. Simulation Circuit

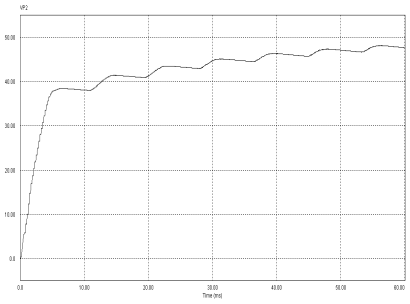


4.2 Simulation waveforms

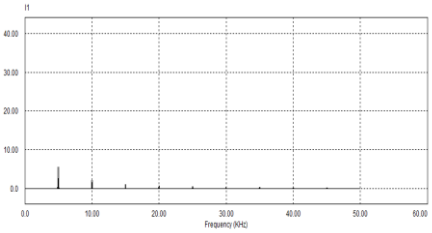
Input current



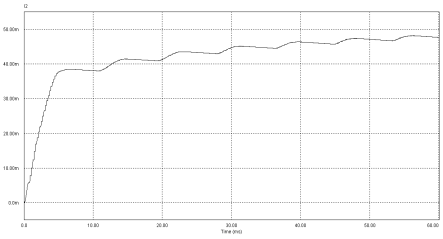
Output voltage



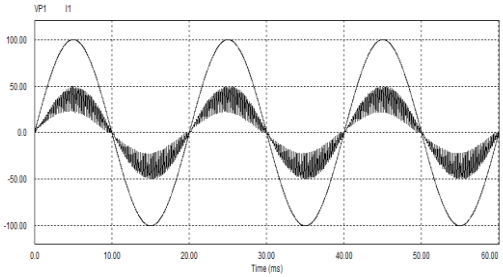
FFT analysis



Output current



PFC waveform



COMPARISON

Description	**Boost+ fly back (DCM+DCM)**	**Proposed converter (DCM+DCM)**
Semiconductors	3 diodes, 1 switch, 1 bridge rectifier	2 diodes, 1 switch, 1 bridge rectifier
Passive components	1 inductor, 2 capacitors, 2-winding transformers	1 inductor, 3 capacitors, 3-winding transformers
Switch current	$I_{LB}+I_{LM}$	$(N_3/N_1)\ I_{LB}+I_{LM}$
Efficiency	70%	>90%
Capacitor voltage	Controlled by the ratio L_M/L_B	Controlled by the ratio L_M/L_B and winding ratio N_3/N_1
THD of the input current	>20%	<10%

5. Hardware Circuit and Output Waveform

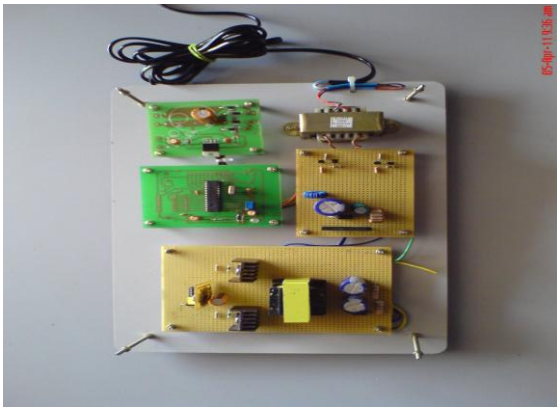
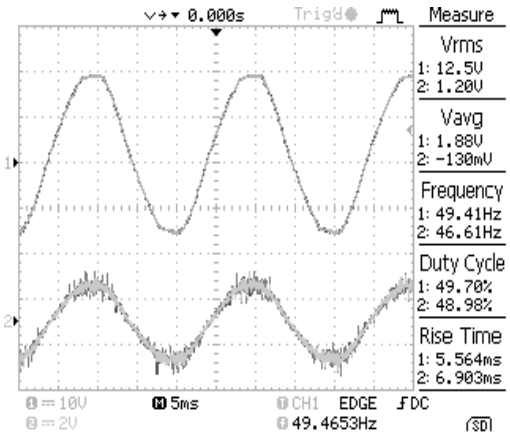


Photo copy of the Hardware



PFC Waveform

7.8 PWM

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load is.

The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switching have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies. The term duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{Fosc}{FPWM}\right)}{\log(2)} \quad \text{bits}$$

Set-up for PWM Operation

The following steps configure the CCP module for PWM operation:

1. Establish the PWM period by writing to the PR2 register.
2. Establish the PWM duty cycle by writing to the DCxB9:DCxB0 bits.
3. Make the CCPx pin an output by clearing the appropriate TRIS bit.
4. Establish the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP module for PWM operation.

5. Conclusion

The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM fly back converter. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible.

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