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Power Gated Pulsed Dual Edge Triggered Flipflop

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***Abstract*— Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption. The performance of the Flip-Flop is an important element to determine the performance of the whole synchronous circuit. In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. High leakage current in deep-submicron regions is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Therefore, identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for battery operated portable low-power applications. This paper targets the power reduction in a conventional flip-flop at the circuit level by introducing power gating with the sleep transistor for the reduction of leakage power. It is proposed that while the flip-flop is in the active mode, the power optimization is achieved through dual edge triggering and when the flip-flop is not in the standby mode, the leakage power is optimized through power gating scheme.**

***Keywords*—** Leakage current, Sleep transistor, Power gating, Dual Edge triggering.

I. INTRODUCTION

High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Therefore, identification and modeling of different leakage components is very important for estimation and reduction of leakage power. This project targets the power reduction in a conventional flip-flop at the circuit level by introducing power gating with the sleep transistor for the reduction of leakage power.

II. DUAL-EDGE TRIGGERED STATIC PULSED FLIP-FLOPS

Myint Wai Phyu discussed that the edge-triggered latches create a narrow sampling window to overcome race problem in comparison to simple latch structures. Therefore this idea was applied to our simple static flip -flop structures. Double-edge triggered flip-flops can latch the data on both rising and falling edge of the clock. Thus, the clock frequency is reduced by half while the data throughput is preserved. Figure13 shows two static pulsed flip-flops structures. They have the same pulse generator circuit as shown in figure9(c).

The pulse generator consists of four inverters which generate delayed and inverted clock signals, *CLK2* and *CLK3*, along with two NMOS transistors for pulse generation. Delayed clock signal *CLK2* which is the inverse of *CLK* is applied to the drain of *MN8* while the clock (*CLK*) controls the gate of *MN8*. When rising edge of the clock signal begins, *CLK2* is high and the pass transistor *MN8* charge the *PULS* node therefore a narrow sample window is generated at the rising edge of the clock signal. Delayed clock signal *CLK3*, *CLK1* and pass transistor *MN9* create another pulse at the falling edge of the clock signal in the same manner. Therefore the pulse signal is generated at both rising and falling edge of the clock as shown in Figure 2

In Figure.1(a) the *PULS* signal applied to the NMOS transistor *MN1* creates a narrow transparency window in which data inputs can affect the state of static nodes *SB* and *S* via NMOS transistors *MN2* and *MN3*. The PMOS transistor *MP5 (MP4)* pulls *S (SB)* node up to *Vdd*. By proper sizing of the NMOS and PMOS transistors of the output inverters and transistors *MN2, MN3, MN4 and MP5*, the proposed flip-flop structure shows equal low to high and high to low output latency, similar to SAFF and CCFF structures.

Figure 1(b) is the another simple structure for dual-edge triggered static pulsed flip-flop. Pass transistors *MN2* and *MN3* contribute in data capturing during the pulse window with *PULS* signal. Since data inputs have direct access to static nodes *SB* and *S* through *MN2* and *MN3*, this structure shows smaller delay than the former one. For distinction of these two dual-edge triggered static pulsed flip-flops the first flip-flop was named as DESPFF and the second one as DSPFF.

In DSPFF two NMOS transistor are controlled by the different delayed pulse and generate a narrow sampling window at both the rising edge of the clock and the falling edge of the clock. After generating the narrow pulse, the two NMOS transistor in the static latch, N1 and N2, are turned on by the pulse in a very short time. At this time, the input data can be captured by the static latch, so notes SB and RB will be charged or discharged which is determined by the input data.

A smaller delay can be obtained because D and DB directly provide the signal to RB and SB respectively. Two PMOS transistors P1 and P2 transfer the Vdd to RB and SB respectively and two NMOS transistors N3 and N4 can connect GND to RB and SB respectively if they are on. So P1, P2, N3 and N4 can effectively avoid the floating of the nodes RB and SB. The size of N3 and N4 should be small in order to make the Clock-to-Q delay to be smaller.

The node that stays at zero voltage (*SB* or *S*) can be floated when the pulse is finished and it could result in short-circuits current on the following inverter or even functional failure. Using two weak NMOS transistors *MN6* and *MN7* the nodes *SB* and *S* will not be floated at anytime. In these structures the generated pulse has a little latency relative to the clock edge.

This provides negative setup time for the proposed flip-flops. The pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation. Figure 15 shows simulated waveforms of DSPFF.

It is obvious that both outputs Q and QB have the same data to output latency. Therefore the proposed dual-edge

triggered static pulsed flip-flops present symmetric output toggling like other high performance flip-flops.

Now, we begin to analyze the disadvantages of the dual-edge triggered static pulsed flip-flop. Because capacitive loads at nodes RB and SB are very large, the flip-flop latency may be degraded. Moreover, because there is a high-voltage drop across either transistor N3 or N4 when they are off, they dual-edge triggered static pulsed flip-flop suffers from high leakage current.

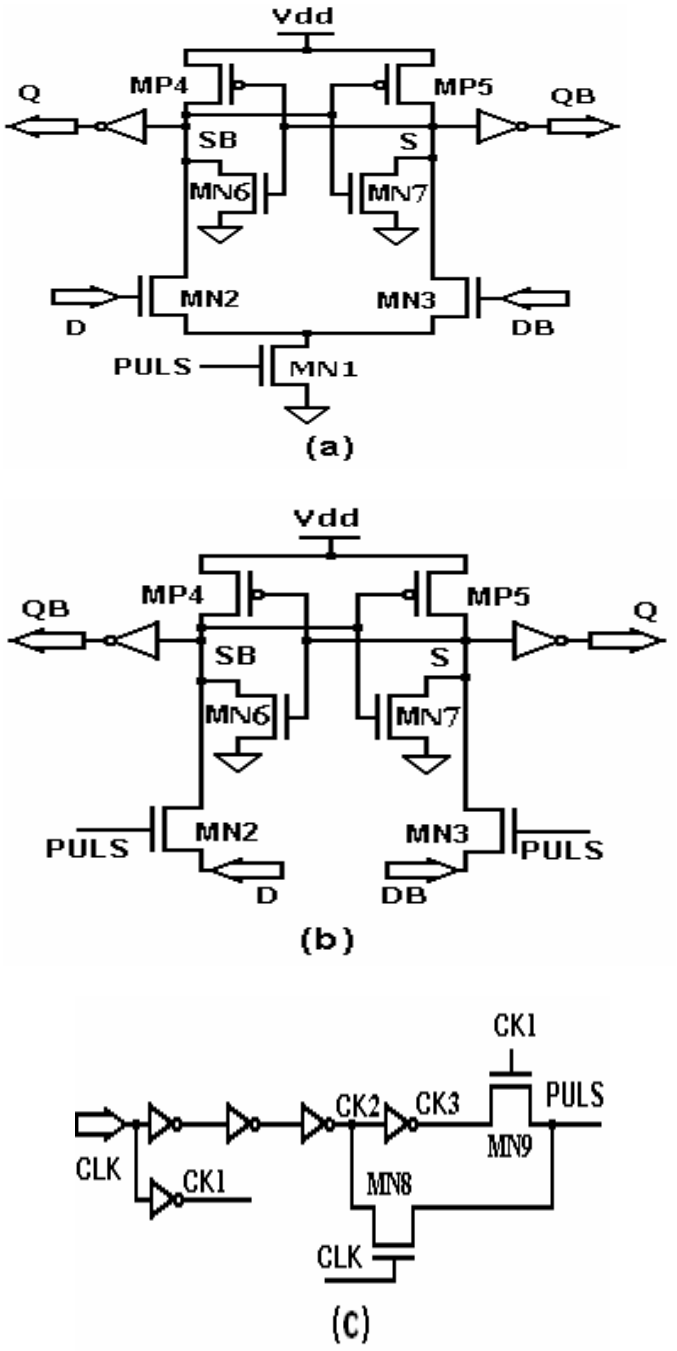

Figure.1. dual-edge triggered static pulsed flip-flop structures (a) DESPFF (b) DSPFF (c) pulse generator.

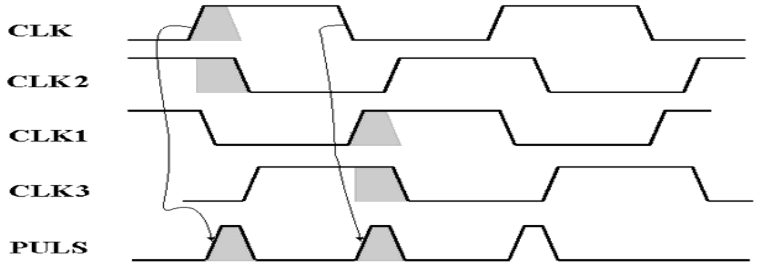

Figure..2. Pulsed clock generation for proposed flip-flops.

. III. COMPARISON OF FLIPFLOPS PERFORMANCE

A dual edge triggered DET flip-flop responds to both edges of the clock. Hence the usage of DET flip-flops reduces clock related power dissipation in digital VLSIs. DET flip-flops are also desirable in high performance applications since Clock frequency can be halved for the same data throughput. In this chapter, we compare several published implementations of DET flip-flops for performance, power consumption.

F.F NAME	Power	Device count
SCDFF	80mw	28
DETFF	400µw	35
Row of PGDETFF for two flipflops	200µw	52

IV. SIMULATION METHODOLOGY AND RESULTS

To evaluate the performance of the DETSPFF [1] flip-flop, The flip-flop was designed using the software Tina 7, at an operating temperature of 27 and a supply voltage of 1.8V, The designs were optimized for a clock frequency Of 1MHZ. A load capacitance of 100 fF was used for all outputs. All the measurements were taken over a 10-cycle data sequence of alternating 1's and 0's.

Simulation result for SCDFF:

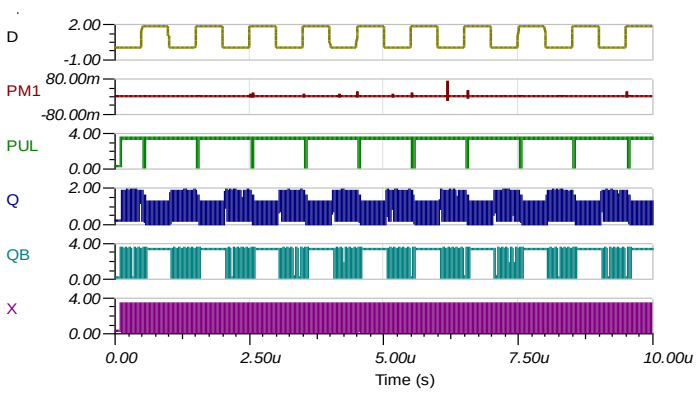

Figure.3 .Simulated waveform and results for SCDFF

Figure.3. represents the simulated waveform for SCDFF in which D is the in put signal with alternating 1's and 0's.Q is the output signal and the pulse is represented by the PULS signal from which the overall power consumption measured is 80mw

Simulation result for DETSPFF:

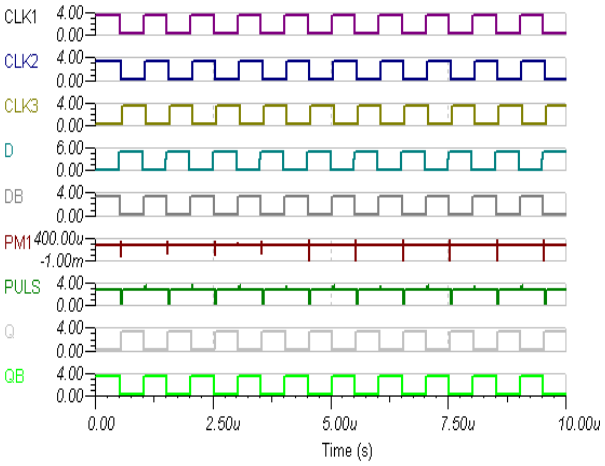

Figure.4.Simulated waveform and results for DETSPFF

Figure.4. represents the simulated waveform for DETSPFF in which D is the in put signal with alternating 1's and 0's.Q is the output signal and the pulse is represented by the PULS signal. Clk1, clk2 and clk3 are the clock, delayed clock and inverted signals respectively from which the overall power consumption measured is -1mw.

Simulation result for PGDETFF:

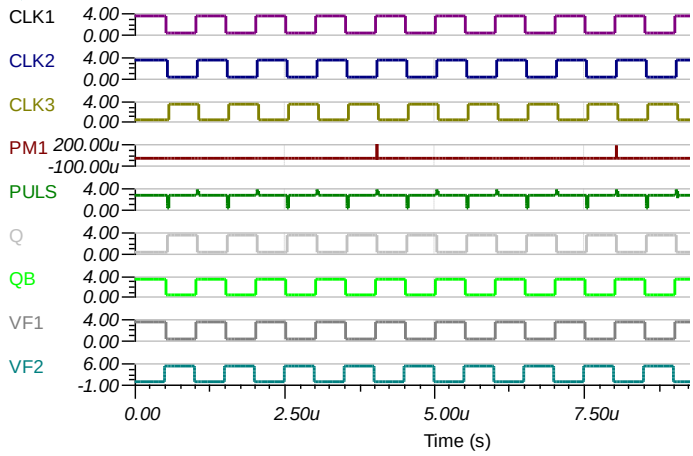

Fig 5. Simulation result for PGDETFF

Figure.5. represents the simulated waveform for PGDETFF in which D is the in put signal with alternating 1's and 0's.Q is the output signal and the pulse is represented by the PULS signal. Clk1, clk2 and clk3 are the clock, delayed clock and inverted signals respectively from which the overall power consumption measured is 200µw.

V. PROPOSED DUAL-EDGE TRIGGERED FLIP-FLOPS

In this section, new dual edge-triggered power gated flip-flops are constructed and discussed. The proposed flip-flop is named the power gated explicit static pulsed dual edge-triggered flip-flop (PGDETFF).

A. Introduction to power gating

The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. However, the performance improvement has been accompanied by an increase in power dissipation; thus, requiring more expensive packaging and cooling technology. Historically, the primary contributor to power dissipation in CMOS circuits has been the charging and discharging of load capacitances, often referred to as the dynamic power dissipation. This component of power dissipation is quadratically proportional to the supply voltage level. Therefore, in the past, chip designers have relied on scaling down the supply voltage to reduce the dynamic power dissipation. Maintaining the transistor switching speeds requires a proportionate downscaling of the transistor threshold voltages in lock step with the supply voltage reduction.However, threshold voltage scaling results in a significant amount of leakage power dissipation due to an exponential increase in the subthreshold leakage current conduction. Borkar in [1] predicts a 7.5-fold increase in the leakage current and a five-fold increase in total energy dissipation for every new microprocessor chip generation.

There are three main sources for leakage current:

1) source/drain junction leakage current;
2) Gate direct tunneling leakage;
3) Subthreshold leakage through the channel of an OFF transistor.

The junction leakage occurs from the source or drain to the substrate through the reverse-biased diodes when a transistor is OFF. The magnitude of the diode's leakage current depends on the area of the drain diffusion and the leakage current density, which, is in turn, determined by the process technology.

The gate direct tunneling leakage flows from the gate thru the "leaky" oxide insulation to the substrate. Its magnitude increases exponentially with the gate oxide thickness and supply voltage.According to the 2001 International Technology Roadmap for Semiconductors, high-K gate dielectric reduced direct tunneling current is required to control this component of the leakage current for low standby power devices. The subthreshold current is the drain-source current of an OFF transistor. This is due to the diffusion current of the minority carriers in the channel for a MOS device operating in the weak inversion mode (i.e., the subthreshold region.)

For instance, in the case of an inverter with a low input voltage, the nMOS is turned OFF and the output voltage is high. Even when VGS is 0V, there is still a current flowing in the channel of the OFF nMOS transistor due to the VDD potential of the VDS.The magnitude of the subthreshold current is a function of the temperature, supply voltage, device size, and the process parameters, out of which, the threshold voltage plays a dominant role. In current CMOS technologies, the subthreshold leakage current is much larger than the other leakage current components.

This current can be calculated by using the following equation:

$$I_{DS} = K\,(1-e^{-Vds/Vt})\; e^{(Vgs-vt+\eta Vds/nvt)}$$

where K and n are functions of the technology, and is the drain-induced barrier lowering coefficient. Clearly, decreasing the threshold voltage increases the leakage current exponentially. In fact decreasing the threshold voltage by 100-mvincreases the leakage current by a factor of 10. Decreasing the length of transistors increases the leakage current as well.

Therefore, in a chip, transistors that have smaller threshold voltage and/or length due to process variation, contribute more to the overall leakage. Although previously the leakage current was important only in systems with long inactive periods (e.g., pagers and networks of sensors), it has become a critical design concern in any system in today's designs.

Unlike the dynamic power, which depends on the average number of switching transistors per clock cycle, the leakage power depends on the number of on-chip transistors, regardless of their average switching activity. The input pattern dependence of the leakage current makes the problem of determining the leakage power dissipated by a circuit a difficult one.

This statement is true even when runtime statistics about the active versus idle times for a circuit are known. This is because by applying the minimum-leakage producing input combination to the circuit when it is in the idle mode, we can significantly reduce the leakage power dissipation of the circuit.

Leakage power is a serious concern in sub-90nm CMOS technology, and several design techniques have been proposed to reduce standby leakage in digital circuits. Power-gating has proven to be a very effective approach to reduce standby leakage, while keeping high speed in the active mode.

It is based on the principle of adding devices, called sleep transistors, in series to the pull-up and/or of the logic gates and turning them off when the circuit is idle, thereby decreasing the leakage component due to I_{ds} sub-threshold currents.

Multithreshold CMOS (MTCMOS) technology provides low leakage and high performance operation by utilizing high speed, low transistors for logic cells and low leakage, and high devices as sleep transistors. Sleep transistors disconnect logic cells from the power supply and/or ground to reduce the leakage in sleep mode.

More precisely, this can be done by using one pMOS transistor and one nMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply as depicted in the left-hand side of Fig. 1. In practice, only one transistor is necessary. Because of the lower on-resistance, nMOS transistors are usually used. In the ACTIVE state, the sleep transistor is on. Therefore, the circuit functions as usual. In the STANDBY state, the transistor is turned off, which disconnects the gate from the ground.

To lower the leakage, the threshold voltage of the sleep transistor must be large. Otherwise, the sleep transistor will have a high leakage current, which will make the power gating less effective. Additional savings may be achieved if the width of the sleep transistor is smaller than the combined width of the transistors in the pull-down network.

In practice, Dual CMOS or MTCMOS is used for power gating [2]. In these technologies there are several types of transistors with different values of V_t. Transistors with a low V_t are used to implement the logic, while high- V_t devices are used as sleep transistors. To guarantee the proper functionality of the circuit, the sleep transistor has to be carefully sized to decrease the voltage drop across it when the sleep transistor is turned on. The voltage drop decreases the effective value of the supply voltage that the logic gate receives.

In addition, it increases the threshold voltage of the pull-down transistors due to the body effect. This phenomenon, in turn, increases the high-to-low transition delay of the circuit. The problem can be solved by using a large sleep transistor.

On the other hand, using a large sleep transistor increases the area overhead and the dynamic power consumed for turning the sleep transistor on and off. Note that because of this dynamic power consumption, it is not possible to save power for very short idle periods.

There is a minimum duration of the idle time below which power saving is impossible. Increasing the size of the sleep transistors increases this minimum duration. Since using one transistor for each logic gate results in a large area and power overhead, one transistor may be used for each group of gates as depicted in the right-hand side of Fig. 6.b

B. Circuit level approach for Proposed PGDETFF

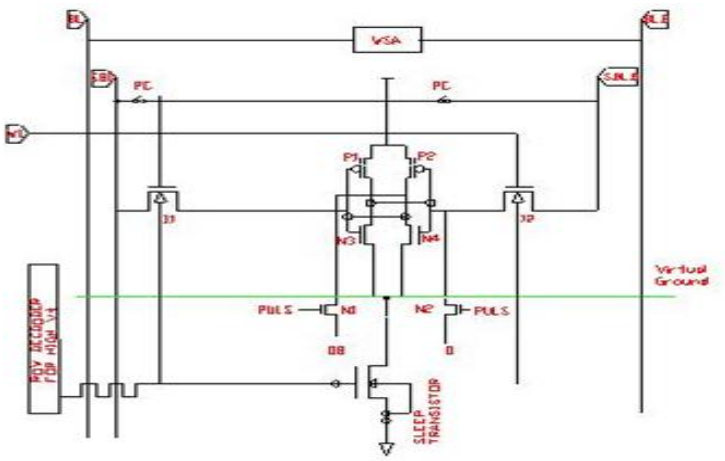

Fig.6. (a).Proposed PGDETFF

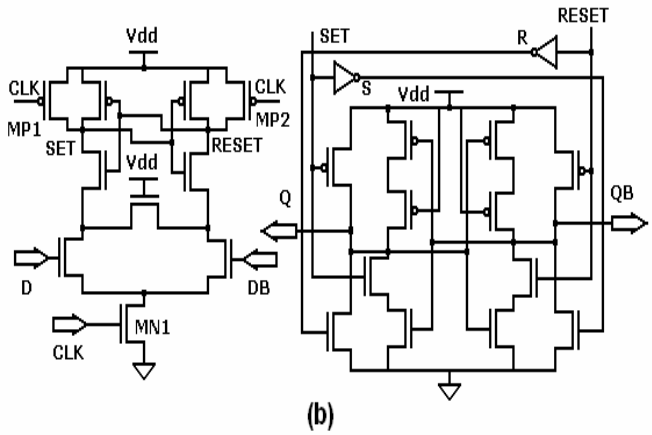

Fig. 6. (b) Conventional high-performance flip-flops:SDFF

Figure.6.a. shows proposed power gated explicit static pulsed dual edge triggered flip-flop [PGDETFF]. The edge-triggered latches create a narrow sampling window to overcome race problem in comparison to simple latch structures. Therefore this idea was applied to our simple static flip -flop structures. Double-edge triggered flip-flops can latch the data on both rising and falling edge of the clock. Thus, the clock frequency is reduced by half while the data throughput is preserved.

The pulse generator in fig 1.c consists of four inverters which generate delayed and inverted clock signals, *CLK2* and *CLK3*, along with two NMOS transistors for pulse generation. Delayed clock signal *CLK2* which is the inverse of *CLK* is applied to the drain of *MN8* while the clock (*CLK*) controls the gate of *MN8*. When rising edge of the clock signal begins, *CLK2* is high and the pass transistor *MN8* charge the *PULS* node therefore a narrow sample window is generated at the rising edge of the clock signal. Delayed clock signal *CLK3, CLK1* and pass transistor *MN9* create another pulse at the falling edge of the clock signal in the same manner. Therefore the pulse signal is generated at both rising and falling edge of the clock.

In Figure 6.a. the *PULS* signal applied to the NMOS transistor *MN1* creates a narrow transparency window in which data inputs can affect the state of static nodes *SB* and *S* via NMOS transistors *MN2* and *MN3*. The PMOS transistor *MP5 (MP4)* pulls *S (SB)* node up to *Vdd*. By proper sizing of the NMOS and PMOS transistors of the output inverters and transistors *MN2, MN3, MN4 and MP5*, the proposed flip-flop structure shows equal low to high and high to low output latency, similar to SAFF and CCFF structures.

The disadvantages of the dual-edge triggered static pulsed flip-flop is the capacitive loads at nodes RB and SB are very large, the flip-flop latency may be degraded. Moreover, because there is a high-voltage drop across either transistor N3 or N4 when they are off, they dual-edge triggered static pulsed flip-flop suffers from high leakage current.

Power gating puts the unused portions of the flip-flop to low leakage mode to reduce power. The key idea is to introduce an extra NMOS transistor Fig.6.a, in the leakage path from the supply voltage to the ground of the DSPFF cells [6.a]; the extra transistor is turned on in the used sections and off in the unused sections, essentially "gating" the supply voltage of the cells.

Gated ground achieves significantly lower leakage because of the two off transistors connected in series, reducing the leakage current by orders of magnitude; this effect is due to the self-reverse biasing of the stacked transistors, which is called the stacking effect, as described earlier.

Similar to conventional gating techniques, the gated-ground transistor can be shared among multiple flip-flops from one or more flip-flop blocks. This amortizes the overhead of the extra transistor. Because the size of the gated-ground transistor plays a major role in the data retention capability and stability of the PGDETFF, and also affects the power and performance savings, the gated-ground transistor must be carefully sized, with respect to the flip-flop transistors.

While the gated-ground transistor must be made large enough to sink the current flowing through the flip-flop in the active mode and to enhance the data retention capability of the flip-flop in the standby mode, a large gated-ground transistor may reduce the stacking effect, thereby diminishing the energy savings.

Moreover, large transistors also increase the area overhead due to gating. In PGDETFF, the gated-ground transistor is shared by a row of flip-flops. The gated-ground transistor is controlled by the row decoder logic of the conventional DETSPFF.

The flip-flops are turned on only when the row is being read from or when data is written into the row. However, this requires the row decoder to drive a larger gate capacitance associated with the gated ground transistor unlike conventional clocking network. To maintain performance, proper sizing of the decoder is required

In active mode the gated circuit operates normally, but it incurs small delay degradation due to the series resistance of the sleep transistor. Thus it reduces the leakage power and increases the performance of dual edge triggered flip-flop in terms of both power and circuit speed.

The proposed PGDETFF has the minimum power consumption when the switching activity is greater than 0.5. At maximum input switching activity, PGDETFF offers 20.3%, 23.2%, 33.5%, and 26% power reductions as compared to SCDFF [10], DSPFF [11], ACSAFF [14], and the proposed PGDETFF. ACSAFF consume more power at high input switching activities due to the addition of the control circuits in the pulse generating paths. However, CGSAFF exhibits its superiority in power saving when the input switching activity is less than 0.5.

With an input switching activity of 0.25, the power consumption of PGDETFF is 20.8%,27.6%, 7%, and 7.6% less than SCDFF, DSPFF, ACSAFF, and the proposed PGDETFF, respectively. The highest reduction of power consumption is achieved when D is idle. And in this case, the power saving is more than 75% as compared to all other reported flip-flops.

C. Analysis of Sleep transistor:

During the active mode, the sleep transistor could be realized as a resistor ***R*** as shown in Figure l(a) **[SI.** This generates a small voltage drop ***VX*** equal to ***I*** x ***R,*** where I is the current flowing through the sleep transistor. The voltage drop across R, reduces the gate's driving capability from *Vdd* to *V d d - 1 5* which in turn degrades the gate's performance.

Therefore, the resistor should be made small and consequently the size of the deep transistor large which comes at the expense of area and power overhead. On the other hand, if the resistor is made large meaning that the sleep transistor is sized small, the circuit speed will degrade. This trade-off between achieving sufficient performance and low power values will become even more severe in the DSM regime.

In DSM technologies, the supply voltage is scaled down aggressively, causing the resistance of the sleep transistor to increase dramatically, requiring even larger size sleep devices. This will cause leakage and dynamic power to significantly mountain in the standby and active modes respectively. Therefore, an important design criterion is sizing the sleep transistor to attain sufficient performance.

To estimate the size of the sleep transistor, the delay of a single gate
(T d) at the absence of a sleep transistor can be expressed as

$$\tau_d = \frac{C_L V_{dd}}{(V_{dd} - V_{tL})^{\alpha}}$$

where *CL* **is** the load capacitance at the gate's output, *KL* is the LVT=350mV, vdd=1.8v and cy is the velocity saturation index which is equal to **1.3** in 0.18pm CMOS technology. In the presence of a sleep transistor, the delay of a single gate be expressed as

$$\tau_d^{sleep} = \frac{C_L V_{dd}}{(V_{dd} - V_x - V_{tL})^{\alpha}}$$

where *VX* is the potential of the virtual ground. Assuming the circuit could tolerate a ***5%*** degradation in performance due to the presence of the sleep transistor, therefore

$$\frac{\tau_d}{\tau_d^{sleep}} = 95\%$$

Substituting for τ_d and **Sleep** a,n d assuming cy = 1 for simplicity,we get

$$1 - \frac{V_X}{(V_{dd} - V_{tL})} = 95\%$$

Therefore *VX* can be formulated as

$$V_X = 0.05(V_{dd} - V_{tL})$$

The current flowing through the "linearly-operating" sleep transistor
is expressed as:

$$I_{sleep} = \mu_n \cos\left(\frac{W}{L}\right)_{sleep} (V_{dd} - V_{tH})V_X - V_{X^2}[2]$$

$$= 0.05\mu_n \cos\left(\frac{W}{L}\right)_{sleep} (V_{dd} - V_{tL})(V_{dd} - V_{tH})$$

where ***pn*** is the N-mobility, ***CO,*** is the oxide capacitance and *V ~ H* is the HVT=SOOmV. The size of the sleep transistor can be therefore expressed as

$$\left(\frac{W}{L}\right)_{sleep} = \frac{I_{sleep}}{0.05\mu_n (V_{dd} - V_{tL})(V_{dd} - V_{tH})}$$

sleep and consequently (*W/L)* chosen to exhibit low power dissipation. *I s l e e p* is chosen to be 250pA, leading to a ***(W/L)=*** 6 for 0.18pm CMOS technology. This constant size (*W / L) s l e e p = 6* will be used for both proposed methodologies i.e Bin-Packing **(BP)** and Set-Partitioning (SP) techniques. Agreeable delay, power and leakage values to analytical calculations were verified for the TINA models, to ensure correct functionality. Leakage current increases by an order of magnitude for every 85mV reduction in *Vth.*

D. Circuit level approach for Proposed Row of PGDETFF

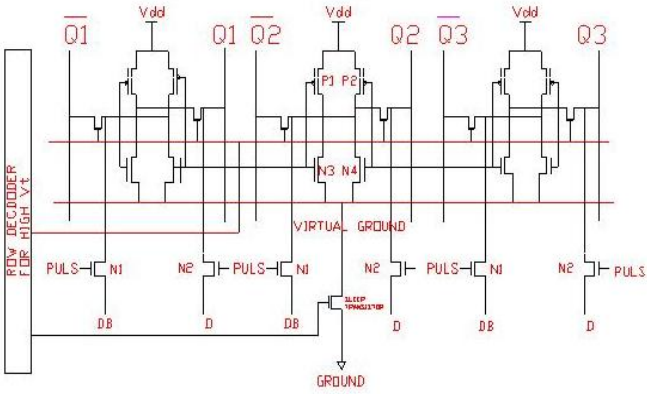

Fig.7.Proposed architecture of the PGDETFF for row of flipflops

Conventional flip-flop stores the data as long as the power supply is on. This is because the cell storage nodes, which are at zero and one, are firmly strapped to the power rails through conducting devices (by a pull down NMOS in one inverter and a pull-up PMOS in the other inverter).

When the gated-ground transistor is ON, the PGDETFF behaves exactly like a conventional DSPFF in terms of data storage. Turning off the gated-ground cuts off the leakage path to the ground. However, it also cuts off the opportunity to firmly strap nodes, which are at zero, to the ground. This makes it easier for a noise source to write a one to that node. Turning on the gated-ground transistor restores the zero data. Simulation results show that data is not lost even if the gated-ground transistor is turned off for indefinite time [2].

Figure 7 is the another simple structure for PGDETFF for row of flipflops.Pass transistors *MN2* and *MN3* contribute in data capturing during the pulse window with *PULS* signal. Since data inputs have direct access to static nodes *SB* and *S* through *MN2* and *MN3*, this structure shows smaller delay than the former one. For distinction of these two dual-edge triggered static pulsed flip-flops the first flip-flop was named as DESPFF and the second one as DSPFF. In DSPFF two NMOS transistor are controlled by the different delayed pulse and generate a narrow sampling window at both the rising edge of the clock and the falling edge of the clock.

After generating the narrow pulse, the two NMOS transistor in the static latch, N1 and N2, are turned on by the pulse in a very short time. At this time, the input data can be captured by the static latch, so notes SB and RB will be charged or discharged which is determined by the input data. A smaller delay can be obtained because D and DB directly provide the signal to RB and SB respectively. Two PMOS transistors P1 and P2 transfer the Vdd to RB and SB respectively and two NMOS transistors N3 and N4 can connect GND to RB and SB respectively if they are on. So P1, P2, N3 and N4 can effectively avoid the floating of the nodes RB and SB.

The size of N3 and N4 should be small in order to make the Clock-to-Q delay to be smaller. The node that stays

at zero voltage (*SB* or *S*) can be floated when the pulse is finished and it could result in short-circuits current on the following inverter or even functional failure. Using two weak NMOS transistors *MN6* and *MN7* the nodes *SB* and *S* will not be floated at anytime. In these structures the generated pulse has a little latency relative to the clock edge. This provides negative setup time for the proposed flip-flops. The pulse generator can be shared among a group of flip-flops to reduce the power and area overhead of pulse generation.. It is obvious that both outputs Q and QB have the same data to output latency. Therefore the proposed dual-edge triggered static pulsed flip-flops present symmetric output toggling like other high performance flip-flops.

The worst case design scenario takes place if all the gates supported by the sleep transistor are simultaneously switching in time .The sleep transistor exhibits maximum current. The sleep transistor is thus sized up to contain the high current. If the gates are discharging mutually exclusive,the sleep transistor is sized according to the maximum current of the mutually exclusive discharging gates *(I* = max(Il,I2, *13))*

The sleep transistor is a lot smaller in this case. If a current-time graph is constructed of the discharged currents, I1**,** 12 and I3 would overlap in time in Case I. On the other hand, no overlap in time occurs for Case 11**.** An intermediate case occurs when the discharged currents "partially" overlap, if the LVT have slightly different discharge times. A single sleep transistor to support the whole circuit was proposed in [C**].** In another work **[**D**],** the sleep transistor was sized according to an algorithm based on mutual exclusive discharge pattem. In [D], cascaded gates are clustered together because simultaneous current discharge can never take place.

This methodology may be efficient for balanced circuits with tree configurations, where mutually exclusive discharging gates are easily detected. However, this methodology would not be efficient for circuits with complicated interconnections and unbalanced structures. Sleep transistor assignments can therefore be wasteful, and would cause dynamic and leakage power to rise.

Finally, the sets of sleep transistors in [D] are merged into a single large sleep transistor to accommodate the whole circuit as in [C]**.** In addition to the drawbacks listed above, sharing a single sleep transistor for the whole circuit would increase the interconnect resistance for distant blocks. As a result, the sleep transistor would be sized even larger than expected to compensate for the added interconnect resistance. Excessively large sleep transistors again augment dynamic and leakage power as well as area.

This drawback would be even more severe in DSM regimes, where interconnects would have a large impact on the circuit's performance . Our proposed methodology in fig solves this problem, and not only clusters gates with exclusive discharge patterns, but with "partially" overlapping discharged currents as well.

VI. CONCLUSION

With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. In this work architectural level approach for the low-power flip-flop using the power gating and Charge-Recycling (for row of flip-flops) while maintaining the performance is proposed for the reduction of leakage power. The Dual edge triggering reduces the on state power by reducing the clock frequency and power gating Scheme reduces the power when the flip-flop is not in use. Simulation result for the DESPFF, CGDETFF, PGDETFF and Modified version of PGDETFF is discussed. From which the PGDETFF achieves substantial active power and standby power reduction by incorporating dual-edge triggering and power gating. PGDETFF is superior in power saving at low switching activities. As compared to DETSPFF, which also has a power saving pulse generator, PGDETFF performs in terms of power consumption (maximum of 75%), latency (27%), setup time (50%) and operation stability. Furthermore, a modified version of the PGDETFF is introduced, which significantly improves Performance for row of flip-flops. Both versions of the proposed PGDETFFs have conclusively proved their robustness and suitability of applications when low power and high speed are of equal importance. In future it is extended for the design of low power SRAM and processor.

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