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Performance Analysis of Dadda Multiplier using 5:2 Compressor and its Applications

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Abstract- **Data compression has a major role in multimedia and image processing applications to encode the information in a compact size. In those applications, reducing area,power and delay are the most important requirements. In this paper two new 5:2 exact compressor are designed to analyze the dadda multiplier based on area, power consumption, delay with error distance.Then the proposed dadda multiplier is utilized to multiply two images pixel by pixel approach with high PSNR value. The simulation results are carried out by Modelsim software and the image multiplication part is done by MATLAB software. The results proved that the dadda multiplier with 5:2 exact compressor achieves better accuracy improvement along with less area, power consumption and less error distance with considerable delay than an 4:2 exact and approximate compressor.**

Index terms –Dadda multiplier, Exact compressor, Approximate compressor, Error Distance.

I. INTRODUCTION

The DSP blocks are an important basis of many multimedia applications. It implements image and video processing algorithms and the output of these algorithms to be numerically approximate rather than accurate for human visibility. This relaxation on numerical accuracy provides some freedom to carry out imprecise or approximate computation. It is used to provide low-power designs with less area and delay at different levels of design abstraction. Multiplication is an important arithmetic operation in digital signal processing. Parallel multipliers provide multiplication with high-speed, but it requires a high area for VLSI implementations. Truncated multiplication multiplies the two numbers by summing only the most significant columns of the multiplication matrix, along with a correction constant [4].This goal is to reduce the area consumption of rounded output multipliers. Low-power is an essential requirement for portable multimedia devices using various signal processing algorithms and architectures. The imprecise or approximate Full Adder (FA) is used to design, approximate multi-bit adder cells with reduced circuit complexity at the transistor level [1]. But, this process is inefficient, since it produces 17 incorrect results out of 32 states. Error Distance (ED) is described as the difference between the actual output and an error output for a given input [2]. The Mean Error Distance (MED) is used for measuring the implementation accuracy of a multiple-bit adder and Normalized Error Distance (NED) is useful in illustrating the reliability of the design. An inaccurate 2 × 2multiplier architecture with tunable error characteristic is proposed in[5]. This multiplier provides average power consumption for an average error than an accurate multiplier. By introducing an error in the sample application, image filtering and JPEG compression is used to offer better Signal-Noise-Ratio (SNR) in multiplier architecture than voltage scaling method. Low-power CMOS logic 4-2 compressor is implemented using a combination of XOR-XNOR gates for high-speed multiplication is described in [8]. In the VLSI implementation for reducing the truncation error with less area and delay, two's complement fixed-width booth multiplier is designed in [10]. An average error reduction is achieved by adding few logic gates to the multiplier. This paper is organized as follows: Chapter 2 explains the implementation of 4:2 exact and approximate compressor with dadda multiplier. Chapter 3 presents the proposed 5:2 exact compressor with dadda multiplier. In Chapter 4 results and discussions are clearly manifested. Chapter 5 illustrates the application part. Finally, Chapter 6 concludes the paper.

II. DESIGN OF 4:2 EXACT AND APPROXIMATE COMPRESSOR

A. Exact 4:2 compressor

Basically the compressor is widely used to speed up the process and reduce the partial product stages during the multiplication. The main goal of exact compressor is to provide an accurate output with higher power consumption, delay and high area requirement. The general block diagram for 4:2 exact compressor is shown in Fig 1.Here X1, X2, X3, X4 are four inputs and sum, carry are the output of the compressor. Carry input (C_{in}) and Carry output (C_{out}) are the carry bit which is coming from the previous compressor and the next compressor respectively.

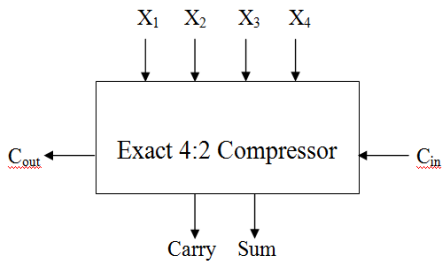


Figure 1. Block diagram for Exact 4:2 compressor

In this compressor, four inputs and sum bit have the same weight and carry output has one binary bit with higher significance. Whenever the 4:2 compressor receives an input (C_{in}) from the previous compressor with one binary bit in lower significance then it produces the output (C_{out}) to the next compressor with higher significance. In the existing system, 4:2 exact compressor is designed by two different implementations,

i) Exact compressor design using Full Adder

ii) Exact compressor design using XOR-XNOR module with a multiplexer

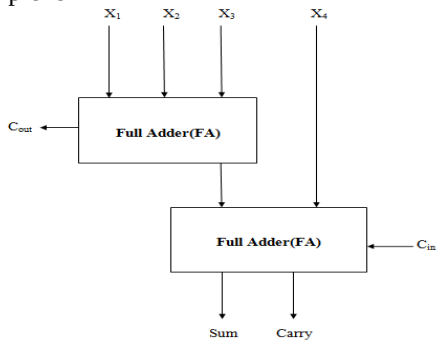


Figure 2. Implementation of 4:2 compressor by FA

The exact compressor is commonly implemented by series connection of two Full Adder (FA) blocks. It calculates a sum value with same order to the next stage and carry has one order higher in the next stage. The implementation of exact compressor with FA is shown in Fig 2. The outputs of exact compressor design using Full Adder are obtained by the following equations,

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X4 \quad (1)$$

$$C_{out} = (X_1 \oplus X_2)\, X_3 + (\overline{X1 \oplus X2})\, X_1 \quad (2)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X4)C_{in} + (\overline{X1 \oplus X2 \oplus X3 \oplus X4})\, X4 \quad (3)$$

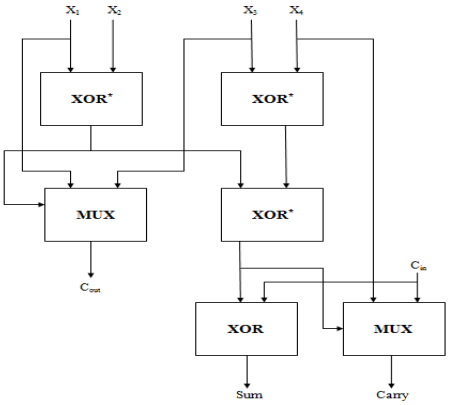


Figure 3. Implementation of 4:2 compressor by XOR with MUX

The XOR-XNOR module is denoted by XOR*, it produces XOR and XNOR signals simultaneously. From the XOR* output, the multiplexer selects input based on the selection line or enable as an output. The output is calculated by,

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X4 \quad (4)$$

$$C_{out} = (X_1 \oplus X_2)\, C_{in} + X_1.X_2 \quad (5)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X4)C_{in} + (X_1 \oplus X_2 \oplus X_3)X4 \quad (6)$$

The truth table of the exact compressor with two different implementations are shown in Table 1.

Table 1: Truth table of the exact 4:2 compressor

C_{in}	X_4	X_3	X_2	X_1	Cout	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

B. Design of Approximate 4:2 Compressor

The 4:2 approximate compressor is designed by two different design provides improved performance compared to an exact compressor in terms of delay, power consumption and transistor count.

i. Design-1 Approximate 4:2 Compressor

The design-1 approximate 4:2 compressor is implemented by making the following modifications in the exact compressor truth table.

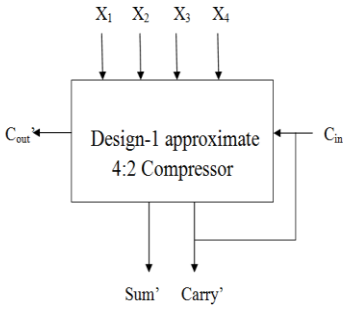


Figure 4. Block diagram for Design-1 approximate 4:2 compressor

In the Exact compressor truth table, out of 32 states 24 has same value in C_{in} and Carry. So,

$$Carry' = C_{in} \quad (7)$$

By reducing the sum value to 0, it produces the approximate outputs that are similar to the exact outputs.

$$Sum' = \overline{Cin}\,(\overline{X1 \oplus X2} + \overline{X3 \oplus X4}) \quad (8)$$

This approximate C_{out} value reduces the error distance given by approximate carry and sum.

$$C_{out}' = \overline{(\overline{X1.X2} + \overline{X3.X4})} \quad (9)$$

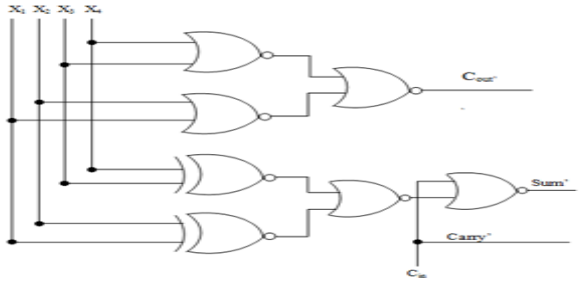


Figure 5. Gate level implementation of Design-1 approximate 4:2 compressor

Table 2: Truth table of Design-1 approximate 4:2 compressor

C_{in}	X_4	X_3	X_2	X_1	Cout'	Carry'	Sum'	Difference
0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	1	0
0	0	0	1	1	0	0	1	-1
0	0	1	0	0	0	0	1	0
0	0	1	0	1	1	0	0	0
0	0	1	1	0	1	0	0	0
0	0	1	1	1	1	0	1	0
0	1	0	0	0	0	0	1	0
0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	0
0	1	0	1	1	1	0	1	0
0	1	1	0	0	0	0	1	-1
0	1	1	0	1	1	0	1	0
0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	0	1	-1
1	0	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	0	-1
1	0	1	0	0	0	1	0	0
1	0	1	0	1	1	1	0	1
1	0	1	1	0	1	1	0	1
1	0	1	1	1	1	1	0	0
1	1	0	0	0	0	1	0	0
1	1	0	0	1	1	1	0	1
1	1	0	1	0	1	1	0	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	0	1	0	-1
1	1	1	0	1	1	1	0	0
1	1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	0	-1

ii. Design-2 Approximate 4:2 Compressor

The design-2 approximate 4:2 compressor is designed in such a way that, the performance of the design which reduces error rate than a design-1 compressor.

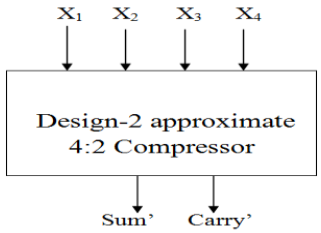


Figure 6. Block diagram for design-2 approximate 4:2 compressor

In this design, Carry and C_{out} have same weight. Thus the Carry and C_{out} value from the design-1 approximate compressor is interchanged.

$$C_{out}' = C_{in} \quad (10)$$

$$Carry' = \overline{(\overline{X1.X2} + \overline{X3.X4})} \quad (11)$$

Whenever C_{in} value is 0, it reflects C_{out} value also 0 in all stages while considering equation(10).Therefore C_{in} and C_{out}, both can be ignored from the design. By substituting C_{in} = 0 in design-1 approximate sum equation,

$$Sum' = (\overline{X1 \oplus X2} + \overline{X3 \oplus X4}) \quad (12)$$

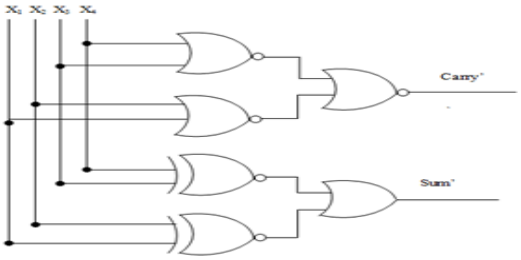


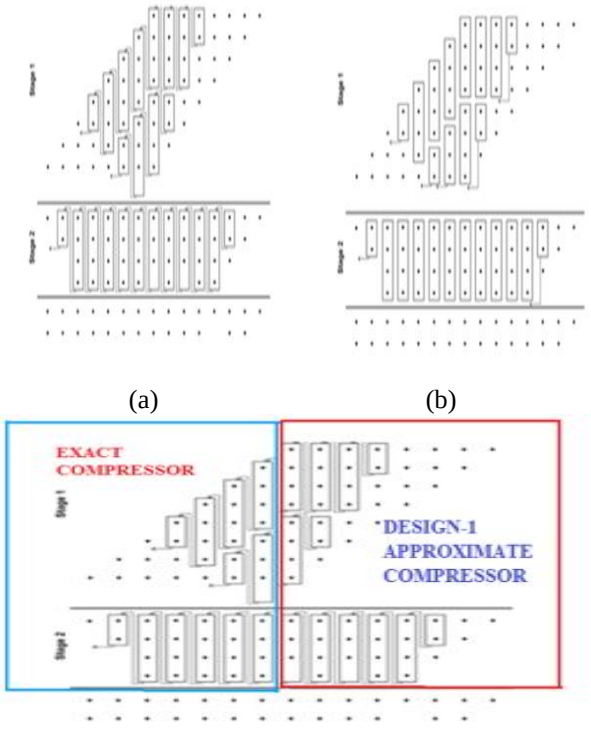
Fig.ure 7. Gate level implementation of Design-2 approximate 4:2 compressor

Table.2 Truth table of Design-2 approximate 4:2 compressor

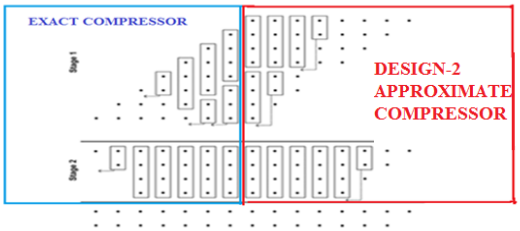
X_4	X_3	X_2	X_1	Carry'	Sum'	Difference
0	0	0	0	0	1	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	-1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	-1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	-1

C. Analysis of 8×8 Dadda Multiplier

The dadda multiplier is analyzed by four different schemes based on the compressor usage is shown in Fig 8.



(c)



(d)

Figure 8. Analysis of Dadda multiplier by (a) Multiplier-1 (b) Multiplier-2 (c) Multiplier-3 (d) Multiplier-4

- In Multiplier-1,Design-1 approximate compressor is used for all 4-2 compressors.
- In Multiplier-2, Design-2 approximate compressor is used for the 4-2 compressors.
- In Multiplier-3, Design-1 is used for LSB and exact compressor for MSB.
- In Multiplier-4, Design-2 is used for LSB and exact compressor for MSB.

D. Applications

This dadda multiplier with 4:2 approximate compressor is used to multiply two images with pixel by pixel. There are two major factors are considered to check the quality of the multiplied image. That are,

- Error Distance(ED)
- Peak Signal to Noise Ratio(PSNR)

Generally, the arithmetic distance between the actual output and error output is known by Error Distance(ED). The PSNR is defined by the ratio of signal power to the noise power. If the PSNR value is in average level, definitely the quality of the image will be improved. ED and PSNR are based on MSE(Mean Squared Error).

$$MSE = \frac{1}{mp}\sum_{i=0}^{m-1}\sum_{j=0}^{p-1}[I(i,j) - K(i,j)]^2 \quad (13)$$

$$PSNR = 10\log_{10}\left(\frac{MAX_I^2}{MSE}\right) \quad (14)$$

where,

m,p - Image dimensions

I(i,j) - Exact value of each pixel

K(i,j) - Obtained value of each pixel

MAX_I - Maximum value of each pixel

III. PROPOSED SYSTEM

The 5:2 compressor is a basic element for high speed and high accuracy multiplier which is shown in Fig 9. To reduce the partial products further during the multiplication process, the proposed two new 5:2 exact compressor is utilized instead of using 4:2 compressor.

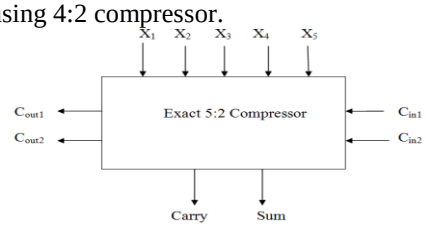


Figure 9. Block diagram of 5:2 compressor

It has five primary inputs X_1, X_2, X_3, X_4 and X_5 with equal weights and sum, carry are the output of the compressor. Carry input (C_{in}) and Carry output (C_{out}) are the bits which are coming from the previous compressor and the next compressor respectively. In this compressor, five inputs, C_{in1} and C_{in2} bits have the same weight with one binary bit in lower significance. It provides sum output with same weight as the inputs. Carry output, C_{out1} and C_{out2} has one binary bit with higher significance. All kinds of 5:2 compressor designs are satisfying the following fundamental equation.

$$X_1+ X_2+ X_3+X_4 +X_5 +C_{in1} +C_{in2} = Sum +2(Carry + C_{out1}+C_{out2}) \quad (15)$$

In the proposed system, exact 5:2 compressor is designed by the following two novel implementations.

i. Design-1 exact 5:2 compressor by full adder
ii. Design-2 exact 5:2 compressor by XOR with Multiplexer

A. Design-1 Exact 5:2 Compressor by Full Adder

The exact 5:2 compressor is implemented by series connection of three Full Adder (FA) blocks. It calculates a sum value with same order to the next stage and carry has one order higher in the next stage. Similarly, both carry input and carry output has one bit higher in the next stage of the compressor. This implementation is shown in Fig 10.

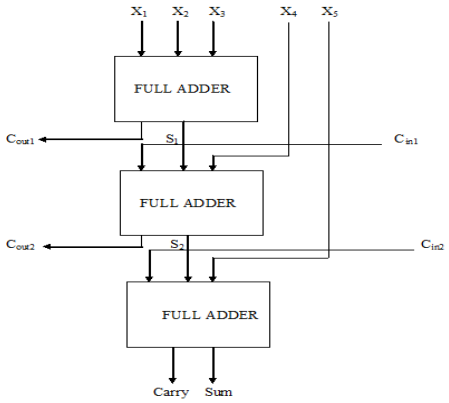


Figure 10. Design-1 exact 5:2 compressor by FA

The outputs of design-1 exact 5:2 compressor design using Full Adder are obtained by the following equations,

$$Sum= X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \oplus C_{in1} \oplus C_{in2} \quad (16)$$

$$Carry=(X1 \oplus X2 \oplus X3 \oplus X4 \oplus X5 \oplus Cin1)Cin2 + \overline{(X1 \oplus X2 \oplus X3 \oplus X4 \oplus X5 \oplus Cin1)}\, X5 \quad (17)$$

$$C_{out1}=(X_1 \oplus X_2)X_3+\overline{(X1 \oplus X2)}\ X_1 \quad (18)$$

$$C_{out2}=(X1 \oplus X2 \oplus X3 \oplus X4)Cin1 + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)}X4 \quad (19)$$

B. Design-2 Exact 5:2 Compressor by XOR With Multiplexer

The efficient implementation of exact 5:2 compressor is designed by XOR with a multiplexer. It has six XOR gates, three 2:1 multiplexers. XOR operation has been implemented over the input signals, Carry and C_{out} signals are generated. XOR output from which the multiplexer selects input based on the selection line or enable as an output is shown in Fig 11.

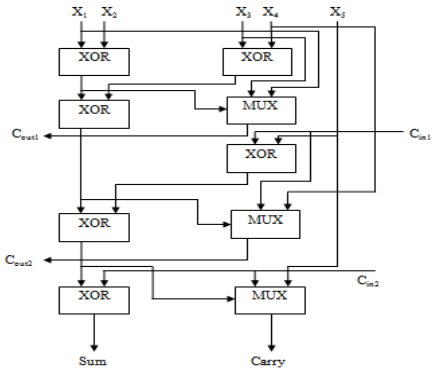


Figure 11. Design-2 exact 5:2 compressor by XOR with MUX

The outputs of design-2 exact 5:2 compressor design using XOR with MUX are obtained by the following equations,

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \oplus C_{in1} \oplus C_{in2} \quad (20)$$

$$C_{out1} = X_1 X_2 + (X_1 + X_2) X_3 \quad (21)$$

$$C_{out2} = (X_4 \oplus X_5) C_{in1} + \overline{(X4 \oplus X5)}\, X_4 \quad (22)$$

$$Carry = ((X_1 \oplus X_2 \oplus X_3) \oplus (X_4 \oplus X_5 \oplus C_{in1}))\, C_{in2} + (\overline{(X1 \oplus X2 \oplus X3) \oplus (X4 \oplus X5 \oplus Cin1)})\, (X_1 \oplus X_2 \oplus X_3) \quad (23)$$

The exact 5:2 compressor using Full Adder(FA) and XOR with a multiplexer implementations has the same output value in terms of Sum,Carry,C_{out1} and C_{out2}.

Table 3: Truth table of exact 5:2 compressor

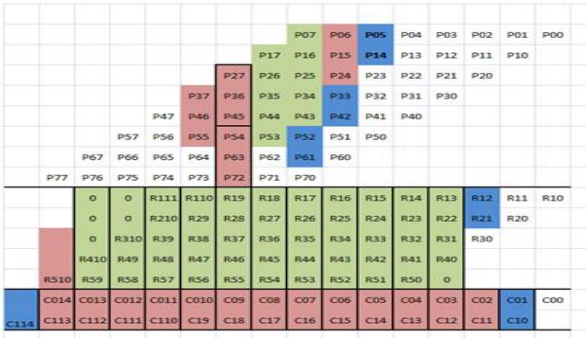
X_1	X_2	X_3	X_4	X_5	C_{in1}	C_{in2}	Sum	Carry	C_{out1}	C_{out2}
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	1	0	0
0	1	0	1	1	0	0	1	0	0	1
1	0	0	0	1	1	0	1	0	0	1
1	1	0	0	0	1	1	0	1	1	0
1	1	0	0	1	1	1	1	1	1	0
1	1	0	0	1	0	0	1	0	1	0
1	1	1	0	1	1	1	0	1	1	1
1	1	1	1	0	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1	1	1

There are lots of input combinations available in the 5:2 compressor, but the some of the input combinations are taken and output values are verified and it is listed in Table 3.

C. Analysis of 8×8 Dadda Multiplier

The dadda multiplier is analyzed by the proposed design-1 and design-2 exact 5:2 compressor is shown in Fig 12.

(a) Design-1 exact 5:2 Compressor



(b) Design-2 exact 5:2 Compressor

Figure 12. Analysis of Dadda multiplier

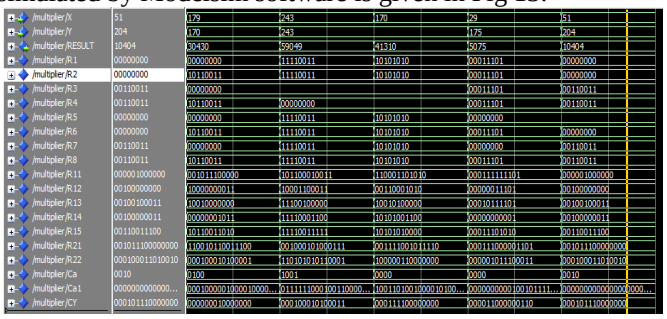
In Fig 12(a) design-1 exact 5:2 compressor is utilized for partial product reduction stages. Similarly, in fig 12(b) design-2 exact 5:2 compressor is used for the reduction process.

D. Applications

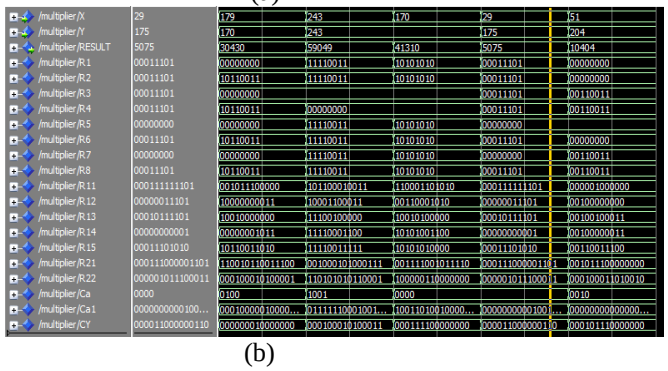
The proposed exact design-1 and design-2 5:2 compressors are used to multiply two images as pixel by pixel basis with high PSNR value than 4:2 compressor.

IV. RESULTS AND DISCUSSION

In this section the proposed two novel implementations of 5:2 exact compressor is designed and simulated by Modelsim software is given in Fig 13.



(a)



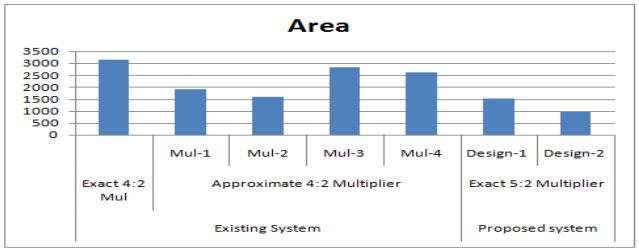
(b)

Figure 13. Output of dadda multiplier with 5:2 exact compressor by (a) Design-1 (b) Design-2

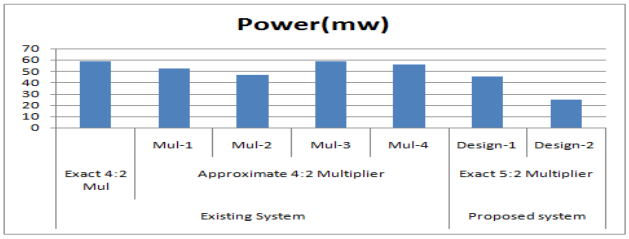
Then the dadda multiplier is analyzed based on area, power consumption and delay. These metrics are compared with existing exact 4:2 compressor is tabulated in Table 4.

Table.4 Comparison report

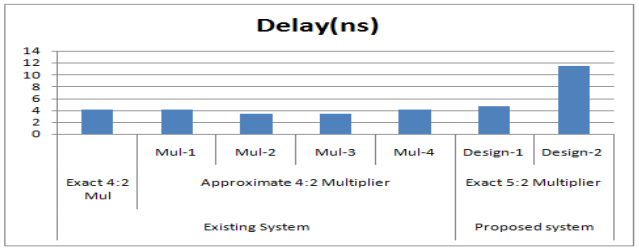
Parameters	Existing System					Proposed system	
	Exact 4:2 Multiplier	Approximate 4:2 Multiplier				Exact 5:2 Multiplier	
		Mul-1	Mul-2	Mul-3	Mul-4	Design-1	Design-2
Area	3146	1901	1602	2845	2599	1534	945
Power(mw)	59	52	47	59	56	45	25
Delay(ns)	4.123	4.123	3.433	3.334	4.123	4.655	11.465



(a)



(b)



(c)

Figure 14. Comparison charts for (a) Area (b) Power (c)Delay for existing and proposed system

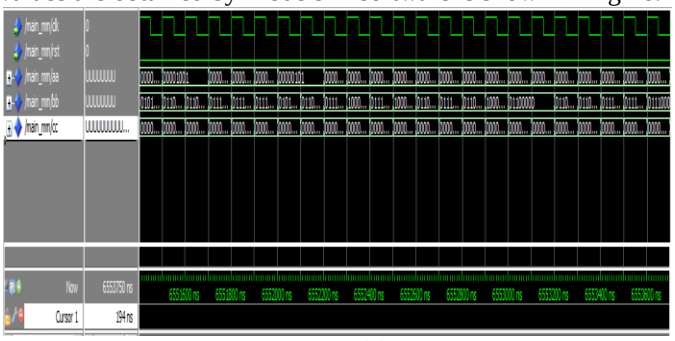
After that the proposed exact 5:2 compressor with dadda multiplier is used to multiply images by pixel basis and the multiplication of images are processed by MATLAB software is shown in Fig 15.

(a)

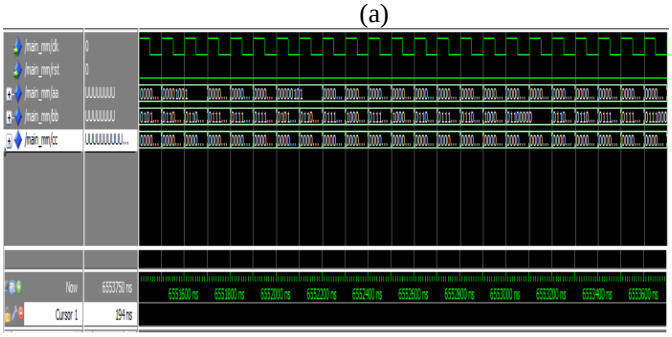
(b)

Figure 15. Image Multiplication for (a) Example-1 (b)Example-2

Each and every pixel values in the input images are multiplied by dadda multiplier and every multiplied pixel values are obtained by Modelsim software is shown in Fig 16.



(a)



(b)

Figure 16. Multiplied value for each pixel on (a) Example-1 (b) Example-2

The quality of the multiplied image is analyzed using PSNR value. The proposed exact 5:2 compressor attains high PSNR value compared to the approximate 4:2 compressor and the results are given in Table 5.

Table.5 Comparison report for PSNR

PSNR	Existing System					Proposed system	
	Exact 4:2 Multiplier	Approximate 4:2 Multiplier				Exact 5:2 Multiplier	
		Mul-1	Mul-2	Mul-3	Mul-4	Design-1	Design-2
Example Image-1	48.13	5.27	3.66	18.48	17.27	48.13	48.13
Example Image-2	48.13	15.22	13.86	23.89	22.79	48.13	48.13

V. CONCLUSION

Two novel implementations of exact 5:2 compressors have been proposed in this paper for analyzing the dadda multiplier based on given metrics for exact multiplication. From the simulation results, existing 4:2 exact compressor provides significant improvement in accuracy,4:2 inexact compressor offers approximate output with less area, power, delay and ED. But these two new 5:2 exact compressor with dadda multiplier provides accurate output with less area, power consumption along with considerable delay than an 4:2 exact and approximate compressors. Also it gives high PSNR value in image multiplication process.

REFERENCES

[1] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, K. Roy, 'IMPACT: Imprecise adders for low-power approximate computing',Low Power Electronics and Design (ISLPED) 2011 International Symposium on. 1-3 August 2011.

[2] Jinghang Liang, Student Member, Jie Han, Member, Fabrizio Lombardi, 'New Metrics for the Reliability of Approximate and Probabilistic Adders', IEEE transactions on computers, TC-2011-12-0946 December, 2011.

[3] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, 'Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications', IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 57, No. 4, pages 850-862,April 2010.

[4] M. J. Schulte and E. E. Swartzlander, Jr., 'Truncated multiplication with correction constant', VLSI Signal Processing VI, pages. 388–396, 1993.

[5] P. Kulkarni, P. Gupta, and MD Ercegovac, 'Trading accuracy for power in a multiplier architecture', Journal of Low Power Electronics, vol. 7,no. 4, pages 490-501, 2011.

[6] J. Gu, C. H. Chang, 'Ultra Low-voltage, low-power 4-2 compressor for high speed multiplications', in 36th IEEE Int. Symp. Circuits Systems, Bangkok, Thailand, May 2003.

[7] Z. Wang, G. A. Jullien, and W. C. Miller, 'A new design technique for column compression multipliers', IEEE Trans. Comput., vol. 44, pages. 962–970, August 1995.

[8] D. Radhakrishnan and A. P. Preethy, 'Low-power CMOS pass logic 4-2 compressor for high-speed multiplication', in Proc. 43rd IEEE Midwest Symp. Circuits Syst., vol. 3, 2000, pages. 1296–1298.

[9] M. Margala and N. G. Durdle, 'Low-power low-voltage 4-2 compressors for VLSI applications', in Proc. IEEE Alessandro Volta Memorial Workshop Low-Power Design, 1999, pages. 84–90.

[10] Baran, Dursun, Mustafa Aktan, and Vojin G. Oklobdzija, 'Energy efficient implementation of parallel CMOS multipliers with improved compressors',Proc. of the 16th ACM/IEEE international symposium on Low power electronics and design. ACM, 2010.

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