

Low power sensitivity and Temperature stability relaxation oscillator for biomedical systems

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Abstract—Nowadays, the increasing concern of people about health has boosted researches on devices and circuits for biomedical systems. The design of low power sensitivity and temperature stability relaxation oscillator for biomedical system has been presented. This oscillator can be applied in any monitoring devices used in biomedical systems. The existing relaxation oscillators have less impact on frequency stability. In order to achieve the high stability in relaxation oscillator, the proposed method employs dynamic switching threshold (DST) technique and limited field (LF) technique. DST technique is proposed to improve the stability of an oscillator frequency against supply voltage. The proposed LF concept is aimed at making the oscillation frequency insensitive to temperature variations. The proposed system was designed in 0.18 μ m CMOS process with 1.84 V power supply. The oscillator in this paper exhibits a competitive performance on frequency stability against both supply voltage and temperature variations by reducing the phase noise and jitter.

Index Terms—

Biomedical systems, frequency stability, dynamic switching threshold (DST), relaxation oscillator, limited field (LF), jitter.

I. INTRODUCTION

The biomedical devices are those that save the most lives and help to improve the patient health, quality of the life of an individual's, effectiveness and delivery of clinical medicine. As medical practice became more technologically based, a progressive

shift is occurring in industry to meet the demand [1]-[3]. A self-chopped relaxation oscillator with adaptive supply generation provides the stable output clock against variations in temperature and supply voltages. The cost is less but power consumption is high [4]. Biomedical armamentaria with wide working temperature range are more attractive for better reliability in biological applications under harsh conditions. In addition, operating with wider range of supply voltage is also appreciated to extend the working time when powered by sources with finite energy. The crystal oscillators are very stable versus temperature and supply voltage variations they cannot be integrated. In a CMOS a high performance in phase noise, jitters and also in frequency stability against environment variations, such as process, supply voltage, and temperature. The external devices cause excessive cost and integration problems. In biomedical applications such as the collection of life parameters and the check of functioning of living organism more concern is focused on the stability of oscillators against PVT variations rather than jitters or phase noise [5],[6]. Relaxation oscillators are more valuable as on-chip clock generators embedded in biomedical systems. Many research activities have been carried out on high-stability relaxation oscillators. Simple resistive and capacitive temperature compensation techniques for relaxation oscillators acceptable high temperature performance particularly, for applications operating below 200°C such as the target application of this work that is monitoring environmental

variables (e.g., temperature and pressure) inside a pulp and paper digester where the temperature can go as high as 180°C [7]. In a 1.1-MHz sub microwatt current-mode relaxation oscillator the current-starving inverters are biased by using the current sources with positive and negative temperature coefficients. It relaxes the temperature variations. The transistors in the sub threshold region, the current-mode comparator, and the current starving inverters are used to reduce the power of the relaxation oscillator. The current-starving inverters are biased by using the PTAT and CTAT current sources to release the temperature variations. The parallel/series composite resistor and the PTAT/CTAT current sources are also used to further reduce the temperature coefficient [8].

Recently, a relaxation oscillator that utilizes electron mobility as a time reference has been reported [9], which, as opposed to mixing resistors. This is less suffered from process variations at the cost of degraded temperature stability.

In this brief, a low power sensitivity and temperature stability relaxation oscillator for biomedical system was presented. The concept of dynamic switching threshold (DST) technique and limited field (LF) technique was employed to attain a high stability in relaxation oscillator.

This brief is organized as follows. Section II describes the related works. Section III describes circuit description. Section IV presents the experimental results. The conclusions are given in Section V.

II. RELATED WORKS

Dynamic threshold (DT) is used to enhance the frequency stability of an oscillator against supply voltage. The SR is proposed to mitigate the frequency drift of the oscillator when temperature changes. Temperature dependence of frequency is mainly caused by the large TC of resistors applied in the circuit. The main drawback of this work is that phase noise and jitter is high [13]. In order to handle low common-mode inputs, a PMOS-input design is used and saturation of the input pair is ensured by sub-threshold operation. Transconductance efficiency is also maximized, hence by reducing power. The main drawback in this work is that voltage drop is high [14]. On-chip oscillators are strongly demanded for the external-XO replacement by low-

cost and single-chip systems.

An oscillator with frequency tracking loop provides a stable output clock under wide supply and temperature variations, but it requires a BGR circuit with high-precision, which induces costs [4].

III. CIRCUITS DESCRIPTION

The block diagram of relaxation oscillator consists of two comparators, a effective capacitor and a latch, as depicted in [10].

The capacitor is alternately charged to V_{OH} and discharged to V_{OL} by a constant current I_C depending on the state of the RS latch. The period of the relaxation oscillator can be expressed as

$$T = 2C_f(V_{OH} - V_{OL}) / I_C + 2t_p \quad (1)$$

Where C_f , V_{OH} , V_{OL} , I_C and t_p are the effective capacitance, high threshold voltage, low threshold voltage, charge and discharge current and delays of comparators and latch.

In order to increase the stability of an oscillator to the supply voltage variation, BGR or current reference is usually employed [5],[6]. These techniques minimize the frequency drift caused by supply variation as well as by temperature changes. In this brief, DST and LF techniques are proposed to improve the stability of an oscillator frequency against supply voltage and temperature changes.

A. DST Technique

The DST technique is proposed to mitigate the frequency drift of an oscillator against supply voltage. The circuit implementation of DST technique is shown in Fig.1. The circuit consists of a timing capacitor, one comparator, a timing resistor, some batches of current.

- When voltage at node B (V_B) is greater than voltage at node A (V_A), the comparator output will be V_{OH} and turns the switches S_C and S_G on. In this period the capacitor will get discharged and results in a decrease of voltage at node B (V_B).
- When voltage at node A (V_A) is greater than voltage at node B (V_B), the comparator output will be V_{OL} and turns the switches S_C and S_G off. In this period the capacitor will get charged and results in an increase of voltage at node B (V_B).

voltage at node B (V_B), the comparator output will be V_{OL} and turns the switches S_C and S_G off. In this period the capacitor will gets charged and changes the state of oscillator to the charging phase.

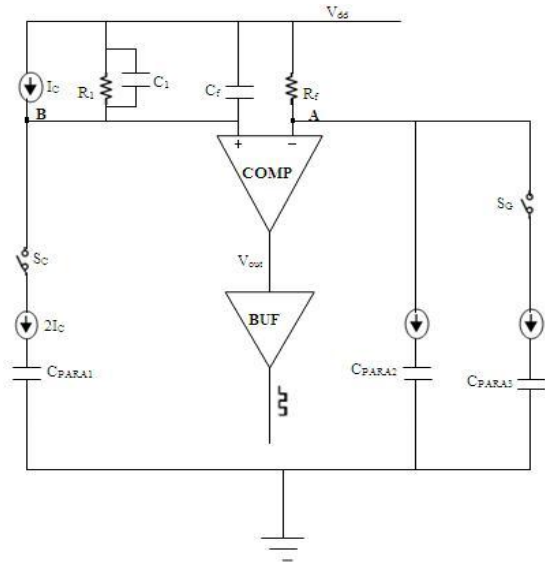


Fig. 1. Circuit schematic of proposed DST technique

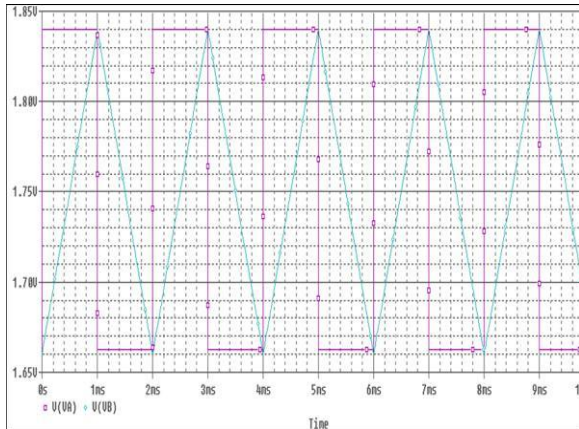


Fig. 2. Simulation waveforms of V_A and V_B .

By observing the above operating mechanism, both high and low threshold voltages are dynamic and temporal. According to DST technique, the oscillation period can be written as

$$\Phi = 2 \frac{Cf(V_{OH} - V_{OL})}{I_C} + 2t_{p+}Cpara \quad (2)$$

where C_f , I_C , t_p are effective capacitance, charging currents and delays of comparators.

$$\Phi = 2R_1C_fI_C + 4t_p + Cpara(3)$$

In several MHZ applications, t_p is negligible with sufficient gains of the comparator, the reason is that it is a primary contributor to power consumption and might consume hundreds of μA currents at frequency bands of MHz.

B. LF Technique

The circuit schematic of the proposed LF technique is shown in Fig. 2. The proposed LF concept is aimed at making the oscillation frequency insensitive to temperature in a process providing at least two types of resistors with different TC_S . In addition, a three parasitic capacitor is added in series to the circuit. Control signals are derived from the output of the comparator. The selection of V_{OUT+} / V_{OUT-} is determined by the polarity of TC_S of R_1 and R_2 .

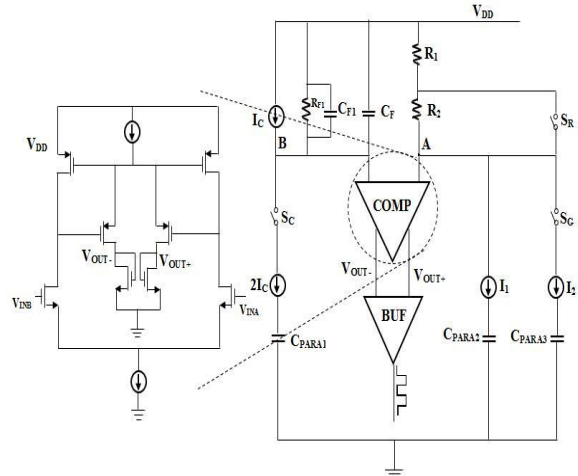


Fig. 3. Circuit of the proposed LF technique.

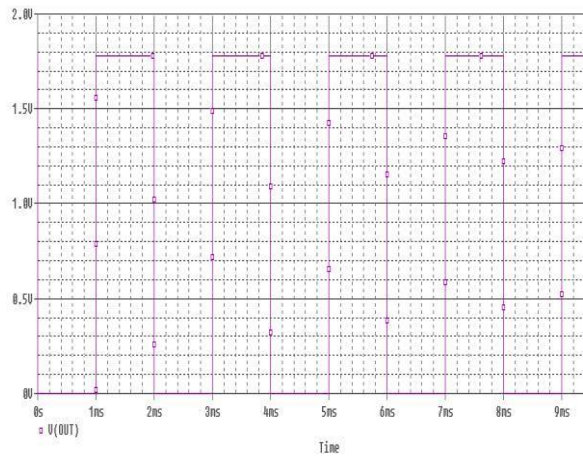


Fig. 4. Output waveform of buffer

- TC_S of R_1 and R_2 have the same polarity: In this case, S_R and S_G must have the same

steering signals. With t_p being ignored, the expression of oscillation period in (2), (3) should be modified correspondingly as

$$\Phi = 2C_{TC} \ln \left(\frac{V_{DD} - V_{OL}}{V_{DD} - V_{OH}} \right) + C_{para}(4)$$

$$\Phi = 2C_{TC} \ln \left(\frac{I_1 R_1 + I_2 R_2}{I_1 R_1} \right) + C_{para}(5)$$

As TCs of capacitor and the second-order TCs of resistors are ignorable with respect to the first-order TCs of resistors, the oscillation period in terms of temperature can approximately be

$$\Phi = 2C_{TC} \ln \left(\frac{I_1 R_1 + I_2 R_2}{I_1 R_1} \right) + C_{para}(6)$$

The above expression is for the first-order TCs of resistors at room temperature.

- TC_S of R_1 and R_2 have the different polarity: In this case, to ensure proper charging and discharging timing, SG must be controlled by V_{out+} .

IV. EXPERIMENTAL RESULTS

The oscillator was designed and implemented with a standard 0.18- μ m CMOS process with the supply voltage of 1.84V. The previous system suffers from large area and high cost. Though our proposed system occupies less area and less cost. Mostly the biomedical systems have embedded memory arrays for critical information and data storage, which can be utilized for frequency calibration by digitally tuning I_C , I_1 , I_2 rather than resistors and capacitors for area saving. In the present design, registers were employed as memories to store the calibration information for the sake of flexibility in testing. In addition, the currents I_C , I_1 , and I_2 are binary coded. The variation of resistors TCs caused by that of process is not her breakertotemperature stability of the oscillator. However, the impact is negligible as TCs of resistors are almost constant against process variation [11], [12]. The oscillator in this paper exhibits its competitive performance of frequency stability against both supply voltage and temperature variations by reducing the phase noise and jitter. Further the area can be reduced by eliminating the decoders and registers.

V. CONCLUSION

This paper has proposed a new concept of DST and LF technique for relaxation oscillator and

analytically explained its immunity against power supply and temperature variations. The minimum achievable sensitivity was generalized to be independent of oscillation frequency. The noise reduction mechanism of DST and LF technique was explained. A system was designed in a 0.18 μ m standard CMOS process with 1.84V power supply. A performance comparison with recent works resulted that our work achieved small area and low power with competitive low sensitivity to voltage and temperature. This oscillator can be applied in any monitoring devices used in biomedical systems.

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