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Low Power SRAM Design Based on Hetero Junction CMOS Technology for Wireless Sensor Networks

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***Abstract*— Nowadays, Wireless Sensor Network (WSN) draws attention in emerging applications such as industrial monitoring and security surveillance. Since a static random access memory (SRAM) is a key circuit in a sensor node of WSN, it is important to reduce its power consumption. This paper proposes a single bit line (BL) SRAM design using hetero junction complementary metal oxide semiconductor (CMOS), to reduce the power consumption of the SRAM. The static noise margin of the single BL is higher than the conventional SRAM with two BL, since the single BL SRAM uses only-one bit-line for the read operation. The hetero junction CMOS technology provides a low noise ratio, to enhance the operating speed of the SRAM. The accuracy of the proposed SRAM circuit is higher than the conventional system. Hence, the design of the SRAM is simplified by using the hetero junction CMOS, to achieve low power consumption and high area efficiency.**

***Index Terms*— Bit Line, Hetero Junction Complementary Metal Oxide Semiconductor (CMOS), Static Noise Margin, Static Random Access Memory (SRAM) and Wireless Sensor Network (WSN)**

I. INTRODUCTION

Wireless Sensor Network (WSN) is utilized in the real-time applications such as industrial application and security application, due to the improved operating performance and energy efficiency. Since a static RAM (SRAM) is a key circuit in a sensor node, it is important to reduce the power consumption of the SRAM, for achieving high network performance. One way to reduce the power consumption level of the SRAM is to reduce the supply voltage. The size of the SRAM is reduced, to achieve significant reduction in the power consumption. The static noise margin is reduced, due to the large variation in the threshold voltage. Adiabatic charging of a word line (WL) in a single-BL SRAM to stabilize the flip-flop (FF) is performed. Single-BL reading is achieved by using a shared reading port. The shared reading port greatly reduces the capacitance of the bit line, while enabling the BL voltage connected to the low-voltage node of the flip-flop to change from the precharge voltage to GND. But due to the shared ports in the circuit, there is occurrence of leakage in the SRAM circuit. Power consumption of the traditional SRAM circuit is high due to the leakage. Significant efforts have taken to find ways to reduce the leakage in the SRAM cell. The existing leakage reduction techniques cannot be applied beyond certain limits, while rendering them ineffective for the ultra-low power domain. The two operation modes of the sensor node are data processing mode and idle mode. With the primary function of reducing the leakage power, good cell stability reflected by a high static noise margin (SNM) has become a critical design objective for the SRAM used in WSN applications.

An obvious way to reduce SRAM energy per operation is to reduce the supply voltage, which reduces the active power quadratically and leakage power linearly. The performance of the SRAM is improved even at a lower supply voltage, by modifying the architecture of the existing SRAM circuits while keeping the reliability and process variation in mind. In the conventional SRAMs, minimum feature sized devices are preferably used to provide high cache density. As a result, there is a significant degradation in the read and write stability due to process variation. The importance of SRAM working at low power and nano-regime is increased nowadays. The design of the sub-threshold SRAM cells reduces both leakage and energy for low power applications and introduces compatibility with the sub-threshold logic to allow system integration. To increase the read stability, extra peripheral circuitry is added to the SRAM circuit. But this will lead to the increase in the power consumption and area of the SRAM design.

With scaling of devices to the nanometer regime, the problems of static power dissipation, cell stability due to variation in process parameters and noise in memory cells become a matter of concern. The considerable amount of power consumption during memory access is also a key factor to be considered for the application of SRAM circuit in WSN. Hence, efficient SRAM designs are required to address the leakage power problems. The data read operation of SRAM cells must be non-destructive and static noise margin must be in an acceptable range. The lowest operational voltages of the SRAM cells are limited by the cell stability and write ability. The area of the SRAM Cell is also very important as it contributes to the silicon area and power consumption. SRAM cells are designed to ensure the stable read operation, so that the contents of the cell are not altered during read access, and the cell can quickly change its state during write operation. These conflicting requirements for read and write operations are satisfied by sizing the bit cell transistors to provide stable read and write operation. During the read operation, an SRAM bit cell is most prone to failure.

Generally, the immunity of SRAM cell to static noise is expressed in terms of Static Noise Margin (SNM). The SNM is defined as the maximum amount of noise voltage V_N at both input terminals of the cross-coupled inverters in different directions. In other words, the SNM quantifies the amount of noise voltage V_N required at the storage nodes of the SRAM to flip the cell data. Static Noise Margin is an important factor for the stability and speed of SRAM cell. The SRAM cell stability depends on the different types of noise analysis. The pull up ratio and cell ratio are the two important parameters of SRAM cell, since they are changed by the design engineer. Reduction in the static noise margin leads to the degradation in the performance of the SRAM cell. Hence the static noise margin is to be improved, for better performance of the SRAM cell.

In order to overcome these drawbacks, this paper proposes a single BL SRAM with hetero junction CMOS technology for WSN. The major characteristics of the CMOS devices are high immunity to noise and low static power consumption. The hetero junction CMOS technology provides a low noise ratio, to enhance the operating speed of the SRAM. Hence, the design of the SRAM is simplified by using the hetero junction CMOS, to achieve high area efficiency. Significant reduction in the power consumption and noise level of the SRAM is achieved.

The rest of the paper is systematized as follows: Section II describes about the conventional SRAM circuit with flip-flop. Section III illustrates about the system design and section IV describes about the proposed SRAM design with hetero junction CMOS. Section V describes the simulation results of the proposed SRAM system and section VI illustrates the conclusion of the proposed low-power SRAM circuit.

II. Related Work

Nakata et al [1] suggested adiabatic charging of the single-bit-line (BL) static RAM (SRAM) to reduce the power consumption. Adiabatic charging of a word line in the single BL SRAM circuit during the read operation is found to provide a large dynamic noise margin (DNM) for reading. An analysis of the time-wise change in the DNM revealed that the read noise margin of this circuit is 1.9 times larger than that of a conventional two-BL circuit. This circuit enables the design of an SRAM that is smaller than a conventional one, resulting in lower energy consumption. But due to the shared ports in the SRAM circuit, there is occurrence of leakage in the circuit. Nakata et al [2] designed a 64-kb SRAM circuit with a single BL SRAM circuit for the reading operation. In addition, this paper proposes a new sense amplifier circuit for single-BL reading and a divided word line architecture for writing to maintain the static noise margin for unwritten blocks at a specific level.

Tache et al [3] suggested a novel reliability-oriented design method based on the unconventionally sizing transistors. The main aim of the proposed method is to design, simulate and compare the benefits of unconventional sizing transistors applied to ultra-low voltage (ULV) SRAM cells. The unconventionally sized SRAM cells achieve higher static noise margin (SNM) than the classically sized SRAM cells. Samson and Mandavalli [4] suggested the design of energy efficient 5-transistor (5T) SRAM suitable for high density embedded systems. The energy saving on the single bit line is achieved using an energy recovery driver, and the write ability of the 5T SRAM is enabled. Gavaskar and Raghupathy [5] presented a power analysis model for the adiabatic SRAM. The power characteristics of the proposed model are simulated, analyzed and compared with various performance frequencies and voltage levels. The simulation results show the power saving is achieved up to 20% over a frequency range of operation of 10MHz to 200MHz respectively against the static CMOS implementation.

Narayanan and Sharma [6] proposed a novel 8T SRAM cell to improve the read stability and write ability, using a single bit-line scheme. A Buffered read scheme separating the SRAM cell nodes from the bit-line is utilized, to enhance the read stability. The power consumption of the proposed cell during the bit-line pre-charging or discharging operation is reduced. The simulation results show that the proposed cell achieves high read noise margin and write ability, when compared with the conventional 6T SRAM cell. Ebrahimi et al [7] proposed a novel 8T subthreshold SRAM cell to improve the writing characteristics. A novel 10T subthreshold SRAM cell is also suggested, based on Fin Field Effect Transistor (FinFET) structures with low standby power. The comparison results show that the 10T structures exhibit better write characteristics and consume less static power. Akashe et al [8] proposed 7T SRAM cell without any direct paths to the data storage nodes, through bit-line (BL). The proposed cell with two separate data access mechanisms for reading and writing operations, shows higher endurance against external noise. Based on the comparison of the power consumption of the conventional 6T and proposed 7T cell, the performance of the proposed cell is higher than the conventional cell.

Kushwah and Vishvakarma [9] presented a single ended 8-transistor (8T) SRAM cell for sub-threshold operation, to achieve improved data stability. The proposed cell interrupts the feedback between true storing nodes, to enhance the writeability of the cell at ULV power supply. The proposed cell achieves a higher mean of write static noise margin as compared to the conventional upsized 6T cell for 200 mV power supply. Upadhyay et al [10] proposed 10T SRAM cell based on the static and dynamic power dissipation analysis and stability analysis. Two stack transistors are connected in the pull-down paths, to increase the threshold voltages of the transistors, while reducing sub-threshold leakage current and static power dissipation. Gavaskar and Priya [11] recommended a novel 9T SRAM cell design that consumes less dynamic power. This paper includes the SRAM array structure consisting of sense amplifier and address decoders. The read stability of the proposed design is improved, without increasing the power consumption.

Madiwalar and Kariyappa [12] proposed a new 7T SRAM cell using single BL, to provide high static noise margin (SNM). The power consumption of the proposed cell is reduced, because of the usage of the single bit line. The read

stability of the 7T SRAM cell is very high compared to the conventional 6T SRAM cell. Gopal et al [13] suggested a novel eight transistor (8T) CMOS SRAM cell design to reduce dynamic and leakage power and improve the stability. The proposed 8T SRAM cell has achieved significant reduction in the dynamic power and leakage power compared with the conventional cell. Kushwah [14] et al proposed a novel FinFET 7T cell with improved writability at ULV, without any boosted supply. The hold static noise margin (HSNM) of the proposed cell is improved, when compared to the upsized 5T (U5T) cell. The read power consumption is reduced significantly, when compared with the write power consumption of U5T cell. The write trip point (WTP) of the proposed cell is lower than the WTP of the U5T cell, at 100mV. Moradi and Madsen [15] presented a novel subthreshold 8T-SRAM for ultra-low power applications. The proposed SRAM cell improves write margin by at least 22% to the standard 6T-SRAM cell at a supply voltage of 1V. Furthermore, read static noise margin is improved by atleast 2.2X compared to the standard 6T-SRAM cell. The proposed SRAM design improves write margin of the SRAM cell in comparison to the standard 7T-SRAM cell.

During the deep sub-threshold operation, the SRAM cell suffers from the write failures and read failures at the low supply voltage. Chang et al [16] proposed a 9T-SRAM cell to increase the dynamic-read-decoupled scheme and write margin. The proposed design prevents read-disturb failures, for achieving deep sub-threshold operation. A negative-pumped wordline scheme is used to suppress bitline leakage current. The proposed cell achieves 130 mV at the minimum supply voltage. The sub-threshold leakage is a major issue for the SRAM design. By reducing the supply voltage, the sub-threshold leakage can be decreased. However, this results in the dramatic increase in the circuit delay. Chen and Cheng [17] proposed a novel 6T SRAM array structure along with a switch module operating in the near threshold region, for reducing the leakage current. An 8192 kB SRAM array is designed and simulated based on the 16 KB single port SRAM cell memory model. With the proposed technique, 28.3% reduction in the leakage current is achieved compared to the traditional 6T SRAM array, in the standby mode.

Due to the increasing demand of the extra-low-power system, there is a need to develop an effective and economic sub-threshold SRAM design. Lin et al [18] recommended categorization of the sub-threshold SRAM designs and studied the faulty behavior of open defects and address decoder faults on each design. The impact of open defects and threshold-voltage mismatch on the sense amplifiers is discussed under the sub-threshold operations. Divyapriya and Ramamoorthy [19] proposed a novel low power 6T SRAM cell with single bitline to enhance the stability. SRAM energy efficiencies can be achieved with a wider SRAM array structure with fewer rows than the columns particularly at low supply voltage. In the proposed 6T SRAM cell, write operation is done by charging or discharging single bit line (BL). Reduction in the dynamic power consumption is achieved. Simulation results show a better efficiency for the same SRAM bit density and the same supply voltage. Majumdar and Basu [20] presented a novel CMOS 6-transistor SRAM cell for various applications. Also, the proposed cells uses a single BL for both read and write purposes. The read stability of the proposed cell is improved, while consuming less dynamic power. The read stability of the conventional SRAM cell is very low, due to the voltage division between the transistors during the read operation. Reduction in the dynamic power consumption of the SRAM cell is achieved, by performing the charging and discharging of the single BL during the read and write operation.

The conventional SRAM circuit utilizes a two-precharged BL for the read operation. But due to the shared ports in circuit, there is occurrence of leakage in the SRAM circuit. Power consumption of the traditional SRAM circuit is high due to the leakage. In order to overcome these drawbacks, this paper proposes a single BL SRAM design. The single BL design has a larger static noise margin than the SNM of the two-BL SRAM circuits. Significant reduction in the power consumption and noise ratio of the SRAM is achieved.

III. SYSTEM DESIGN

A. CMOS DESIGN

Complementary metal–oxide–semiconductor (CMOS) is utilized for the construction of the integrated circuits. The CMOS technology is utilized in SRAM, microcontrollers, microprocessors and various digital logic circuits. CMOS technology is also utilized for analog circuits such as image sensors (CMOS sensor), data converters and highly integrated transceivers for many types of communication. The major characteristics of the CMOS devices are high immunity to noise and low static power consumption. The series combination of the transistors draws significant power momentarily during switching between the ON and OFF states, since one transistor of the transistor pair is always OFF. Consequently, the CMOS devices do not produce much waste heat. Therefore CMOS integrated circuits are used widely to develop the SRAM. The hetero junction CMOS technology provides a low noise ratio, to enhance the operating speed of the SRAM.

B. SRAM DESIGN

SRAM is a type of semiconductor memory that uses bistable latching circuit for storing each bit. The SRAM is differentiated from the dynamic RAM (DRAM) which should be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that there is the eventual loss in the data, when the memory is not powered. The storage cell comprises two stable states to denote “0” and “1”. A typical SRAM cell consists of six metal oxide semiconductor field effect transistors (MOSFETs). Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that constitute two cross-coupled inverters. Two additional access transistors control the access to a storage cell during the read and write operations. The word line (WL) controls the access transistors M5 and M6 that controls the connection of the cell

to the bit lines BL and $\overline{BL}$, for enabling access to the cell. The Bit lines are used to transfer data for the read and write operations. Even though it is not necessary to have two bit lines in the SRAM circuit, both the signal and its inverse are usually provided for improving the noise margins.

C. Writing circuit, Self-enabled switching circuit and Reading circuit

The writing circuit enhances the Spin transfer torque-magnetic random access memory (STT-MRAM) architecture. To optimize the complexity level. The write driver provides a bidirectional current passing through magnetic tunnel junction (MTJ). The enable circuit to improve the writing speed in STT-MRAM architecture. Although the speed of STT switching is proved as fast as subnano second, the STT switching is stochastic. Some input data could not be stored correctly during one limited writing pulse. Both the power-efficient write operation and the whole lifetime of MTJ can be greatly improved, because of the shortened switching duration and the reduced switching number. The analysis of the sensing output is worse due to the high resistance in sensing circuit. The reliability of the reading circuit is improved.

IV. LOW-POWER SRAM DESIGN BASED ON HETERO JUNCTION CMOS TECHNOLOGY

This paper proposes a low-power SRAM design based on hetero junction CMOS technology. The major characteristics of the CMOS devices are high immunity to noise and low static power consumption. The series combination of the transistors draws significant power momentarily during switching between the ON and OFF states, since one transistor of the transistor pair is always OFF. Consequently, the CMOS devices do not produce much waste heat. Therefore CMOS integrated circuits are used widely to develop the SRAM. The hetero junction CMOS technology provides a low noise ratio, to enhance the operating speed of the SRAM. The static noise margin of the single BL SRAM is higher than the conventional SRAM with two BL, since the single BL SRAM uses only one BL for the read operation. Hence, the design of the SRAM is simplified by using the hetero junction CMOS, to achieve high area efficiency. Significant reduction in the power consumption and noise level of the SRAM is achieved.

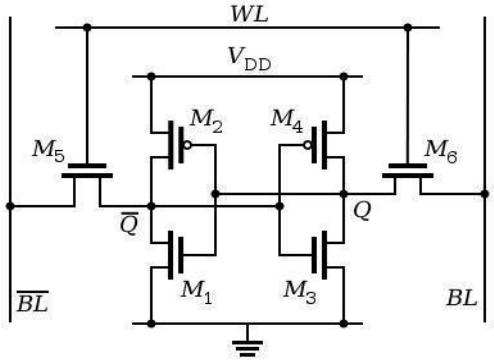

Fig.1 Circuit diagram of SRAM

Fig.1 shows the circuit diagram of the SRAM cell. Four transistors form two cross coupled inverters. Each bit in the SRAM is stored on four transistors. The stable states of the storage cell denote “0” and “1”. Two additional transistors serve as the access transistors to control the storage cell during the read and write operations. The smaller cells reduce the cost per bit of memory, since the processing cost of the silicon wafer is relatively fixed. The word line (WL) enables access to the SRAM and controls the access transistors, by controlling the connection of the cell to the bit lines BL and $\overline{BL}$. The BLs transfer data during the read and write operations. The signal and inverse are typically applied to the bit lines to improve the noise margins. The inverters performs active driving of the bit lines to the high and low states, during the read operation. The SRAM should require “readability” and “write stability”, to operate in the read mode and write mode.

A. Reading mode

Consider the assumption that the content of the memory is “1” and stored at the transistor Q. The read operation is performed by using the sense amplifiers that pull the data and produce the output. The row decoders and column decoders are used to select the appropriate cell for reading data and are given to the sense amplifiers through the transmission gate.

To read logic ‘0’: The bit lines BL and $\overline{BL}$ are pre charged to „1“. The word lines are made high (transistors M5 and M6 turns ON). M2 and M3 are ON and M1 and M4 are OFF. Hence VDD flows to the bit line $\overline{BL}$ through M5 and M2keeping it in logic state „1“. On the other hand, the bit line BL is connected to ground through the transistors M6 and M3 making it into logic state „0“.

To read logic ‘1’: First the bit lines BL and $\overline{BL}$ are pre charged to „1“. The word lines are made high (transistors M5 and M6 turns ON). M1 and M 4 are ON and M2 and M3 are OFF. Hence bit line is connected to VSS making it into „0“. On the other hand the bit line BL is connected to VDD through the transistors M6 and M4, while keeping it in logic state „1“.

B. Writing mode

By applying the writing value to the bit lines, the start of a write cycle is initiated. The bit line BL is set to 0 and $\overline{BL}$ is set to 1, for writing “0”. The values of the bit lines are inverted, for writing “1”. Then the word line is declared, for latching the value that is to be stored into the word line. The input drivers of BLs are designed to be more durable than the transistors in the cell, so that the input drivers can easily perform the overriding of the previous state of the cross-coupled inverters.

To write logic ‘0’: Set BL to „0“ and $\overline{BL}$ to „1“and the word lines are made high (transistor“s M5 and M6 turns ON). The logic „0“ in the bit lines enters to the first cross coupled inverter and turns ON transistor M2 and turns OFF transistor M1. Hence VDD flows through M2 and $\overline{Q}$ remains high. As $\overline{BL}$ is made logic „1“, then transistor M3 turns ON and M4 goes OFF, thereby keeping Q as „0“.

To write logic ‘1’: Set BL to „1“ and $\overline{BL}$ to „0“and the word lines are made high (transistor“s M5 and M 6 turns ON). The

logic „1" in the bit lines enters to the first cross coupled inverter and turns ON transistor M1 and turns OFF transistor M2. Hence $\overline{BL}$ is connected to ground via transistor M1. On the other hand, when is made logic „0" transistor M4 is ON and M3 is OFF, thereby VDD keeps BL at logic „1" through transistor M4.

C. Read Stability

Data retention capability of the SRAM cell during the standby mode and reading mode is a significant functional constraint in the advanced technology nodes. The stability of the SRAM cell becomes low with the reduction in the supply voltage. The increase in the leakage current and variability of the SRAM cell results due to the technology scaling. The read stability of the SRAM cell is usually defined by the SNM. The cell is more vulnerable to noise during the read operation, due to the rise in the voltage level of "0" internal storage node than the ground. Owing to this voltage division, the SNM is primarily determined by the ratio of the pull down (PDN) to pass gate (PG) transistor, known as the cell ratio. The read margin of the SRAM cell is directly proportional to the cell ratio. Each of the two cross-coupled inverters has an infinite gain, during the ideal case.

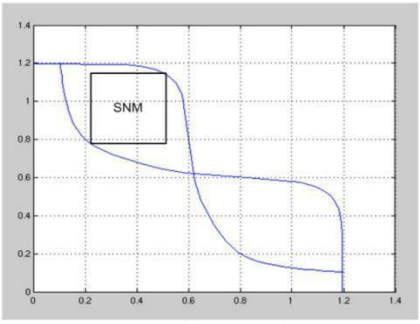

Fig.2 Butterfly curve of SNM

The two-lobed graph called as a "butterfly" curve is shown in the Fig.2. The butterfly curve is used to determine the SNM of the SRAM cell. The SNM value is defined as the side length of a large square that can be fitted inside the lobes of the "butterfly" curve. The read stability of the SRAM cell is high, with the increase in the SNM value. The read stability of the SRAM cell is poor, when the value of Read SNM (RSNM) is low. Fig.3 shows the schematic diagram of the proposed SRAM circuit with hetero junction CMOS to reduce leakage power.

During the read operation, there is a decrease in the read-SNM. This is due to the reason, that the read-SNM is calculated, when the WL is set to be high and both BLs are still pre-charged high. At the beginning of the read operation, the access transistor is set to "1" and the bit-lines are already pre-charged to "1". There is a significant degradation in the SNM due to the increase in voltage, during the read operation. During the read operation, a stored "0" can be overwritten by a "1", due to the positive feedback mechanism.

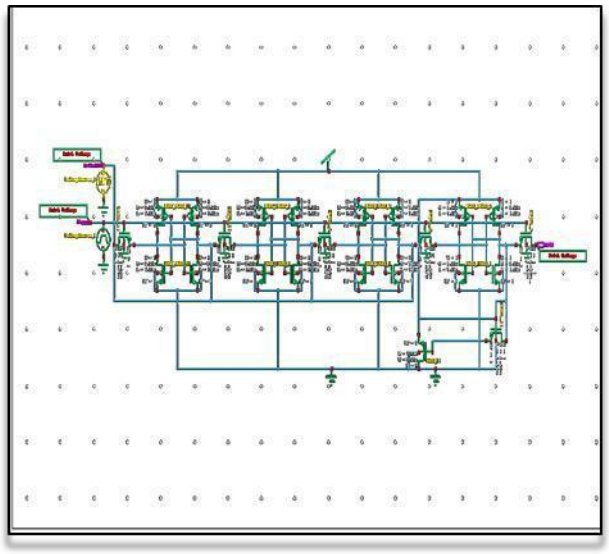

Fig.3 Schematic diagram of the proposed SRAM circuit

V. SIMULATION RESULTS

Tanner EDA 13.0 is utilized as a simulation tool to show the performance analysis of the proposed SRAM circuit. The comparison between the read noise margin and accuracy of the proposed SRAM circuit with the conventional SRAM design with flip flop is performed.

Fig.4 Input and output signals of SRAM circuit

Fig.4 shows the input and output signals of the SRAM circuit. Initially, the clock is enabled and then the input data values are assigned. The read and write operations are performed, after the simulation process.

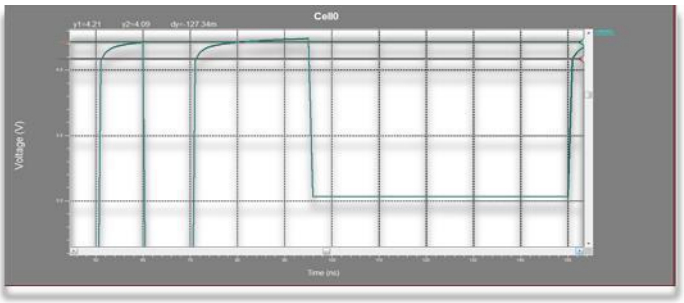

Fig.5 Read noise margin of the proposed system

Fig.5 shows the read noise margin of the proposed system. The simulation result shows that the leakage power obtained in the proposed circuit is 127 mV.

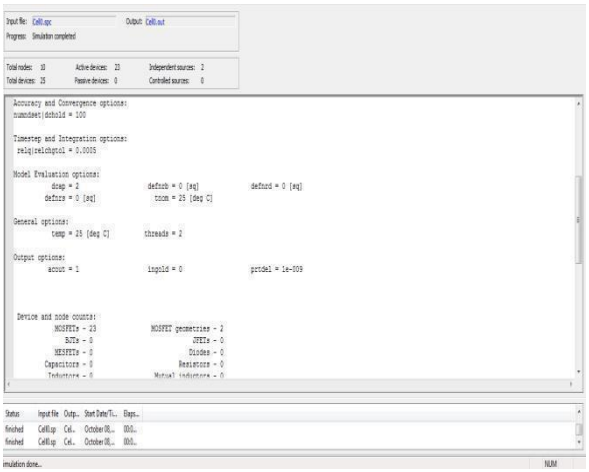

Fig.6 Accuracy result

Fig.6 shows the accuracy result of the proposed SRAM circuit design. The proposed SRAM circuit achieves 100% accuracy, while the existing design achieves 98% accuracy rate.

The simulation result shows that the leakage power obtained in the proposed circuit is 127 mV. Therefore, the leakage power of the proposed SRAM circuit is less than the conventional circuit. The accuracy of the proposed circuit is higher than the conventional circuit. Hence it implies that the proposed circuit is more efficient than the existing SRAM circuit. The reduction of noise in the read port and delay is achieved, while enhancing the area efficiency than the existing design of flip-flop.

VI. CONCLUSION

The proposed SRAM circuit design with hetero junction CMOS technology provides better performance than the existing SRAM circuit design. Hence, the design of the SRAM is simplified by using the hetero junction CMOS, to achieve high area efficiency. Significant reduction in the power consumption and noise level of the SRAM is achieved. The simulation result shows that the leakage power obtained in the proposed circuit is 127 mV. Therefore, the leakage power of the proposed SRAM circuit is less than the conventional circuit. The accuracy of the proposed circuit is higher than the conventional circuit. Hence it implies that the proposed circuit is more efficient than the existing SRAM circuit. The reduction of noise in the read port and delay is achieved, while enhancing the area efficiency than the existing design of flip-flop.

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