Implementation of multiple bit carry look ahead adder using verilog platform

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Abstract- In VLSI design adders are the most critical components and attention should be focused in designing them.This paper deals with implementing carry look ahead adder with 4bits,8bits,16bits,32bits,64bits and 128bits using verilog platform.The designed carry look ahead adders are simulated using multisim 5.7g and the sum generation and carry propagation are recorded.It is observer that the designed carry look ahead adders performance is better when compared with traditional carry look ahead adder.

Keywords-Verilog platform, modelsim5.7g, XilinxISE 10.1,carry look ahead adder(CLA),addition.

INTRODUCTION:

Addition is a fundamental arithmetic operation used in VLSI design systems like data process unit,microprocessor and DSP architecture.Adders are the most shortest parth circuits used for the execution of addition.Adders like carry save adder(CSA),carry select adder,carry skip adder(CSK),ripple carry adder(RCA),carry look ahead adder (CLA) etc., contributes good attributes and some drawbacks.

A.Carry save adder:

CSA is a kind of adder with low propagation delay, instead of adding two input numbers to a single sum output, it adds three input of numbers to an output pair of numbers.When two outputs are then summed by a traditional carry look ahead (or) ripple carry adder, we received the sum of all three inputs. The propagation delay of a CSA is not affected by the width of vectors being added.Each full adders output 'S' is connected to corresponding output bit of one output , and its output Cout is connected to the next higher output bit of the second output. The lowest bit of the second output is fed directly from the carry - saves C input.

B.Carry select adder:

The simplest n-bit carry select adder is built using three n/2 bit ripple carry adders.The lower half of n-bit sum is computed using the first adder, while the other two compute the higher half : one based on the postulation that the input carry is zero , the other based on the postulation that it is one. In this way the computation of the higher half can start without delay. When the lower half of the sum is computed and the carry input for the next stage is accessible , the correct half of the sum is selected by a multiplexer.The required area and power consumption of this adder particularly doubles with respect to RCA because of the simulation technique.

C.Carry skip adder:

CSK is a creative adder with a minimum of additional logic.The n-bit adder is divided into 'k' ripple-carry adder blocks.A group propagate signal is given to each adder block meaning when this signal is one , an incoming carry cannot be engaged and will propagate through the adder block as an alternativeby skipping the adder segment through the skip logic.Different performance in terms of delay , and power and area for same length of binary numbers can be performed using these adders.

D.Ripple carry adder:

Several full adders connected in series constitutes a ripple carry adder.The carry is propagated through every full adder before the addition is completed.Each full adder inputs a Cin , which is the Cout of previous adder.Since, each carry ripples to the next full adder , this kind of adder is known

as ripple carry adder.RCA requires the least amount of hardware of all adders , but they are the slowest.

E.Carry-lookahead adder:

Carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits.It can be contrasted with simpler but usually slower , ripple carry adder for which the carry bit is calculated alongside the sum bit , and each bit must wait until the previous bit has been calculated.The carry-lookahead adder calculates one or more carry bits before the sum , which reduces the wait time to calculate the result of the larger value bits.CLA depends on two things;Calculating for each digit position , whether that position is going to propagate a carry if one comes.This paper is structuredas follows : section (II) provides a review about CLA adder , logical diagram , function and equation.section (III) focuses on the verilog platform.section (IV) provides the design of multiple bits of CLA.section (V) provides the conclusion.

II.REVIEW OF CARRY-LOOKAHEAD ADDER:

Carry look ahead logic uses the concepts of generate and propagate carry. In the context of a carry lookahead adder, it generate and propagate a binary addition. There will be a carry propagation if OR operation is performed for that either one of the input is one or input carry also be 1. For carry generation there should be AND operation for that both the inputs should be 1.

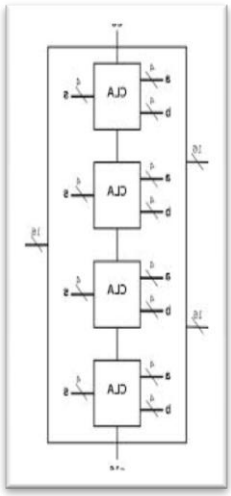

Fig (1): design of multiple bit CLA section

Generate and propagate can be represented by the following Boolean equation:

Pi = xi or yi --Carry Propagation
Gi = xi and yi --Carry Generate
Ci+1 = Gi or (Pi and Ci)--Next Carry

$$Cout = A \bullet B + A \bullet C + B \bullet C$$

$$Cout = \underbrace{A \bullet B}_{\text{Carry Generate}} + \underbrace{(A + B)}_{\text{Carry Propagate}} \bullet C$$

Fig(2): Equations for carry generate and carry propagate

III.VERILOG PLATFORM AND ITS HISTORY:

Verilog standardized as IEEE 1364,is a hardware description language (HDL).It is used to model electronic systems.It is used in the design and verification of digital circuits at the register-transfer level of abstraction and also used in the verification of analog circuits and mixed-signal circuits.Verilog was the first modern (HDL) to be invented.It was invented by Prabhu Goel sbd Phil Moorby .The wording for this process was “Automated Integrated Design Systems”(later renamed to Gateway Design Automation in 1985)as a hardware modeling language. A verilog design consists of a hierarchy modules. Modules encapsulates design hierarchy and communicate with other modules through a set of declared input,output,and bidirectional ports.A module can contain any combination of the following net/variable declarations concurrent and sequential statement blocks,and instances of other modules.Verilog’s concept of ‘wire’ consists of both signal value(4 states: “1,0,floating,undefined” and strengths.

IV.DESIGN OF MULTIPLE BITS CLA:

The figure depicts the implementation of 16 bit carry – lookahead adder using 4 bit CLA.The sum and carry signals are generated.It is very clear there is no propagation delay.

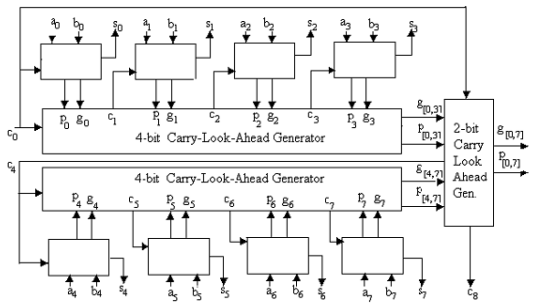

Fig (3): 8 bit CLA using two 4-bit CLA

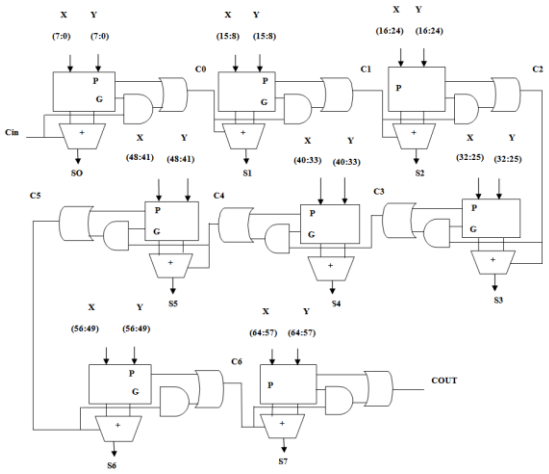

Figure (4):64-bit Carry-lookahead adder

The inputs for this CLA are X and Y.The propagate signals and generate signals are represented as (p) and (g) respectively.Using two 64-bit carry-lookahead adder 128 bit is simulated.

V.IMPLEMENTATION:

Table (1) shows the modified CLA in terms of power.

D	E	F	G	H
On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	72	7168	1
Signals	0.000	106	---	---
IOs	0.000	115	141	82
Leakage	0.060			
Total	0.060			

VI.CONCLUSION:

Multiple bits carry lookahead adder is implemented successfully using Xilinx ISE10.1 and Multisim 5.7g on verilog platform.It is observed that with increasing bits, the speed of the adder is doubled.With respect to bit size the CLA has fastest growing area and power consumption.Using verilog platform other kinds of adders can be implemented.

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