Implementation of 16-Bit Area Efficient Ling Carry Select Adder

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***Abstract*–Parallel Prefix Adders plays a prominent role in Digital Combinational Circuits. The basic function of Adder in Arithmetic and Logical Unit (ALU) is an addition. It is also used in Multipliers which results in decrease or increase of Delay that depends on the architecture of adder. Area and power are other factors which really makes the adder effective. The high-performance digital adder with reduced area and low power consumption is an important design constraint for modern advanced processors. So, low power adders are also a need for today's VLSI industry. This paper focuses on the operation of parallel Prefix Adders of 16bit Brent-kung and Ling adder**.

Key words*: *Parallel prefix adder, Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Carry Look Ahead (CLA) Brent-Kung (BK), Ling adders (LA).

I. INTRODUCTION

The Design of area efficient and high-speed logic systems is the very important aspect in the Very Large Scale Integrated Circuits (VLSI). The operation of an adder is limited by the carry propagation signal because the generation of a carry signal requires a more amount of time when compared with the summation output. Adder is a digital circuit which performs addition of numbers. The Addition is one of the basic need for performing a multiplication, subtraction, and division. So, all these operations are based on the addition only. Hence, it is an integral part of ALU. Adders are found in most of the microprocessor and digital signal processing chips and these are the basic building block of the subtraction, multiplication, and division. The amount of delay can be calculated by the resident adders and these affect the performance of the circuit. The performance of the digital circuits is based on the area, power consumption, and amount of delay it acquired. However most of the circuits are designed based upon the low power and fewer delay techniques.

Parallel prefix adders are one of the most important techniques to reduce area and delay of the circuit.. Designing of more accurate and high-speed adder is called the carry select adder (CSLA).

In array processing multiplication, division, and multi-operand adder plays an important role. The design of more accurate and high-speed multi-operand adder is called the Carry Select Adder (CSLA). The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (MUX).

In CSLA architecture output is calculated for both the carries i.e.., for Cin=0 and for Cin=1. Based upon the previous group carry output one of the carry branch can be selected and the summation output is selected with the help of Multiplexer at the bottom of the architecture. The conventional carry select adder [1] [14] is having two Ripple Carry Adders (RCA) one for C_{in}=0 and another one for C_{in}=1. An RCA is turned into a Carry Select Adder by saving the carry instead of propagates. Due to the presence of two RCA's area occupied by the conventional carry select adder is more [3] [14], so to avoid the area inefficient problem in the CSLA architecture the RCA's are replaced with the Brent-Kung and Ling Adder (LA). Transistor count and the amount of delay are also increased in the proposed architecture.

In the proposed adder one of the RCA i.e.., RCA with C_{in}=0 is replaced with a Brent-Kung and Ling adder (LA) to reduce the delay and area [11]. The summation output and the final carry output will be available within less amount of time and obviously this is one of the basic needs for a digital circuit.

Organization of this paper is as follows: Section II describes the proposed methodologies of CSLA using Brent-Kung and Ling Adder. Section

III gives the area and delay evaluation [8] of 16-Bit regular Linear Brent-Kung and Ling Carry Select Adder. Section IV explains the simulation results of the adder and the comparison results of both. The paper is concluded in Section V.

II. PROPOSED METHODOLOGY.

A. Regular Linear Carry Select Adder of 16-Bit Brent Kung Adder

Brent Kung [2] adder is one of the parallel prefix adders. Its architecture gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. Parallel prefix adders are one of the unique adders that work on the propagating and generating signals. Cost and wiring complexity of the Brent Kung adder is less. But the gate level depth of Brent-Kung adders [10] is 0 (log2 (n)), so the speed is lower. The regular linear CSLA of 16-Bit BK adder is shown in fig1

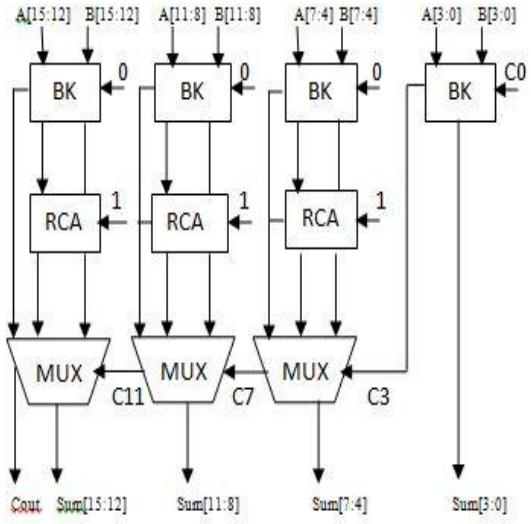

Fig. 1.Block Diagram of 16-Bit Brent-Kung Ling Carry Select Adder

Regular linear CSLA of 16-bit BK adder has one RCA, BK and a MUX. When compared with the conventional CSLA [14] one RCA is replaced with BK for C_{in}=0, hence delay [13] will be reduced. The RCA requires a more no of transistors for the implementation of the adder logic i.e.., if the bit size is increases the no of full adders are increases proportionally. But in the BK adder it requires a less no of logic gates to implement the same logic, hence the BK adder as less delay and more area efficient. The BK adder follows the tree structure form to increase the speed

B. LING ADDER (LA)

Ling Adder is one of the special kinds of a Carry look Ahead adder [15]. In this adder, an Ex-or gate is replaced with an OR gate to perform the operations easily and this approach is faster and less expensive. In this adder, it generates a simplified group of a function called a pseudo carry. The first level of carry computation stage is simple and it is easily obtained by the factorization of one not kill bit from the group function, and the remaining carry computation logic is similar to the conventional parallel prefix adder. The not kill term is combined with the remaining computation logic before the outcome of summation at the end. As this process involves less delay because of a multiplexer instead of an XOR gate to compute the sum, the adder becomes a one of the fastest adders in the parallel prefix adders.

C. Regular Linear Carry Select Adder of 16-Bit Ling Adder

Regular Linear Carry Select Adder [6] has dual RCA's one for C_{in}=0 and other for C_{in}=1. The Ling adder has less area and requires low power consumption when compared with RCA. Hence, the RCA with C_{in}=0 replaces with Ling Adder for C_{in}=0. So, regular linear Ling CSLA is designed using Ling adder. The linear Ling CSLA has a Ling adder for C_{in}=0 and for c_{in}=1 RCA are placed normally as in the linear regular CSLA. It has four groups of the same size. Each group consists of one Ling adder and one Ripple carries adder for different carries. To increase the speed of arithmetic operation here we are using the tree form structure. The block diagram of Regular linear Ling CSLA is shown in Figure. 2.

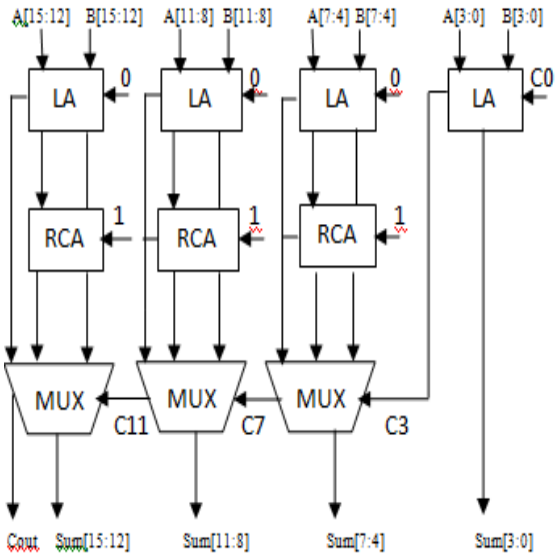

Fig. 2.Block Diagram of 16-Bit Linear Ling Carry Select Adder

In group2, the Linear Ling Adder CSLA has

single Ling adder for C_{in}=0 and single RCA for C_{in}=1. Based upon the Carry of group1 the Ling Adder with Cin=0 or RCA with Cin=1 is selected and the 4-Bit summation output is taken from the multiplexer present at the bottom of the architecture of Linear Ling CSLA [7]. If the carry is 1 then the output of RCA with C_{in}=1 is selected using the MUX. A 4-bit sum [7:4] and an output carry is obtained at the output of group2.

III. AREA & DELAY EVALUATIONS

A. REGULAR 16-BIT LINEAR BRENT-KUNG ADDER

The 16-bit regular linear CSLA BK adder has 4 groups. Group1 contains a single BK adder and the remaining groups contains a single BK adder for C_{in}=0, a RCA for C_{in}=1 and a MUX. The area and delay evaluation of a 16-bit Regular linear CSLA BK adder is estimates as follows:

1. Group1 contains a four bit BK adder the delay for the S(0), S(1), S(2), S(3) and carry output c(3) are 3 units, 6 units, 8 units,10 units and 9units respectively. Area occupied by these summation and carry outputs are 3 units, 7 units, 9 units, 9 units and 3 units respectively. So, total delay and area occupied in group1 is 10 units and 48 units.
2. Group2 contains a four bit BK adder the delay and area for them is same as group1. The group2 also contains a RCA. The four bit RCA as four Full adders and the area and delay occupied by the four bit RCA is 52 units and 12 units. So, total delay and area occupied in group2 is 14 units and 110 units.
3. Group3 and Group4 contains a one BK adder and one RCA hence the area occupied by both the groups are same as group2 but the delay will be varied from group2 to group8 with increasing of 3 units from the previous groups

Depending upon the And-Or-Inverter (AOI) [7] [8] Logic the area and delay evaluations of any logic can be calculated and the delay of the logic gates in any circuit can be calculated as shown in the below figure 3.

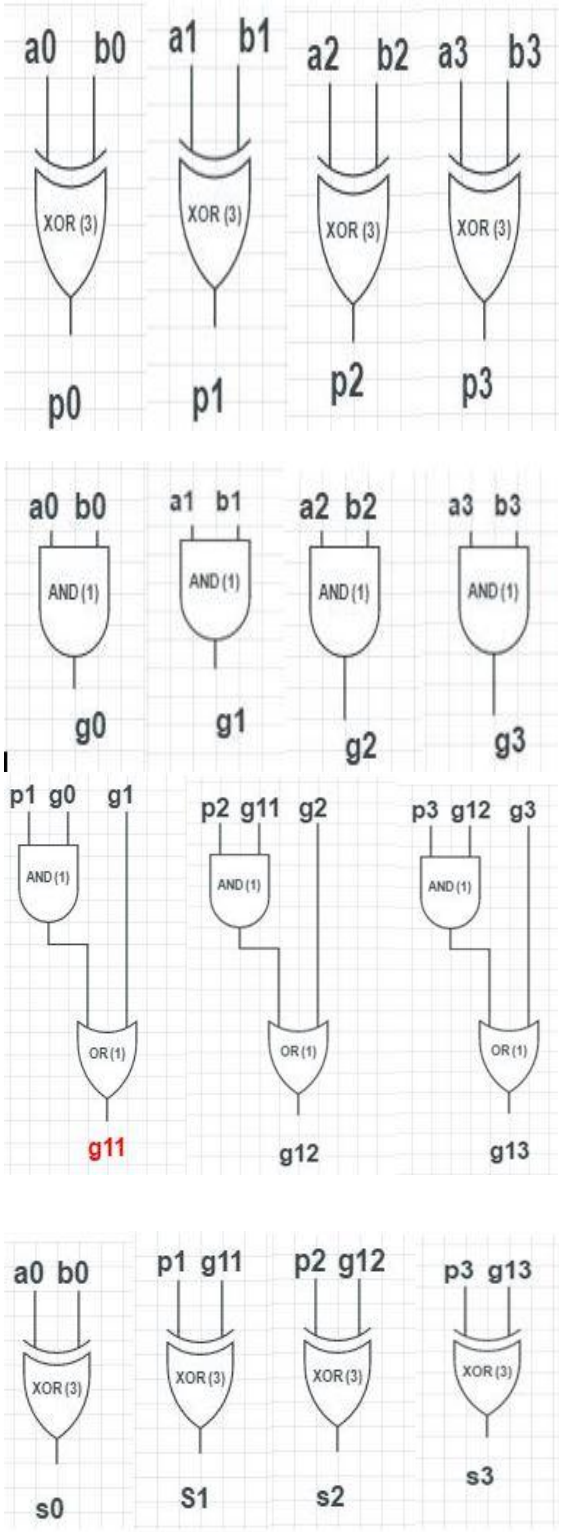

Fig 3. Pictorial representation of delay evaluations of BK adder

The Calculation of the final Sum and Carries for Brent-Kung Adder is shown in the above figure 3. The number in the gate represents the delay correspond to the gate depend on the delay of the gates the total theoretical delay and area for 16-Bit

regular Linear CSLA Brent-Kung adder is calculated and it was shown in the below Table. I.

TABLE I Theoretical AREA and DELAY EVALUATION

Group	Delay	Area
1	10	48
2	15	110
3	18	110
4	21	110

From the above Table I it is observed that the area is less consumed when compared with the Conventional Carry Select Adder [3] [14].

B. REGULAR LINEAR 16-BIT LING CARRY SELECT ADDER.

The 16-bit regular linear CSLA LA adder has 4 groups. Group1 contains a single LA adder and the remaining groups contain a single LA adder for C_{in}=0, an RCA for C_{in}=1 and an MUX. The area and delay evaluation of a 16-bit Regular linear CSLA LA adder is estimated as follows:

1. Group1 contains a four bit LA adder the delay for the S(0), S(1), S(2), S(3) and carry output c(3) are 3 units, 7 units, 7 units,7 units and 7 units respectively. The area occupied by these summation and carry outputs are 3 units, 11 units, 11 units, 11 units and 10 units respectively. So, total delay and area occupied in group1 is 7 units and 46 units.
2. Group2 contains a four bit LA adder the delay and area for them are same as group1. The group2 also contains an RCA. The four bit RCA as four Full adders and the area and delay occupied by the four bit RCA is 52 units and 12 units. So, total delay and area occupied in group2 is 14 units and 98 units.
3. Group3 and Group4 contains a one LA adder and one RCA hence the area occupied by both the groups are same as group2 but the delay will be varied from group2 to group8 with increasing of 3 units from the previous groups.

Depending upon the And-Or-Inverter (AOI) [7] [8] Logic the area and delay evaluations of any logic can be calculated and the delay of the logic gates in any circuit can be calculated as shown in the below figures 4.

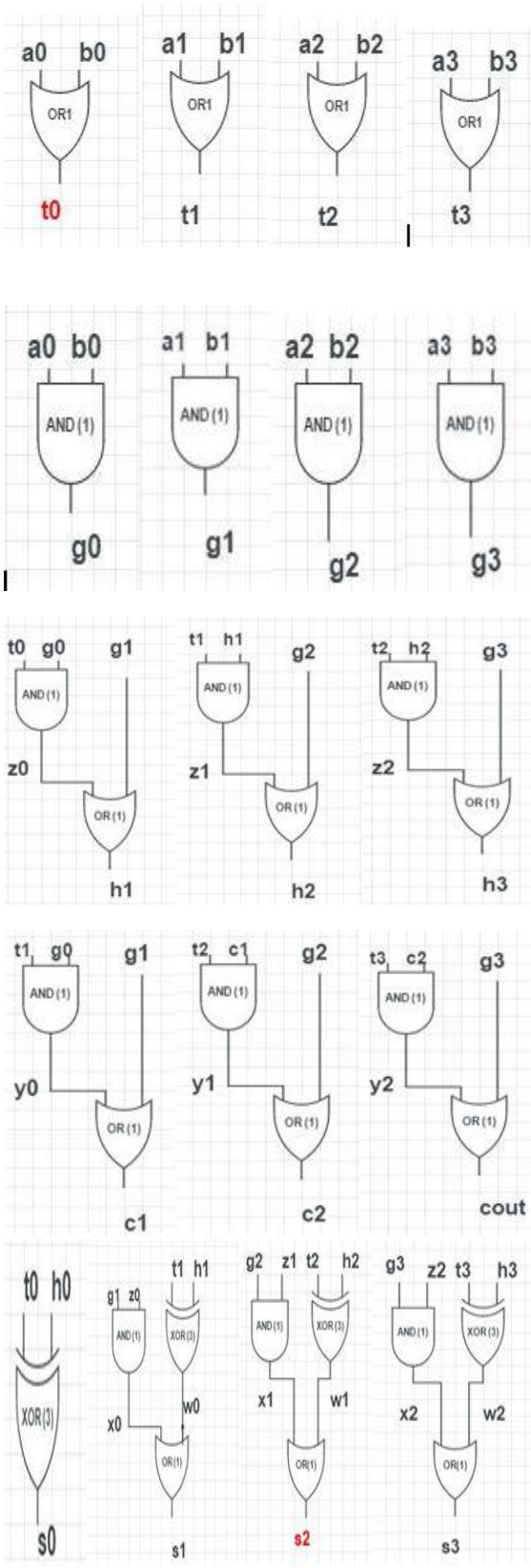

Fig 4. Pictorial representation of delay evaluations for Limg adder

The Calculation of the final Sum and Carries for Ling Adder is shown in the above figures 4. The number in the gate represents the delay correspond to the gate depend on the delay of the gates the delay will be calculated and the total theoretical delay and area for 16-Bit regular Linear CSLA Ling adder is calculated and it was shown in the below Table. II

TABLE II Theoretical AREA and DELAY EVALUATION

Group	Delay	Area
1	7	41
2	14	108
3	17	108
4	20	108

From the above Table II it is observed that the area is less consumed when compared with the Brent-Kung adder and Conventional Carry Select Adder [3] [14]. Hence, the Ling Adder is the Area efficient Carry Select adder obviously it is one of the main aims in the digital circuitry.

TABLE III Practical AREA and DELAY EVALUATIONS

Design Utilizations	Brent-Kung Adder	Ling Adder
Slices	22	13
Four Input LUT's	40	24
Bounded IOB's	49	42

The above Table.III gives the design utilization summary for both the regular linear 16-bit Brent-Kung and Ling adder architectures.

IV. SIMULATION RESULTS.

The results of Brent-Kung adder are simulated by using the Xilinx software. The simulated results of 16-Bit Linear Brent-kung CSLA are shown in Figure 3.

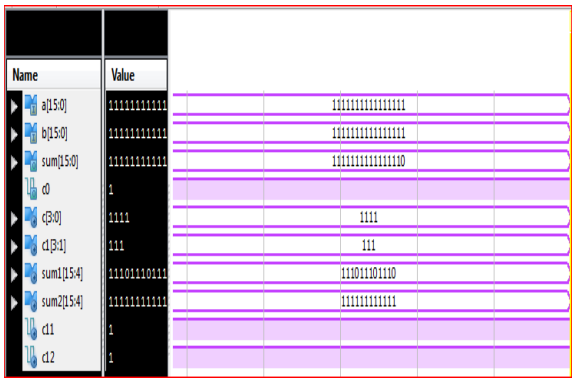

Fig.3. Simulation results for Linear BK Carry Select Adder

The results of Ling adder are simulated by using the Xilinx software. The simulated results of 16-Bit Linear Ling CSLA are shown in Figure 4.

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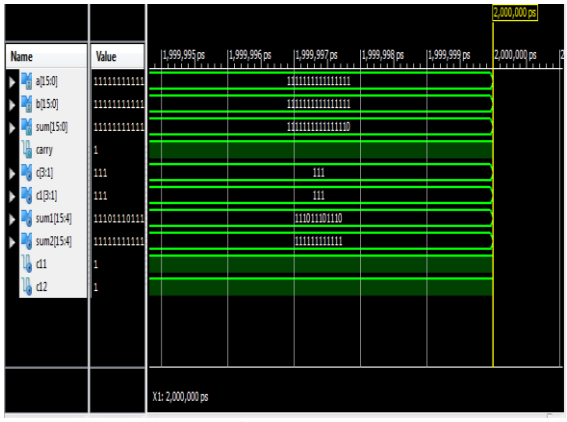

Fig.4. Simulation results for Linear Ling Carry Select Adder.

The area occupied by the 16-Bit Ling Carry Select Adder is less when compared with the 16-Bit Brent-Kung Adder architectures and this was shown in the following figure 5. The graph was drawn based on the theoretical calculations of the Ling and Brent-Kung adders. The x-axis shows the name of the individual group and y-axis shows the no of logic gates occupied by the adders in each group.

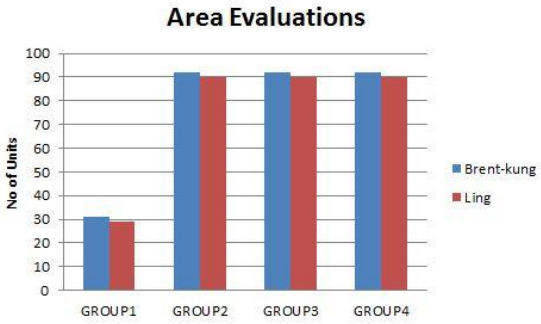

Fig 5.Area comparison of Brent-Kung and Ling adders (Theoretical)

Comparison of areas for both the 16-Bit adder architectures depend upon the design utilities is shown in the below figure 6. The graph drawn based on the no of utilities occupied by an each adder and the graph in figure 6 is drawn based on the practical calculations by using Xilinx software.

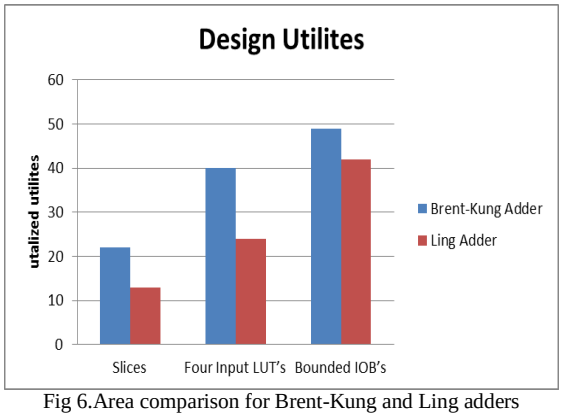

Fig 6.Area comparison for Brent-Kung and Ling adders (Practical)

V.CONCLUSION

In this wok, a Linear Brent-Kung and Ling Carry Select Adder is proposed which contains a Brent-kung, Ling Adder along with Ripple Carry Adder (RCA). When compared with the Brent-Kung adder the 16-Bit Linear Ling Adder is area efficient [8] [3]. Simulation and synthesis are carried on Xilinx ISE 12.2 on an INTEL core2 (TM). The present work can be further extended by implementing SQRT CSLA and its simulation results can be compared in the aspect of bit size, workload and delay time.

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