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Implementation Of 64-Bit Sqrt Carry Select Adder Using Bec-1

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ABSTRACT:

In VLSI design a largest area of research is based on design of area,high speed processing and efficient data logic paths. A good compromise between the cost and carry propogation can be deemed by a carry select method.To perform fast arithmetic operations we go in for carry select adders which is considered as a fastest adders. CSLA has a scope to reduce the area and delay because of its structure. The area and delay can be reduced by designing a CSLA model based on gate level modification(in regular structures). The regular SQRT CSLA is compared with the modified square root CSLA structure with 16,32,64 and 128 bits. The comparison proved that the proposed structure of CSLA has reduced the area and delay to a great extent than that of the regular SQRT CSLA model.this work of proposed CSLA model concludes that its performance is far better and efficient than a regular SQRT CSLA model interms of delay and area consumption.

Keywords: *Binary to Excess -1 converter (BEC), Common Boolean Logic (CBL), Area efficient, SQRTCSLA (square root carry select adder).*

I.INTRODUCTION:

The main area of research in VLSI design is to propose a system with reduced area and high speed data path logic.High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The time required to propagate a carry through the adder has limited the speed of addition in digital adders. The previous bit position are added and a carry is propagated into the next position and then it is sequentially generated in a elementary adder for the sum of each bit position.The production of carry is considered as a major limitation of any adders and many authors considered the addition problem.Inorder

To overcome these limitations CSLA has been developed that reduces the area and delay to a greater extent.

By considering the carry input,the csla is sum and carry.the multiplexer selects the final sum and carry. The area will increase due to the use of two independent RCA, which leads an increase in delay. To BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates used will be decreased.

Inorder to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. To generate the resultant sum it uses independent ripple carry adders (for Cin=0 and Cin=1). However, the regular CSLA is not area and speed efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input. This logic can be replaced in RCA for Cin=1 to further improves the speed and thus reduces the delay. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area, delay swhich speeds up the addition operation. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure because the number of gates will be decreased.

II. PRIMARY ADDER BLOCK

In this section the adder block using a Ripple carry adder, BEC and Mux is explained. We calculate and explain the delay & area using the theoretical approach and show how the delay and area effect the total implementation. The

AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. All gates are made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit which is shown by the delay and area estimation methodology. In the longest path of a logic block we then add up the number of gates that contributes to the maximum delay. By counting the total number of AOI gates required for each logic block the area evalution is done. Based on this approach, the blocks of 2:1 mux, Half Adder (HA), and FA are evaluated.

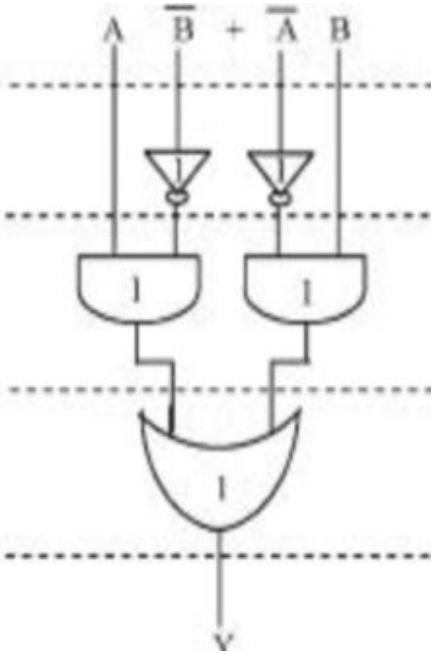

Fig 1: Delay and area evalution of xor

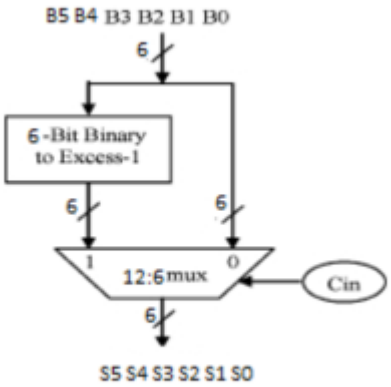

Fig 2: 6-bit BEC with 12:6 mux

Fig 2 shows the basic 6-bit addition operation.The addition operation is performed for Cin=0 and for Cin=1.By using ripple carry adder Cin=0 addition is performed and for Cin=1 the operation is performed using 6-bit BEC by replacing RCA.Based on Carry in signal from the previous group,the resultant is selected. The mux delay and Cin signal from previous group both add up to give the total delay.

III. BINARY TO EXCESS-1 CONVERTERS:

To achieve lower area and increased speed of operation we can use Binary to excess-1 in the regular CSLA. By giving Cin=1 this logic is replaced in RCA. This logic can be implemented for different bits which are used in the modified design. It uses lesser number of logic gates than the n-bit Full Adder (FA) structure which is considered as one of its main advantage. As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. An n+1 bit BEC logic is required to replace the n-bit RCA. The structure and the function table of a 6-bit BEC are shown:

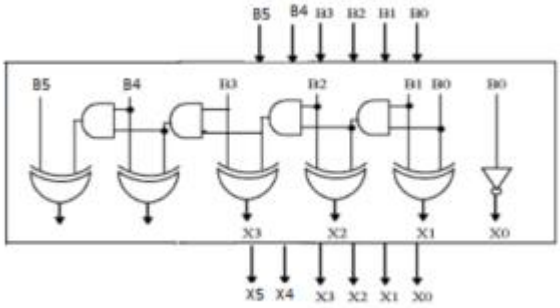

Figure 2: 6-BEC-1 convertor

IV. REGULAR 64-BIT SQRT CSLA MODEL:

A 16-bit carry select adder can be developed in two different sizes namely uniform block size and variable block size.

In two modes of different block sizes we can also develop a 32,64 and 128 bits correspondingly. Ripple-carry adders performance are limited by a carry that must propogate from the least significant bit to most significant bit. It is although considered as the simplest and most compact full adders. It can be used to develop various 16, 32, 64 and 128-bit CSLA.By performing parallel additions and decreasing the maximum carry delay the speed of carry-select adder can be improved upto 40% to 90%.

Fig 3 shows the structure of 64-bit SQRT CSLA. The structure includes many ripple

carry adders that are divided into groups of variable sizes. The 2-bit RCA belonging to group 0 which contains only one ripple carry adder which adds the input bits and the input carry and results to sum [1:0] and the carry out. The Group 0 produces carry out which acts as the selection input to group 1 mux, it selects the result from the corresponding RCA(Cin=0) or RCA (Cin=1). Similarly the remaining groups will be selected depending on the Cout from the previous groups.

The Regular CSLA contains only one RCA to perform the addition of the least significant bits [1:0].The addition is performed by using two RCAs by assuming a carry-in of 0,the other a carry in of 1 within a group for all remaining bits other than LSB's. The same data inputs but differening Cin is received in a group by two RCA's. A carry-in of 0 can be obtained from the upper adder, and the lower adder produces a carry-in of 1. The obtained Cin from the previous section selects one of the two RCAs.The carry-in is 0, the sum and carry-out of the upper RCA is selected, and if the carry-in is 1, the sum and carry-out of the lower RCA is selected.

For this Regular CSLA model, the implementation code, for the Full Adders and Multiplexers of different sizes (6:3, 8:4, 10:5 up to 24:11) were designed initially. The regular 64-bit, 128-bit CSLA were implemented by calling the ripple carry adder and multiplexers.

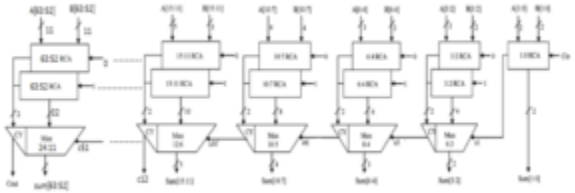

Figure 3: Regular 64-bit SQRT CSL Model

V.PROPOSED MODEL OF 64-BIT SQRT CSLA :

This model is similar to regular 64-bit SQRT CSLA but the difference is that we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC can perform similar operations as that of the replaced RCA.Fig 4 shows the Proposed model of 64-bit SQRT CSLA.The BEC logic requires a number of bits that is is 1 bit more than the RCA bits. The proposed model is divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux.The Group 0 contain only one RCA with input of lower significant bit and carry in bit and produces result of sum[1:0] and carry out which acts as a mux selection line for the following group, and the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival time of selection input C1 of 8:3 mux is earlier than the sum of RCA and BEC. The selection input arrival is later for RCA and BEC in remaining groups. Thus, then the mux outputs sum1 and c1 depends on mux and it produces results computed by RCA and BEC respectively. The sum2 depends on c1 and mux.The delay of the MUX depends on the arrival time of mux selection input and the mux delay.

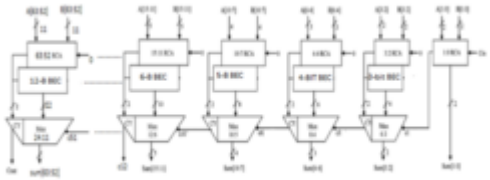

Figure 4: Proposed Model Of Modified 64-bit SQRT CSLA

Name	Power (W)	Used	Total Available	Utilization (%)
Logic	0.000	3	7168	0.0
Signals	0.000	7	--	--
IOs	0.000	86	141	61.0
Total Quiescent Power	0.056			
Total Dynamic Power	0.000			
Total Power	0.056			

Fig 5:Power report

VI.RESULTS

The Verilog-HDL (Modelsim) can be used to stimulate this design and its results can be implemented. The adders of various sizes can be designed and simulated using verilog-HDL(ModelSim). All the V files classified as regular modified are also simulated in Modelsim and results are compared.By using Xilinx ISE 9.1i different size codes are synthesized after simulation. The synthesized tool imports the simulated V files and note the produced area and delay values.For different sized adders the area and delay can ba calculated.The design low is similar both for regular and modified model of different sizes.

Final Results:

Final Report

RTL Top Level Output

File Name :sqrtcsla64.ngr

Top Level Output

File Name :sqrtcsla64
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics
IOs : 3392

Cell Usage :
BELS : 5
GND : 1
LUT3 : 1
LUT4 : 2
MUXF5 : 1
IO Buffers : 86
IBUF : 5
OBUF : 81

Device utilization summary:
Selected Device : 3s500efg320-4 Number of Slices: 2 out of 4656 0% Number of 4 input LUTs: 3 out of 9312 0%
Number of IOs: 3392 Number of bonded IOBs: 86 out of 232 37%

Partition Resource Summary:
No Partitions were found in this design.

TIMING REPORT:
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
No clock signals found in this design

Asynchronous Control Signals Information:
No asynchronous control signals found in this design

Timing Summary:
Speed Grade: -4
Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 6.557ns

Timing Detail:
All values displayed in nanoseconds (ns)
Timing constraint: Default path analysis
Total number of paths / destination ports: 12
Delay: 6.557ns (Levels of Logic = 4)
Source: a0<1> (PAD)
Destination: y175<1> (PAD)
Data Path: a0<1> to y175<1>
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
IBUF:I->O 2 1.218 0.622 a0_1_IBUF (a0_1_IBUF)
LUT4:I0->O 1 0.704 0.000 r1/f2/Mxor_s33_xo<0>21 (r1/f2/Mxor_s33_xo<0>2)
MUXF5:I1->O 1 0.321 0.420 r1/f2/Mxor_s33_xo<0>2_f5 (y175_1_OBUF)
OBUF:I->O 3.272 y175_1_OBUF (y175<1>)
Total : 6.557ns (5.515ns logic, 1.042ns route)
(84.1% logic, 15.9% route)
Total REAL time to Xst completion: 23.00 secs
Total CPU time to Xst completion: 23.13 secs
Total memory usage is 201468 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 490 (0 filtered)
Number of infos : 0 (0 filtered)

VIII. CONCLUSION

To reduce the area and delay of SQRT CSLA architecture an efficient model is proposed. By simply replacing the RCA with BEC in the structure the number of gates used can be reduced to a great extent . The compared results shows that the modified SQRT CSLA has a slightly larger area for lower order bits which further reduces for higher order bits. The modified SQRT CSLA has reduced the delay to a greater extent.

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