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High Speed Vlsi Architecture For 1024 Bit Carry Select Adder

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***Abstract*— The basic building blocks of any processor are an adder. But carry generation is difficult in the design of adders. Power dissipation is one of the most important design objectives in integrated circuits, after speed. As adders are the most widely used components in such circuits, design of efficient adder is of much concern for researchers.. In order to reduce the power consumption of a processor we need to reduce number of transistors of the adder. Carry Select Adder is one of the fast adders used in many processors. There is a chance to reduce the area, power and delay in the CSLA structure. The proposed design is implemented by using D-latch along with RCA cascade structure. This paper also presents performance analysis of carry select Adders. The comparison between RCA used CSLA and carry look ahead adder used CSLA is done on the basis of three performance parameters i.e. Area, Speed and Power consumption. We present a modified carry select adder designed in different stages. Results obtained from modified carry select adders are better in area and power consumption.**

Index terms –D Latches, multiplexers, ripple carry adder, carry select adder, power consumption, time delay.

I. INTRODUCTION

In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [2].

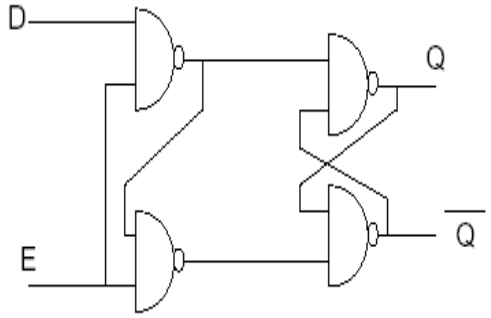


fig.1.1-D latch

However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1. The basic idea of this work is to use D-Latch instead of RCA with Cin = 0 or cin = 1 anyone in the regular CSLA to achieve High speed, lower area and power consumption [5]-[6]. The main advantage of this D-Latch logic comes from High Speed than the n-bit Full Adder (FA) structure.

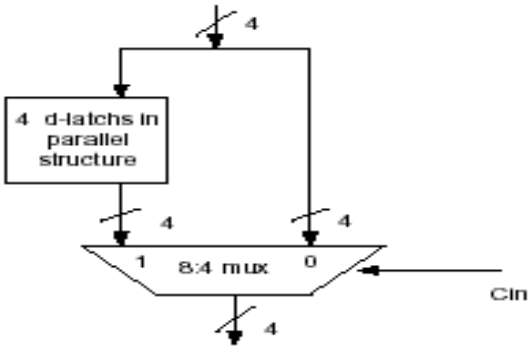


fig.2.internal structure of 4-D latch with multiplexer

Fig.1 shows the internal structure of D-Latch when D-Latch en=1 the input to the d-latch pass transistor should be D and when en=0 the input to the pass transistor should be value of D just before the transition of clock from 1 to 0.To obtain the value of D just before transition a buffer is needed. Fig.2 shows the internal structure of 4-bit D-Latch circuit. When en=1 then the RCA structure will calculate the output for cin=1 and that will be stored in D-Latch.

When en=0 then the RCA structure will calculate the output for cin=0 and the D-Latch out will not change that will stores previous value of RCA when en=1. And that D-latch, RCA structure outputs are given to the multiplexer by using selection line (cin) it will gives the proper output.

II. RELATED WORK

Sajesh Kumar U, Mohamed Salih K. and Sajith K 2012 propose carry select adder without using multiplexer which reduce area and power consumption.[4]

Bedriji 1962 proposes that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums.[2]

Youngwood Kim and Lee Sup Kim 2001 introduces a multiplexer based add one circuit is proposed to reduce the area with negligible speed penalty.

Yajuan He at 2005 proposed an area efficient square root carry select adder scheme based on a new first zero detection logic.

AkhilashTyagi 1993 introduces a scheme to generate carry bits with block carry in 1 from the carries of a block with block carry in 0.

Chang and Hsiao 1998 propose that instead of using dual carry ripple adder a carry select adder scheme using an add one circuit to replace one carry ripple adder. [3]

Ramkumar and Harish 2012 propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

Naldurg amd Kravets proposed the Security-Aware Ad-hoc Routing (SAR) which deploys a generalized framework for any on-demand secure ad-hoc routing protocol. It uses security information to dynamically control the routing selection process according to routing tables. Nodes at the same trust level must share a secret key.

III. REGULAR 16-B SQRT CSLA

CSLA compromise between ripple carry adder and carry look ahead adder. When compared to RCA, CSLA is high speed and when compared to carry look ahead adder hardware complexity less. The main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The Fig.4 shows the regular 16-bit carry select adder. It is divided into five groups with different bit size RCA. From the structure of CSLA, it is evident that there is scope for reducing area, power and delay in CSLA. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer. Internal structure of the group 2 to 5 of regular 16- bit CSLA is shown Fig.3. One input to the multiplexer goes from the RCA with Cin=0 and other input from the RCA with Cin=1. There is a chance to reduce the area, power and delay in the CSLA structure.

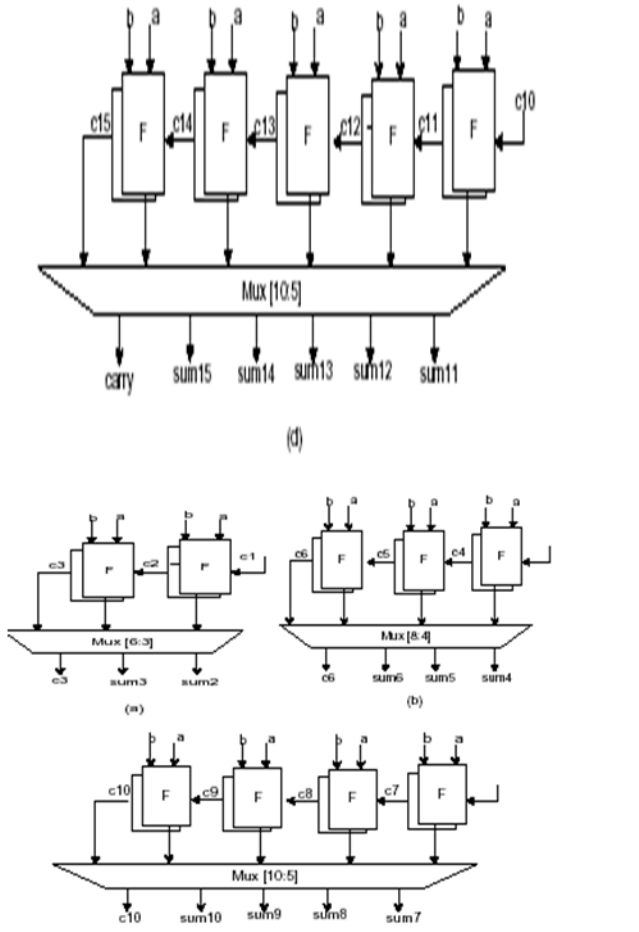


fig.3.internal structure of regular CSLA (group a to d)

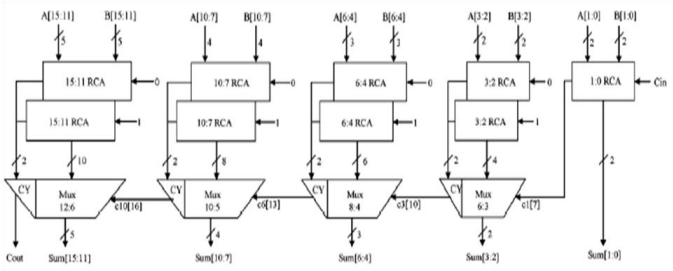


fig 4. 16-bit regular CSLA

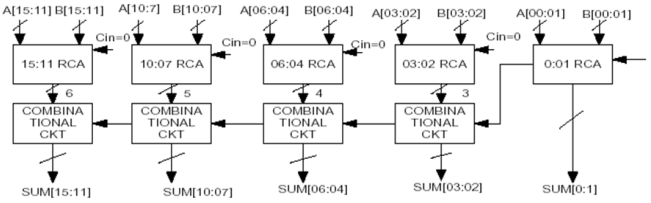


fig 5. 16 bit CSLA without using MUX

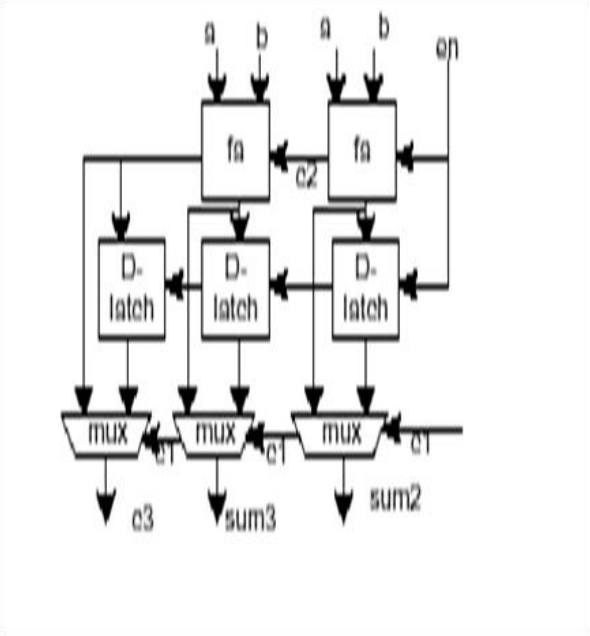
IV. MODIFIED 16-B SQRT CSLA(WITHOUT USING MUX)

In this method CSLA with cin=1 and multiplexer is replaced by the simple combinational circuit which consists of XOR and AND gates. By using this method area and power is reduced when compared to regular CSLA and modified CSLA(BEC). The modified 16-bit CSLA without using mux is shown in fig.5 REF[4]. The structure is again divided into five groups with different bit size RCA and Combinational. Initially RCA structure is calculate for cin =0 the output of full adder is given to the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using Xor and And gates structure. The group 2to 5 of the modified 16-bit CSLA is shown Fig. 5.Comparing the group 2 to 5 of regular, modified BEC and WITHOUT MUX CSLA, it is clear that in this structure area and power is reduced. But the disadvantage of WITHOUT MUX method is that the delay is increasing than the regular CSLA.

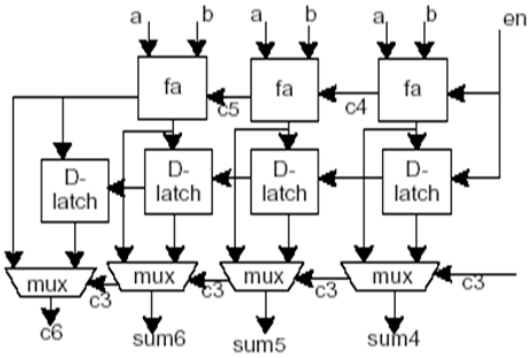
V. PROPOSED CSLA USING DLATCH

In this method replace any one of the RCA structure (i.e. cin =1 or cin =0) by parallel structure of D-latches. For n bit RCA structure it required n D-latches with enable pin as a clk. Latches are used to store one bit information. The RCA structure cin is replace by enable pin, where enable signal is clk signal. When enable pin en =1 then the RCA structure is calculate for cin=1 that result is stored in D-latch. When en =0 then it will calculate for cin =0 and the D-latch output and full adder output is given to the mux. By using selection line it will gives the proper output. Where the enable time period for '1' is very less when compared to the enable pin '0'. Initially RCA structure will calculate for en=1 and then en =0. The architecture of proposed 16-b CSLA is shown in Fig. 7. It has different five groups of different bit size RCA and D-Latch. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock.

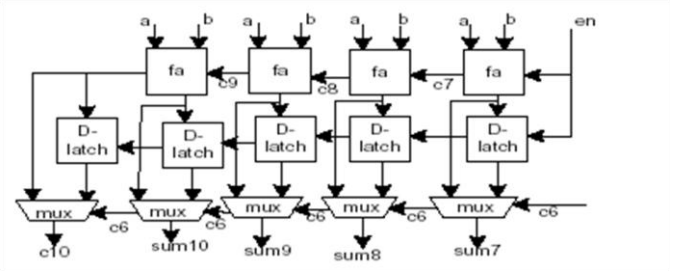
Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. 6, it can understand that latch is used to store the sum and carry for Cin=1. Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder.If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry. The Fig.6 shows the internal structure of group 2 to 5 of the proposed 16-bit CSLA.



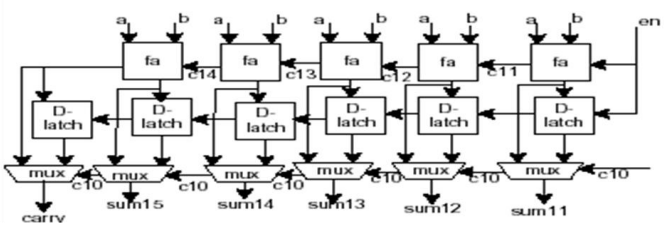
(a)internal structure of 3-D latch



(b)internal structure of 4-D latch



(c)internal structure of 5-D latch



(d)internal structure of 6D-latch

fig 6. internal structures of proposed structure of CSLA

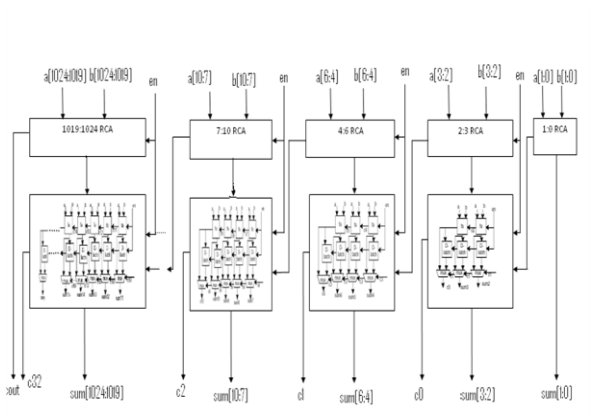


fig7. Proposed CSLA using D latch

VI.SIMULATION RESULTS

The design proposed in this paper has been developed using Verilog-HDL and synthesized the power and timing report in fig.7. The comparison between carry select adder using RCA and Look ahead adder is made based on the power and delay obtained as in table 1.

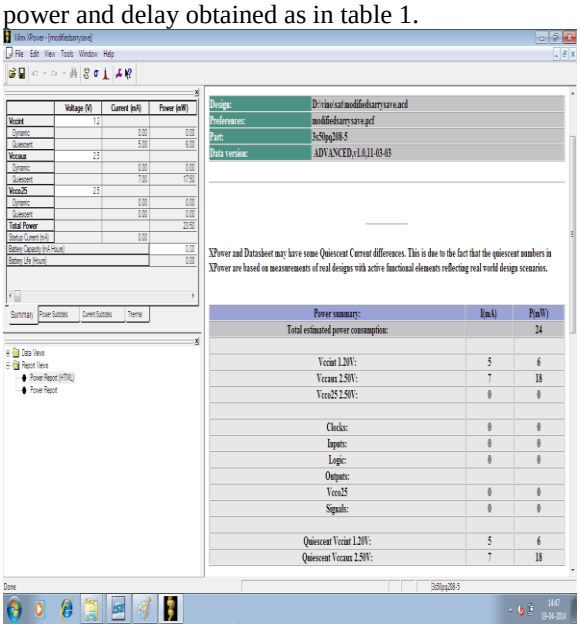


Fig.7.power report for 1024 bit CSLA

TABLE.1

TYPE OF ADDER	DELAY(ns)	POWER(W)
CSLA using RCA and D latch -1024 bits	13.514	0.024
Csla using carry look ahead Adder-1024 bits	696.528	4.224

VII. CONCLUSION

A unique approach is proposed in this paper to reduce the power and delay of SQRT CSLA architecture. This paper shows the design of carry select adder implemented by using D-Latch and compared with CSLA using carry look ahead adder.These two adders are implemented on Spartan XC3S500E FPGA device and the performance is compared. Power and Area is calculated by using synopsys RTL tool. This paper having better results when compared to CSA and modified techniques.

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