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High Speed Reconfigurable Fpga Architecture For Multi-Technology Applications

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Abstract: Field-programmable gate arrays (FPGAs) have revolutionized programmable/ reconfigurable digital logic technology. Current FPGA limitation is that the user is limited to strictly electronic designs. Thus they are not suitable for applications that are not purely electronic. While a wide variety of multi-technology devices like photonic information processing devices have been implemented and they are limited to systems built with application-specific devices(ASIC). Though they are well optimized for specific applications, they do not provide flexibility for reconfiguration of hardware. The difficulty of using custom designed multi-technology VLSI components is overcome with the introduction of Multi-Technology FPGA (MT-FPGA) with innovative system architecture. Different multi technology blocks are integrated in the proposed MT-FPGA architecture. Here each logic block in the array consist of a MTB(Multi technology block) and four programmable logic blocks. The cluster is referred as MTLC (Multi technology logic cluster).MTLC can communicate with other MTLCs in the chip via programmable connection blocks, switch blocks and routing channels. The proposed field programmable device will extend the flexibility, rapid prototyping and reusability benefits associated with conventional FPGA technology into photonic and other multi-technology domain. Performance analysis shows that use of soft links between PLBs in the critical path of MTLC speeds up the system.

Keywords: Application Specific Integrated Circuits (ASICs), Field-Programmable Gate Arrays (FPGAs), multi-technology devices, reconfigurable architecture, Double edge triggered flip flop(DEF).

I. INTRODUCTION

Over the years, Field Programmable Gate Arrays (FPGAs) have made profound impact on the electronics industry. With rapidly improving semiconductor manufacturing technology ranging from sub-micron to deep sub-micron processes and equally innovative CAD tools, FPGAs can be used to solve variety of computing problems. Thus, FPGAs give us the facility to build systems with a set of primitive computational elements interconnected through flexible interconnects. Though FPGAs have made amazing advances in performance and capacity, their use is restricted to electronic designs and thus they have not yet brought the advantages of reprogramming and reconfiguration to multi-technology domain. To get the same advantages in the multi-technology domain, a novel Multi-Technology FPGA(MT-FPGA) has been developed . The development of Multi-technology Field-Programmable Gate array opens a new era for multi-technology applications to use flexibility, rapid prototyping and reusability benefits associated with conventional FPGAs.

For any multi-technology system, a designer can implement the logic parts of a design in the programmable block. The multi-technology components can be incorporated from different multi-technology blocks available in the library. This kind of implementation is similar to a conventional FPGA; the idea is robust and scalable. Further, existing high-level CAD tools can be readily modified to provide a CAD environment that is comparable to existing technology. Designers also get the choice to either implement all the components used in an application in the same block or distribute it among different logic blocks. If the designer chooses to implement different parts of circuit in different bocks then the whole logic can be distributed between various MTBs and appropriate routing channels are used to transfer data from one block to another maintaining the integrity of the signal. The explosive growth in information technology is creating a greater need for optical techniques in data networking and storage, and for new digitally-compatible optical sensors and imaging devices[1]

Development of MT-FPGA will allow designers to implement a whole range of multi-technology functions on a single chip along with their electronic counterparts. There are many applications which can benefit from this hardware such as biochips, where one might have to insert a chip in a living tissue. These chips can be used to analyze the optical signature of biological liquids to detect the presence of certain chemicals . In these kinds of

applications MT-FPGA can serve as a single chip solution. However, applications requiring customized fabrication techniques will not benefit from this architecture. An alternative could be the use of various signal processing arrangements. This architecture would give an advantage of the locality of signal processing units adjacent to the optoelectronic or other technology components.

II. MULTI-TECHNOLOGY FPGA ARCHITECTURE

An earlier version that introduced the design and implementation of a new multi-technology FPGA architecture appear in [2]. MT-FPGA chip includes several Multi-Technology Logic Clusters (MTLCs) connected with a complete routing architecture (i.e., connection blocks, switch blocks, input/output (I/O)blocks, segmented and hierarchical routing channels, etc.) Additionally, this new chip includes the description and testing of a new optical block designed to function as an optical power meter. Fig. 1 illustrates the high-level architecture of the MT-FPGA. To be compatible with the current FPGA design methodology, a symmetrical array of blocks with vertical and horizontal programmable routing channels was adopted in the architecture. Each block in the array consists of a cluster of sub-blocks, viz. a MTB and four programmable logic blocks. This cluster is referred to as a "Multi-Technology Logic Cluster" (MTLC). The MTLCs are the core of the MT-FPGA and are responsible for all the data processing that occurs within the FPGA. The inputs and outputs of the MTLC are connected to the global routing channels around the MTLC in a programmable way by the Connection Block (CB). The connection block receives and sends both analog and digital signals to and from the global routing channels in all four directions i.e. north, south, east and west

III. ARCHITECTURE OVERVIEW OF HIGH SPEED MT-FPGA

We propose an improved version of the MT-FPGA which considerably optimizes speed, area and power when compared to the previous design.

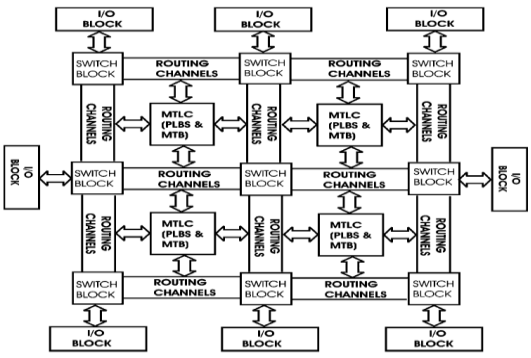

Fig.1. Top level architectural view of an MT-FPGA

A. Multi-Technology Logic Cluster (MTLC)

The MTLC is primarily comprised of four programmable logic blocks (PLBs) in a L3-4.2 tree structure [3] containing hard and soft-connects for speed area optimization. Fig. 2 shows the logical description of a PLB. The principal entity in each of the 4 PLBs is the 4-input Look up table (LUT). Each LUT has a total of 16 programmable components (SRAMs). By programming the SRAMs appropriately, the truth table of any 4 input logic functions can be realized. The 4 inputs to the LUT come from the outputs of four 10-to-1 multiplexers (except when the LUT inputs are hard connected). The inputs to the 10-to-1 multiplexers come from the internal routing channels and other PLB outputs. The use of 10-to-1 multiplexers provides greater connection flexibility between the PLBs and the routing channels. In comparison, the previous generation of the MT-FPGA had 8- to-1 multiplexers connected to the LUT inputs. Each PLB also consists of a user flip-flop which can be used in combination with the LUT for the implementation of sequential circuits. The user flip-flop is driven by two non overlapping clocks and can be reset asynchronously. The MTLC inputs and outputs are connected to the routing channels around the MTLC in a programmable way using Connection Blocks (CB) [4]. In our proposed MT-FPGA, there are two 2-to-1 analog MUXes (implemented using transmission gates), two 4-to-1 MUXes (using tri-state buffers) and one 4-to-1 DEMUX (using tri-state buffers) in the North and South Connection Blocks. The two analog MUXes are replaced by a 2-to-1 MUX and a 2-to-1 DEMUX for digital signals in the East and West Connection Blocks.

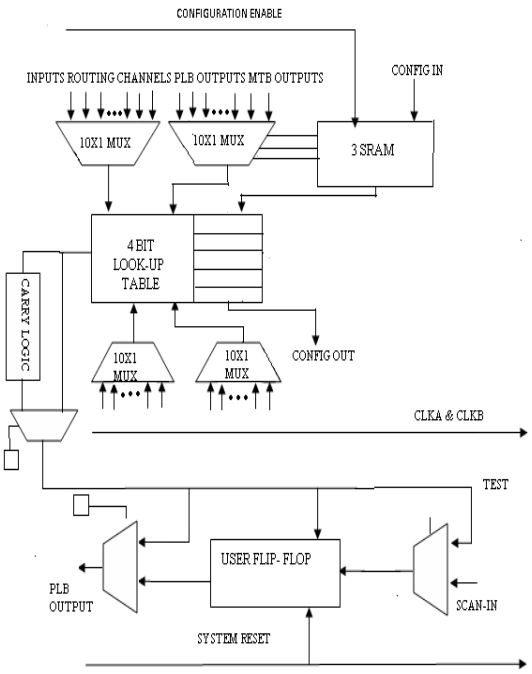

Fig.2 Logic description of a PLB

B. Multi-Technology Block (MTB)

The ability to integrate photonic devices along with digital and analog circuits on the same chip has made photonic technology best choice for current and future technologies. Investigations motivated the merits of optoelectronic approaches in optical communication and photonic information processing systems [5]**.** In order to illustrate the interconnection and communication among MTBs and PLB clusters located within same and neighboring MTLCs, an optoelectronic block embedded in the MTB space of MT-FPGA have been chosen. We use "pixel scale optical power meter" MTBs as a general purpose optical gateway where optically encoded signals can be received and converted into digital data and transformed to compensate for signal losses in the optical paths[4]

i) Components of Optical Power Meter

The pixel-scale optical power meter consists of a photo detector, photo receiver, analog-to-digital converter (ADC) module and storage elements. Additionally, buffers and a sample-and-hold circuit are added to maintain signal driving strength and integrity at the nodes. Fig. 4 shows how optical light enters into the system and passes through the series of components until it is converted into a digital signal. The purpose of the photo receiver circuit is to provide a flexible amplifier capable of amplifying both small and large amounts of current from the photodetector. So a desirable choice for this design is the Variable Gain Amplifier (VGA). A Flash ADC with fastest data conversion capability is selected as the ADC for MTB design. The ADC circuit has two different comparator circuit designs. To convert a total of $(2^N -1)$ comparators outputs to a 4-bit digital output signal, a 16:4 decoder is used. The MTB of the MT-FPGA chip receives an infrared laser beam from a modular laser diode controller through a planar-convex lens to prevent beam divergence and then sent into a beam splitter.

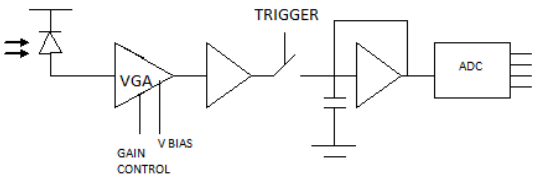

Fig.4. Top level diagram of MTB (pixel scale power meter)

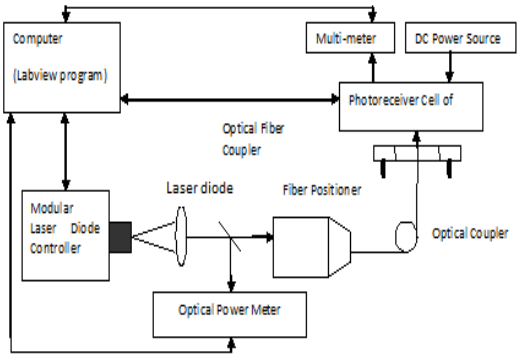

Fig.5. Experimental setup for testing optical MTB

The beam splitter divides the light into two paths for the purpose of providing an accessible measurement point so that the light can be measured and delivered to the photodetector simultaneously. One of the divided paths from the splitter continues on into a fiber coupler and coupling assembly. After being coupled into a single mode fiber, the light then travels to a second fiber mounting assembly used to direct the fiber tip onto a precise spot on the exposed photodetector of the MTB device under test in the MT-FPGA chip. Fig.5. Experimental setup for testing optical MTB.

IV. DESIGN OF THE HIGH SPEED MT- FPGA

When doing a very large scale integration (VLSI) layout, it is desirable to find some regularity in the topology to make the task of integration easier. Keeping this in mind, we decided to implement a 'tile' consisting of the MTLC, MTB and the Switch Blocks. The final MT-FPGA was then created by the custom integration of the array with the programmable I/O modules and the pad frame. Fig. 5 shows the floor plan of the MT- FPGA and the floor plan of a single tile. Inorder to obtain he benefits of increased speed and reduced power consumption, our MT-FPGA has been fabricated using an improved process technology (TSMC 0.25 μm deep sub-micron process) as compared to the previous generation (fabricated using TSMC 0.35 μm process). Also the current generation of the MT-FPGA has 15 MTLCs which is 6 more than the previous generation. This gives the second generation MT-FPGA a greater processing capability.

V. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

The goal of our work was to design an MT-FPGA which offered improved performance when compared to the existing design. In this section we will analyze each component individually and analyze how well this goal was met. For this a simple image processing system with an inexpensive digital camera, memory, and an FPGA device for performing basic operations on the image was considered. The image pixels are streamed from memory, N pixels per clock into the FPGA to be processed, where

N is determined by the memory port width. This limits the rate of processing to (R x C / N) cycles per image where R and C are the number of rows and columns in the image. For a small image, say 128x128, with a memory port width of 128-bits, N is 32 for 4-bit pixels. Hence, the number of clocks required to find for example the average intensity is (128 x 128 / 32) = 512 clocks. However, the MT-FPGA has all pixels available simultaneously and just has to sum them. If pair wise additions are performed each clock then it would require $\log_2$ (R x C) clocks to compute the sum, for this example clocks $\log_2$ (128 x 128) = 14 clocks.

Next we provide the area, speed and power measurements for each component from simulation and compare it with the results available for the previous generation. The combined dimensions of the MTLC and the MTB in the TSMC .25µm technology MT-FPGA are 215 µm by 317 µm, giving them a total area of 0.07 mm2. in comparison, the MTLC and the MTB of TSMC .35µm MT-FPGA had an area of 0.3 mm2. This gain is significant even if one ignores the inherent advantage obtained by scaling down to a lower technology. This was achieved because of the rigorous floor planning techniques adopted while integrating the individual components of the MTLC. The speed and area and power measurements for each component are shown in Table 1 and Table 2 .

	Existing MT-FPGA	**Proposed High Speed MT-FPGA**
Power consumption	17 mW	7 mW
Total area	0.3 mm^2	0.07mm^2

Table 1. Power and Area metrics of MT-FPGAs

	Image resolution				
Processing time (x 10^{-8} s)	**1**	**2**	**3**	**4**	**5**
Existing MT-FPGA	770	1386	1694	2156	2772
Proposed High Speed MT-FPGA	584.5	1052.1	1585.9	1636.6	2104.2

Table 2. Parameters showing the Processing time MT-FPGAs

Note: Pixel size: **1**- 128x128 **2**- 512x128 **3**- 1024x512 **4**- 2048x512 **5**-2048x1024

The increase in speed /clock frequency is achieved only at the expense of power consumption. Fig 6 shows the comparative analysis of Time of processing with image resolution.

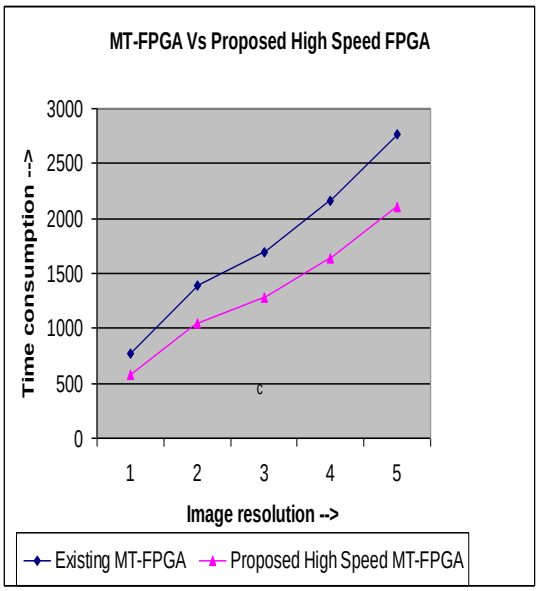

Fig 6. Processing time for different Image sizes of First generation MT-FPGA and Proposed High Speed MT-FPGA

In general, the time of processing increases with increasing image resolution. The proposed High Speed MT-FPGA has less processing time compared with existing MT-FPGA.

A plot of Power consumption and Area of the Existing and Proposed MT- FPGAs is shown in Fig 7 and Fig 8 respectively.

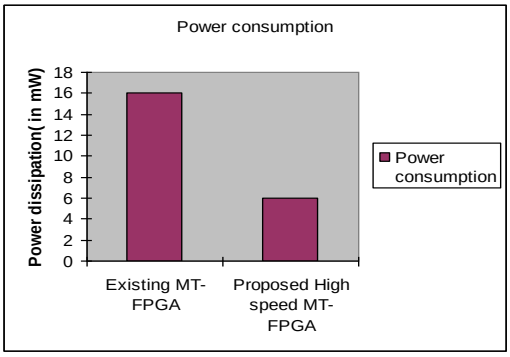

Fig 7. Power consumption of First generation MT-FPGA and Proposed High Speed MT-FPGA

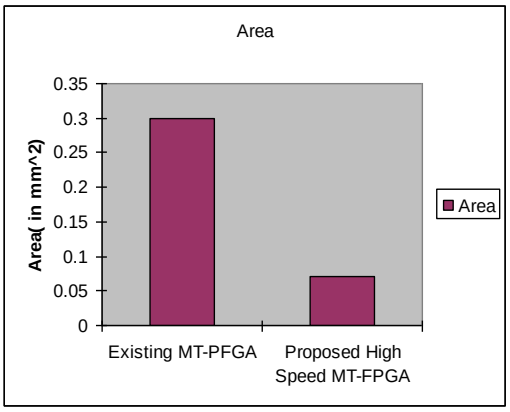

Fig 8 . Area metrics of First generation MT-FPGA and Proposed High Speed MT-FPGA

Although the high speed is achieved due to increase in clock frequency, the power consumption of proposed High Speed MT-FPGA is less compared to the existing MT-FPGA. The total area occupied by the proposed High Speed MT-FPGA is also less.

VI. CONCLUSION

In this paper we have proposed an improved version of the MT-FPGA. We have focused on achieving a high-speed design with improved area and power metrics. The results obtained from the simulation of the individual components have shown that our design of the MT-FPGA compares favorably with the previous version. As we scale down to lower technologies we will have to contend with reduced supply voltages, increased number of metal layers and a different set of electrical parameters. These will impact the architectures of the MTLC, Switch Block and the I/O module. Hence the existing design must continue to evolve to meet these new challenges. Dual Edge-Triggered Flip-flop and Low power Design of SRAM can be used in order to reduce the power consumption further.

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