International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:268
Vol.2, No.4, April 2013 DOI:10.15693/ijaist/2013.v2i4.52-56

Hardware Implementation of Wave Pipe ling Backtracking Switch for Optimizing Nocs

ANITA.P
IV SEM M.Tech (VLSI Design and embedded system),CMRIT, Bangalore,
Karnataka, India, 560037

SHRABANI BARAL
Assistant Professor/Department of ECE
CMRIT, Bangalore,
Karnataka ,India, 560037

***Abstract*. This paper presents the Hardware implementation of Wave-Pipelined Backtracking Switch for optimizing NoCs support guaranteed throughput. The proposed circuit-switched switch, based on a backtracking probing path setup, operates with a source-synchronous wave-pipeline approach. The switch can support a dead- and live-lock free dynamic path-setup scheme and can achieve high area and energy efficiency. It is a challenging task in a network-on-chip to design an on-chip switch/router to dynamically support (hard) guaranteed throughput under very tight on-chip constraints of power, timing, area, and time-to-market, and coded using Xilinx 10.1**

Index terms: Backing, circuit-switched, dynamic path-set up, guaranteed throughtput,network-on-chip (Noc),on- chip switch, soure synchronous, wave pipeline.

I. INTRODUCTION

AS the complexity of systems-on-chips (SoCs) increases, the network-on-chip (NoC) is being adopted as a scalable communication-centric solution for integrating numerous on-chip components i.e., sub blocks, processing elements (PEs), and intellectual properties (IPs). One of the most difficult tasks in NoC design is guaranteeing throughput (or providing a quality-of-service (QoS) mechanism) of the traffic offered by the on-chip components, particularly with the very limited budget of the on-chip resources. The requirements of the performance metrics for certain traffic classes, such as data loss, data rate (throughput), delay, and delay jitter, need complex QoS mechanisms involved in many levels of abstraction of NoC design. Many NoC-based applications used in hard real-time systems, as well for future possible NoC usages, demand a hard QoS (strong guaranteed throughput) requirement. An efficient and proper design of on-chip switching node (i.e., the switch or the router) is needed with an adequate QoS property, while keeping compatibility.

The two main themes in the literature for switching mechanisms used in the design of NoC routers are circuit switching and packet switching that impact greatly on the implementation overhead and the QoS property.

A. Guaranteed Throughput Implementation With The Packet-Switching Approach

A time-division multiplexing (TDM) time slot and "logical lanes" (virtual circuits with priority) solutions are used for the worst-case scenarios in most practical packet-switched NoCs to provide guaranteed data service. These solutions set up (or reserve) the dedicated path through a packet-based NoC for contention-free and deadlock avoidance of guaranteed data packets. The TDM approach faces difficulty in the management of huge time-slot tables at guaranteed service routers for contention-free communication, especially when the systems are scaled. Restriction of the routing function for deadlock-free data transfer in the virtual circuits with a priority approach may lead to throughput degradation in packet-switched NoCs . Moreover, the implementation of queuing buffers in the packet-switched routers dramatically increases the cost in terms of area required and power consumption

B. Guaranteed throughput implementation with the circuit-switching approach

The "pure" circuit-switching approach is favored to provide hard guaranteed throughput due to its attractive QoS property, once a circuit is set up . After this setup, end-to-end data can be pipelined in order at the full rate of the dedicated links with low delay, no data jitter, and in a lossless manner (i.e., without data dropping) due to there being no collisions among the data streams. Importantly, without queuing buffers and complex routing/arbitrating implementation, the circuit-switched router results in a low-cost (i.e., area, power) design suitable for the limited on-chip budget. However, a path-setup scheme used in circuit-switched NoCs needs critical considerations for proper functioning (i.e., dead and live-lock free) and

low-latency setup with minimization of introduced hardware overhead. Moreover, the dynamic and distributed feature of the path-setup in the circuit-switched NoC is also mandatory to ensure system flexibility and scalability in dynamic management (allocation) of the guaranteed communication circuits. This work advocates the guaranteed throughput implementation with the "pure" circuit-switching approach due to compact implementation of routers suitable for on-chip environment and an intrinsic hard QoS property after a circuit has been setup. A novel, practical pipeline circuit-switched switch design is proposed, termed backtracking wave-pipeline switch (or BW switch), to support on-chip hard guaranteed throughput applications.

II. MOTIVATION AND CONTRIBUTION

The relevant design issues of a pipeline circuit-switched switch are considered from both the network-level and the Implementation viewpoints. These lead to the key contributions of this paper. First, as introduced in Section I, a path-setup scheme is critical for circuit-switched NoC. The path-setup scheme (or path configuration) in circuit-switched NoC can be classified as static (at design time or at system boot up time) or dynamic (at runtime) approaches . The static path-setup approach lacks flexibility and scalability, while the dynamic path-setup scheme is flexible and more favored in some circuit-switched NoCs, . The mesh-based SoC BUS presented can dynamically set up a path in distribution, but faces high path-setup latencies, because the occupied channels block the setup of a new path. The work in proposes to use a supplemental packet-switched best-effort (BE) network for the delivery of the path configuration from a central control node (CCN). However, the use of a CCN limits system scalability, and the use of a BE network may result in quite high path-setup latencies, even in the order of , as stated in . At a neutral point, a hybrid packet-/circuit-switching architecture, requires an additional packet-switched network for circuit-setup and back pressure signaling, thus increasing overall system cost and complexity . Moreover, if congestion of the setup headers occurs, the preferred circuit-switching mode reluctantly changes to packet-switching mode . This degrades the QoS property of the circuit-switched data flows. However, no design efforts for dead-/live-lock free delivery of the setup headers are clearly mentioned in previous works . In a pipelined circuit-switching scheme, the data do not immediately follow the header into the network. Hence, it is first observed that it is beneficial if the setup header can flexibly backtrack (under a backtracking routing algorithm) to search for available alternative paths rather than wait (or queue) until the blocking channels become available. Such a backtracking-based path-setup scheme can be implemented in distribution to easily scale the system without the need of additional control network.Second, the implementation of NoCs without global synchronization schemes, e.g., mesochronous or asynchronous, where inter-clock domain data transfers are needed, becomes common in practice. In such schemes, source-synchronous1 wave-pipeline data transfers with transceiver designs are efficiently used to combat multiple-clock-cycle multi-Gb/s transmissions in global (inter-router) links. An early study presented in reported that the on-chip wave-pipeline approach, used in global interconnections, offers high performance, while using a smaller area and being more energy-efficient than the pipeline approaches using latches or flip-flops. In the design of a pipeline circuit-switched switch (or router), a separate implementation between the data path and the control part is feasible, since, after the path is set up, data can be directly pipelined from source to destination in a control-free manner. From this point, it can be observed that the design of a pipeline circuit-switched switch, in which its intra-switch data path allows direct-forwarding (i.e., wave-pipelining) of the source-synchronous data from the links, can result in the required latency/throughput property of an on-chip end-to-end path close to that of a dedicated interconnection. The above observations are the motivation for using both backtracking and wave-pipeline techniques for the proposed BW circuit-switched switch, to support on-chip hard guaranteed throughput. The main contributions of this paper are given here.

TABLE I
FORMAT OF SWITCH-BY-SWITCH HANDSHAKE

Request Signal: Req (1 bit)	
0: Idle (Release)	1: Circuit Request
Answer signal: Ans (2 bits)	
00: Idle	10: Network Blocked
01: Circuit Acknowledge	11: Busy Destination

III. BACKTRACKING WAVE-PIPELINE SWITCH ARCHITECTURE

Here, we propose the backtracking wave-pipeline switch architecture for use under a torus topology. The torus topology is chosen, as the folded torus, a laid-out version of the torus, can fit the tile-based NoC implementation in a conventional 2-D chip, and its good path diversity can be naturally suited to a path-setup scheme with backtracking. The operation

of end-to-end communication with the proposed probing path-setup scheme is explained from a network-transaction viewpoint before detailing the proposed BW switch architecture

A. End-to-end flow-control operation with backtracking probing path-setup scheme

A typical end-to-end communication, as used in the pipelined circuit-switching approach, is described to provide a clear description of the backtracking probing path-setup scheme used with the BW switch. Communication includes three basic phases: path-setup (or probing), transmission, and release. In the path-setup phase, a probe header containing destination address is sent from the source towards the destination to setup a communication circuit. When congestion occurs, the probe header needs to backtrack and search for alternative links, instead of waiting for a busy link to become idle. That is, the path is set up under a backtracking probing path-setup scheme. When the probe header reaches its destination, an ACK signal is returned to the source. Then, in the transmission phase, the source starts to transmit source-synchronous data through the set up path to the destination. Fig. 1 illustrates the inter-switch and switch-wrapper interconnections with this handshake. Each switch has five bidirectional ports: four ports are connected to corresponding neighboring switches, and the remaining port is connected to the on-chip IP through a wrapper. According to this handshake scheme, one bit is used for the **Request** (**Req**) signal to denote the on-probing state (circuit request) and the circuit idling state. Two bits are used for the **Answer** (**Ans**) signal. An **Ans** status of "01" denotes that the receiver is ready to accept data from the sender, whereas a status of "10" denotes that the intended path is blocked in the network, forcing the probe header to backtrack to discover possible alternative paths.

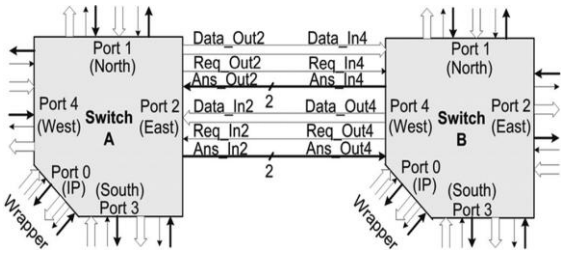

Fig. 1. Switch-by-switch interconnection scheme

. An Ans after the last data status of "11" denotes that the receiver is not ready to receive data (e.g., due to being busy, or having an overflow at the receiving buffer). During the setup and the transmission phases, Req is set to "1." When Ans is "00," the probe header continuously advances until it reaches the destination. Then, the destination returns "01" to the source wrapper. When the source wrapper receives "01", it immediately starts to transmit the pipelined data.

B. Proposed switch architecture and design

As motivated in Section II, the key targets of a proposed BW switch architecture is to support the backtracking probing path setup scheme, and to allow direct-forwarding of source-synchronous data transmissions. As for the backtracking feature of the path-setup scheme, some design issues are first considered. The EPB-based probing path-setup performs a straightforward depth-first search of the network using only profitable links Overall Architecture and Operation**:** The proposed switch architecture has the following main components that can be divided into two function groups.

• The data path includes CROSBAR with internal transceivers to support a direct-forwarding (wave-pipelining) of the source-synchronous data.

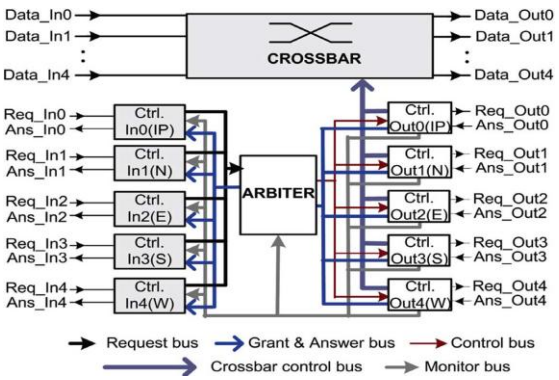

Fig.2, Proposed BW switch Architecture

• The control part includes Ctrl Ins, Ctrl Outs, and ARBITER. Each pair of Ctrl In and Ctrl Out performs handshaking activity at a certain bi-directional port, namely, North, East, South ,West, and IP.

IV. Design of CROSSBAR with Internal Transceivers*:*

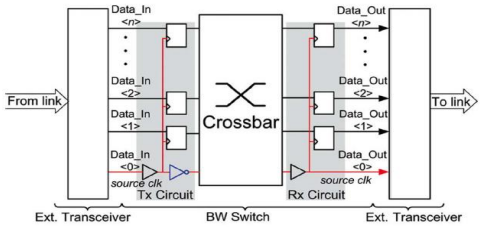

Fig. 3.Internal transceivers (gray boxes) in use with crossbar

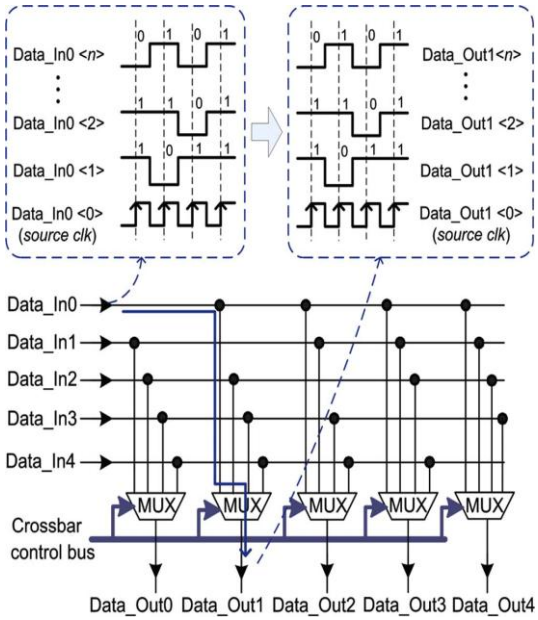

Fig 4. Mux based crossbar structure supporting data wave pipeling

The **CROSSBAR** with internal transceivers is the key component to perform the wave-pipelining of source-synchronous data. Regarding the layered design concept in the NoC paradigm, the router/switch and the transceiver (with inter-router link) can be designed independently. They can cooperate in NoCs, provided the interface between them is defined. As introduced in Section II, the design of source-synchronous transceivers (with wave-pipelined links) becomes common practice. It is studied to improve energy efficiency and data rate and to combat PVT variations, random mismatch, and crosstalk. In these transceivers, the received data can be realigned with the received (source) clock (as in circuit-switched NoC), or with a local (router) clock (often with synchronizing first-in first-out (FIFO), as in packet-switched NoC) . In cooperating with a circuit-switched switch, like the BW switch, the realignment of data to the source clock can be applied.. In the BW switch, the concept of wave-pipeline is illustrated in the sense that it allows direct-forwarding of the source-synchronous data (i.e., data along with source clock) from its inputs to the corresponding outputs. In other words, the crossbar of the BW switch can be considered to be a set of intra-switch links that requires internal transceivers to work with a source-synchronous direct-forwarding scheme.

V IMPLEMENTATION

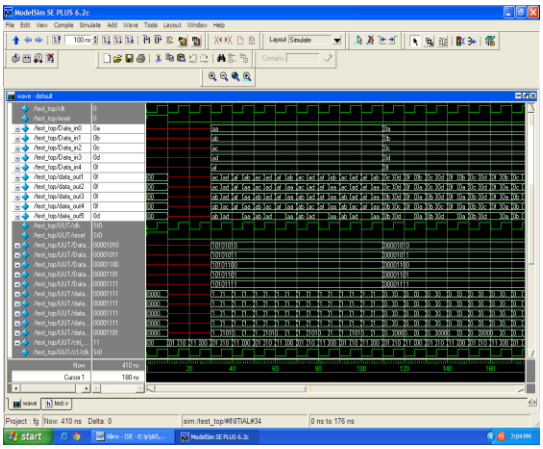

Fig 5 Mux based crossbar structure

VI. CONCLUSION AND FUTURE STUDY

This paper has presented a practical and cost-effective design of the proposed BW switch to support guaranteed throughput that combines both backtracking and wave-pipelining features. The backtracking feature provides a dynamic and dead- and live-lock free path-setup scheme in a distributed fashion. The wave-pipelining (i.e., direct-forwarding) feature practically provides low fall-through latency and high multi-Gbps bandwidth, and suggests suitability for an end-to-end source-synchronous data transmission. In addition, a BW switch prototype with 16-bit-data 5-bidirectional-port configuration has been fabricated and tested for area minimization, to reduce the latency and to increase the speed .In this paper, the HDL-based implementation of the BW switch, can result in fast switching with reduced latency and has good portability.

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Authors Profile

Anita.P received the **B.E.** degree in Electronics and communication engineering from the Golden valley institute of technology, Kolar gold field, Bangalore University, Karnataka, India, in 2001.Currently doing **M.Tech.** in Electronics and communication engineering (VLSI Design and embedded system) from CMR Institute Of technology in VTU , Bangalore, India. Her research interest includes wireless communication, Low power VLSI, Communication networks.

Shrabani Baral received the **B.E.** degree in Electronics and tele-communication engineering from the Orissa College of Engineering, Bhubaneswar, UTKAL University, India, in 1995 and M.Tech in Digital electronics, from CMR Institute Of technology in VTU, Bangalore, India. Currently Working in CMRIT, Bangalore, from 2006 till date. Her research interest includes wireless communication, Mobile communication optical fiber Communication networks.