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HIGH SPEED ALU ARCHITECTURE WITH MAC UNIT FOR IOT PROCESSOR

S.S.Sreeja[1], N.Vidhya[2],J.Vinitha[3]E.Manoranjitham[4]

[1,2,3]UG Scholar, Dept. of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India.

[4]Assistant Professor, Dept. of ECE, Tejaa Shakthi Institute of Technology for Women, Coimbatore, India.

ABSTRACT: This paper describes a design methodology of a single clock cycle MIPS RISC processor using Verilog to ease the description, verification, simulation and hardware realization. One of the most basic operational units in the processor is an ALU. ALU is a critical component of a microprocessor and is the core component of central processing unit. This paper describes the design technique for high speed Arithmetic and logic unit design. This research work proposes novel high sped ALU for IOT applications. MAC unit with modified booth algorithm is used for high speedALU in the processor. RADIX-4 hybrid adder is used in the MAC unit to increase the speed of the processor. Thus we can reduce the overall delay. Once detecting the particular approaches for input, output, main block and different modules, the Verilogdescriptions are run through a Xilinx ISE 10.1simulator, followed by the timing analysis for the validation, functionality and performance of the designated design that demonstrate the effectiveness of the design. Then it is implemented using TMSC 90nm CADENCE ENCOUNTER.

Key words: *IoT, ALU, MAC, MIPS, RISC, Booth Multiplier*

I. INTRODUCTION

Low power circuit design has now become an important subject of interest, which is evident from the surge of related activities in the engineering and research domain. In the past, the device density and operating frequency were low enough that the power dissipation was not a constraining factor in the chips. However, as the scale of integration improves, more transistors are being packed into a chip that leads to an increase in the processing capacity of chips and thereby results in the increase of power dissipation. Earlier the major concerns among researchers and designers for designing integrated circuits were on area, speed, and cost; while secondary importance was paid to power dissipation. In recent years, however, this scenario has changed and now reducing power dissipation through improved circuit design techniques is an important research area. With the increasing demand of battery operated portable systems, it is important to increase the battery life as much as possible, since it is the limited battery lifetime that typically imposes strict restriction on the overall power dissipation of such systems. Although the battery industry has been making efforts to develop batteries with a higher energy capacity, however a revolutionary increase in the energy capacity does not seem imminent. In the absence of low power circuit design techniques, present and future portable systems will either suffer from a very short battery life or a very heavy battery pack. So, portable systems that are powered with batteries require low power circuit design for increasing their lifetime. Low power circuit design is highly desirable for burst mode type systems, where computation occurs for only short duration, and the system is inactive for the majority of time. For such type of battery operated systems, it is highly unacceptable to have excessive drainage of useful battery power during the long standby period. To integrate more functions on a chip, the feature size of a transistor has to shrink. As a result, the power dissipation per unit area rises, which increases the chip temperature. Since the dissipated heat needs to be removed to maintain an acceptable chip temperature, large cooling devices and expensive packaging techniques are required in portable devices and high-performance digital systems such as microprocessors. The issue of reliability of an electronic system with the increase in system temperature also accelerates the need for low power circuit design. High power dissipation systems often run hot, and the high temperature tends to accelerate the silicon failure mechanism. Another major demand for low power circuit design comes from environmental concerns. Modern offices are now furnished with office automation

equipment's that consume large amount of power. Since electricity generation is a major source of air pollution, inefficient energy usage by electronic equipment indirectly contribute to an increase in the environmental pollution. The requirement for low power circuit design varies from applications to applications. In case of battery operated portable systems, the overall goal of reducing the power dissipation is to keep the battery lifetime and weight reasonable; and for high performance and non-battery operated systems, the overall goal of power minimization is to reduce the overall system cost (cooling, packaging and energy bill) and also to increase the system reliability. Hence, reducing the power dissipation in electronic systems by utilizing low power circuit design is becoming a top priority issue. Internet of Things (IoTs) is a concept where variety of things/objects are connected to each other through wireless or wired connections and unique addressing schemes are able to interact with each other and cooperate with other things/objects to create new applications/services and reach common goals. In this context the research and development challenges to create a smart world are enormous. A world where the real, digital and the virtual are converging to create smart environments that make energy, transport, cities and many other areas more intelligent.

The goal of the Internet of Things is to enable things to be connected anytime, anyplace, with anything and anyone ideally using any path/network and any service [5].

The typical IOT system consists of three subsystems:

- Sensor: To collect the data from the device
- Controller: To process the sensor data.
- Communication: To transmit the processed data & to transmit.

The primary requirement of the IOT device is the Ultra Low power consumption since the device will be used in remote locations & may not have power source.

II.RISC BASED MIPS SINGLE-CYCLE PROCESSOR

Here, We are using RISC based MIPS instruction set architecture. The MIPS single cycle processor performs the tasks of instruction fetch, decode, execution, memory access and write back all in one clock cycle.By using the PC value 32-bit value of the next instruction to be executed. The data values can be operated on by the ALU whose operation is determined by the control unit. The ALU of this single-cycle MIPS processor can be speeded up by using the MAC unit with RADIX-4 modified booth multiplier and Logic Unit adder.

III. BASIC MAC UNIT

The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register [7].

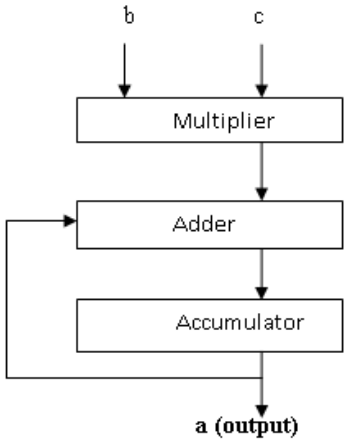

Figure1. Basic MAC unit

$$a \leftarrow a+(b*c) \quad (1)$$

Where, a→ accumulator register b&c→inputs of the multiplier.

RADIX-4 hybrid Adder can be used with an additional advantage of high speed. One implementation of the multiplier could be modified booth multiplier.

IV.DESIGN OF PROPOSED MAC UNIT

The Fig.2 shows the block diagram of proposed MAC Unit consisting RADIX-4 modified booth Multiplier. The result of multiplier is provided to the input of Accumulator through RADIX-4 hybrid adder.

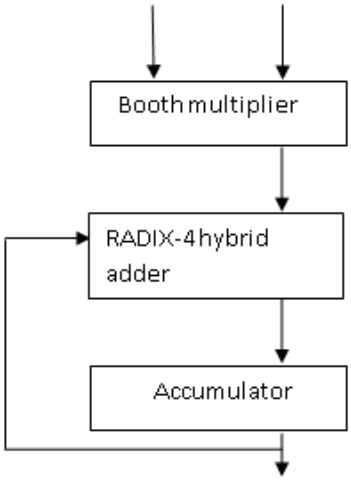

Figure2. Proposed MAC unit

V.PROPOSED BOOTH MULTIPLIER

If an operation to multiply two N –bit numbers and accumulates into a 2N -bit number, addition, subtraction, Sum of Absolute Difference (SAD), and Interpolation is considered. The critical path is determined by the 2-bit accumulation operation. If a pipeline scheme is applied for each step in the standard design of Fig. 1, the delay of the last accumulator must be reduced in order to improve the performance of the MAC. The overall performance of the proposed VMFU is improved by eliminating the accumulator itself by combining it with the hybrid adder function. If the accumulator has been eliminated, the critical path is then determined by the final adder in the multiplier. The basic method to improve the performance of the final adder is to decrease the number of input bits. In order to reduce this number of input bits, the multiple partial products are compressed into a sum and a carry by hybrid adder. The number of bits of sums and carries to be transferred to the final adder is reduced by adding the lower bits of sums and carries in advance within the range in which the overall performance will not be degraded. A 2-bit CLA is used to add the lower bits in the hybrid adder. In addition, to increase the output rate when pipelining is applied, the sums and carries from the hybrid adder are accumulated instead of the outputs from the final adder in the manner that the sum and carry from the hybrid adder in the previous cycle are inputted to hybrid adder. Due to this feedback of both sum and carry, the number of inputs to hybrid adder increases, compared to the standard design. In order to efficiently solve the increase in the amount of data, a hybrid adder architecture is modified to treat the sign bit.

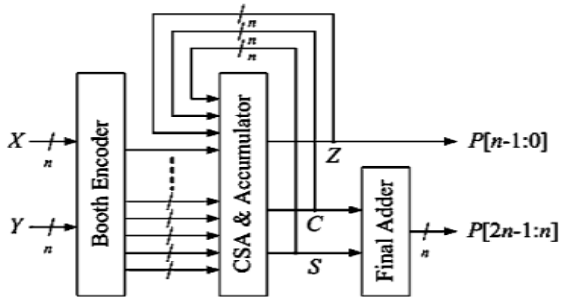

Figure 3. Booth encoded MAC unit

MODIFIED BOOTH ENCODER

In order to achieve high-speed multiplication, multiplication algorithms using parallel counters, such as the modified Booth algorithm has been proposed, and some multipliers based on the algorithms have been implemented for practical use. This type of multiplier operates much faster than an array multiplier for longer operands because its computation time is proportional to the logarithm of the word length of operands. Booth multiplication is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is possible to reduce the number of partial products by half, by using the technique of radix-4 Booth recoding. The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ±1, ±2, or 0, to obtain the same results. The advantage of this method is the halving of the numberof partial products.To Booth recode the multiplier term, we consider the bits in blocks of three, such that each block overlaps the previous block by one bit. Grouping starts from the LSB, and the first block only uses two bits of the multiplier. Fig 4 shows the grouping of bits from the multiplier term for use in modified booth encoding.

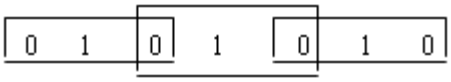

Figure 4. Grouping of bits from the multiplier term

Each block is decoded to generate the correct partial product. The encoding of the multiplier Y, using the modified booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in the multiplier performs a certain operation on the multiplicand, X, as illustrated in Table 1

Table 1. Operation of Modified Booth Encoder

Block	Re-coded digits	Operation on X
000	0	0X
001	+1	+1X
010	+1	+1X
011	+2	+2X
100	-2	-2X
101	-1	-1X
110	-1	-1X
111	0	0X

For the partial product generation, we adopt Radix-4 Modified Booth algorithm to reduce the number of partial products for roughly one half. For multiplication of 2"s complement numbers, the two-bit encoding using this algorithm scans a triplet of bits. When the multiplier B is divided into groups of two bits, the algorithm is applied to this group of divided bits [8].

TABLE 2. Design summary

Parameters	**Normal ALU**	**Proposed ALU**
No.Of.Slices	**158**	**148**
No.Of.Bonded IOBs	**101**	**32**
No.Of 4 input LUTs	**282**	**263**

VI.RESULT AND CONCLUSION

This work presents a functional unit which is designed with multiplier-accumulator (MAC), with addition, subtraction, sum of absolute difference. A Modified Booth multiplier circuit is used for MAC architecture. Compared to other circuits, the Booth multiplier has the highest operational speed and less hardware count. The basic building blocks for the unit are identified and each of the blocks is analyzed for its performance.MAC unit is designed with enable to block. Using this block, the MAC unit is constructed and MAC unit parameters are calculated. The presented technique explores its applications in multimedia/DSP computations, where the theoretical analysis and the realization issues are fully discussed.In this paper we used Xilinx-ISE tool for logical verification, and further synthesizing it on Xilinx-ISE tool using target technology and performing placing & routing operation for system verification.

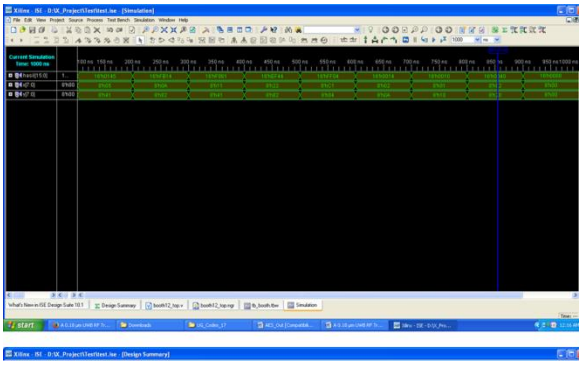

FIGURE 5. SIMULATION OUTPUT OF BOOTH MULTIPLIER

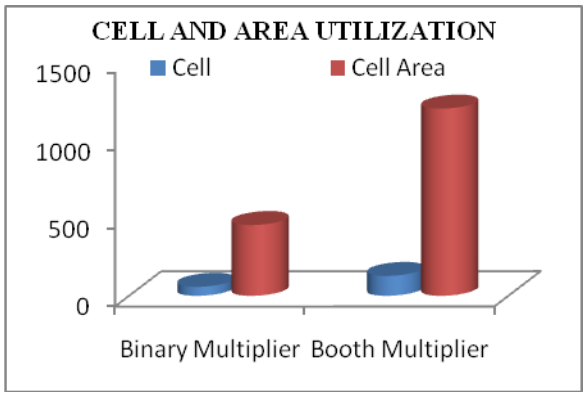

FIGURE 6. CELL AND AREA UTILIZATION

TABLE 2.CELL AND AREA UTILIZATION

Multiplier Type	CELL	CELL AREA
Binary Multiplier	58	455
Booth Multiplier	128	1203

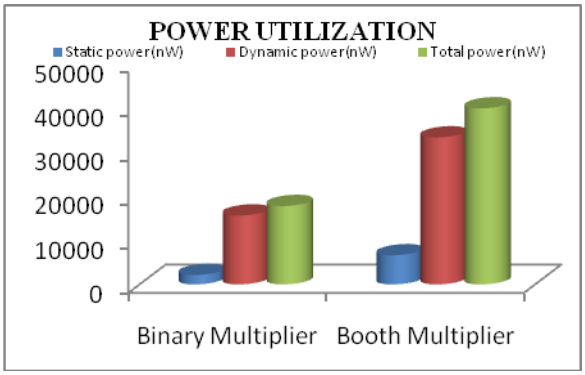

FIGURE 7.POWER UTILIZATION

TABLE 3.POWER UTILIZATION

Multiplier Type	Static power(nW)	Dynamic power(nW)	Total power(nW)
Binary multiplier	2152.34	15670.36	17822.70
Booth multiplier	6619.65	33412.12	40031.78

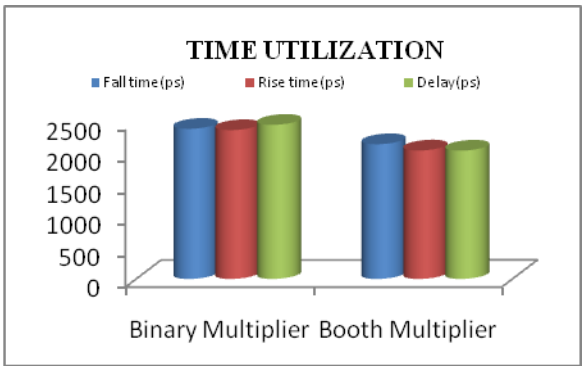

FIGURE 8.TIME UTILIZATION

Our proposed work has achieved a high speed ALU when compared to the existing technique.

TABLE 4.TIME UTILIZATION

Multiplier Type	Fall time(ps)	Rise time(ps)	Delay(ps)
Binary multiplier	2390	2369	2453
Booth multiplier	2145	2045	2043

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AUTHOR'S PROFILE

N.Vidhya is presently pursuing Bachelor's degree in Electronics and Communication Engineering at Tejaa Shakthi institute of Technology, Coimbatore. she has interested in VLSI Design using Cadecnce Encounter TMSC 90nm and Embedded system.

S.S.S.Sreeja is presently pursuing Bachelor's degree in Electronics and communication Engineering at Tejaa Shakthi institute of Technology, Coimbatore. she has interested in VLSI Design using Cadecnce Encounter TMSC 90nm and Digital image processing.

J.Vinitha is presently pursuing Bachelor's degree in Electronics and communication Engineering at Tejaa Shakthi institute of Technology, Coimbatore. she has interested in VLSI Design using Cadecnce Encounter TMSC 90nm and Medical electronics.

E.Manoranjitham obtain BE ECE in 2011 and ME VLSI Design in 2013 in Anna University and She is presently working as a Assistant Professor in Dept. of ECE at Tejaa Shakthi Institute of Technology for Women, Coimbatore. She is interested in Lowpower VLSI design, Digital system design and VLSI Digital Signal Processing.