FPGA Based,Vertically Partitioned Ternary ContentAddressable Memory Using SRAM Cell

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***Abstract*—Ternary content addressable memory TCAM is a kind of semiconductor memory that operates for determining a match between received search data and stored data in TCAM bitcells. These memories performs very high speed lookup operations, but when compared to conventional RAM technology,TCAM circuitry suffers from certain limitations such as low access time, low storage capacity, circuit complexity and much high cost. So, this paper adopts an idea of implementing TCAM functionality by using basic RAM cell. To offer more significant table entries a partitioning technique called vertical partitioning of conventional TCAM table is done and then, search algorithm is applied to perform a match operation. In this paper a 16X16 size of SRAM based TCAMmemory is implemented on Altera Quartus II software and results are simulated using modelsim to verify its functionality.**

Index terms: TCAM, SRAM, VERTICAL PARTITIONING (VP), APT, BPT, APTAG.

I.INTRODUCTION

Ternary content-addressable memory (TCAM) is a dedicated high-speed memory device that searches its entire data in a single clock cycle .The term "ternary" refers its capability to store and query data using three different inputs: 0, 1 and don't care (X). Ternary content addressable memory (TCAMs) executes very high-speed search operation in a deterministic time [1]. A conventional TCAM cell circuitry consists of a bit storage unit and a comparison unit. A pair of memory cell is used in bit storage unit for holding stored data and comparison circuitry works for compared an input word against pre stored data.[2,3].Ternary content addressable memory (TCAM) memory can be seen as an extension of random access memory (RAM) but dissimilar to RAM**.** Stored data is accessed by the contents in TCAM rather than by memory address as in SRAM andmatch location is sent on output line [4,5].Since TCAM can store don't care state (X), which can be matched to both 0 and 1 during a comparison operation, so multiple matches may occur. In a typical search operation an input searchkey is compared in contrast to all the stored words
in parallel and returns the address of the best matches [6]. These days TCAMs are used in parallel and returns the address of the bestin parallel and returns the address of the best matches [6].These days TCAMs are used in various applications such in IP networking, microprocessors, real-time matching applications, compression,virus-detection, intrusion-detection systems, gene pattern searching in bioinformatics, and image processing etc. [7]. But most important application of TCAM is in network routers where to compare the destination address of incoming IP packet against the stored addresses and forward the packet to the appropriate output port with very high speed.There are various research works available on FPGA implementation [8,9], some of the relates research is explained here.

An area efficient stacked TCAM cell for fully parallel search is discussed in [10]. This paper proposed a TCAM cell that consists of a pair of memory elements connected to an associated pair of comparisonscircuits, which are interconnected so as to be disposed substantially vertically in active NMOS and active PMOS layers. On the basis of previous literature [11] TCAM array uses a hybrid partitioning (HP) of the conventional TCAM table to buildmemory architecture of TCAM.It breaks a conventional TCAM table into columns, vertical partitions (VP) and rowscalled horizontal partitions (HrP) that result into number of TCAM subtables. Developing a hybrid typeTCAM design decouple all the CAM cells from the match line, and provide a fast path to accelerate the search operation.
Novel memory architecture, named Z-TCAM, which joints the TCAM functionality with SRAM is proposed in [12]. Two designs for Z-TCAM of sizes 512 × 36 and 64 × 32 have been implemented on Xilinx Virtex-7.Search latency for each design is three clock cycles. Each TCAM subtable is given a name as hybrid partition and the collective partitioning scheme (vertical and horizontal) is called HP. The role of verticalpartitioning (VP) part of HP is to divide TCAM word of dbits into msubwords, where each sub word is of *w* bits.Hybrid partitioning spanning the same addresses ranges.A method of implementing classification TCAM functionality using primarily RAM is discussed in [13]. This method provides significant table entries in a given area, or significantly less area for a given table size than the conventional ternary CAMs.

II.VP SRAM-BASED TCAM

VP-SRAM based TCAM represents a SRAM based Implementation of TCAM with vertical partitioning of conventional TCAM table. Hereestablishinga table partitioning concept in a conventional TCAM table for attaining practical alternative in the form of VP SRAM-based TCAM. Vertical partitioning technique logically dissects a conventional TCAM table into 'k' number of columns to forms 'k' number of TCAM sub-tables. These TCAM sub tables are then further processed by applying a data mapping scheme in each TCAM subtableto be stored in their correspondingSRAMblocks. This partitioning technique divides a TCAMinput word of width 'W' into 'k' sub-words, each of w bitsto store into 'k' subtables[13].

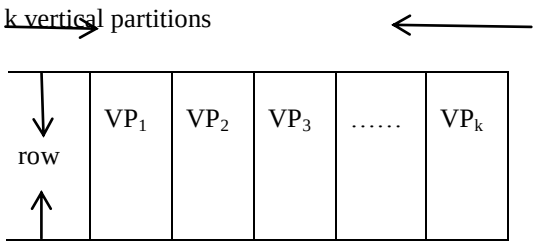

Fig 1. Vertical partitioning.

***TCAM Architecture*:**Fig 1showing a conceptual view of partitioning scheme. Its main components includes 'k' Bit Position Tables (BPTs), 'k' Address Position Tables (APTs), 'k' APT Address Generators (APTAGs), Priority Encoder (PE), and AND operation. BPTs and APTs are constructing from SRAM.In a BPT, 2^w bits of memory are grouped into 2^{w-p}rows; with each row having a 2^pnumber of bits. Each row is assign with a value called Last Index (LI).The length of last index value is w+1 bit and it is always initialized by a minus one value.The 'w-p' high order bits of input sub-word are used to find out a specific row in BPT, thus acting as an address.This address is named as BPT Address (BPTA) that Indicate a particular bit position in the selected row.A conceptual view of each vertical partitioning is shown in figure two where k represents number of vertical partitions. In BPT 'p' that forms lower order bits, is called as Bit Position Indicator (BPI)of the input sub-word and these bits are used to indicate a particular bit position in the row selected in a TCAM subtable. If the bit position point out by BPI is high, then it means that the input sub-word is present in that particular subtable otherwise not. APTAG generates an address known as APT Address (APTA) that is used to index a row in APT[13].

APTAG consists of a 1's counter and adder circuit. The 1's counter calculates the number of 1's in the selected row of BPT up to the indicated bit position and then forwards this information to adder. The adder then adds the output of the 1's counter and Last index value of the selected row. The proposed TCAM borrows the concept of BPT and APTAG from [14] .The size of each APT is 2^w*N where 2^w denotes number of rows and 'N' is the number of bits in each row where each bit denotes an address position.

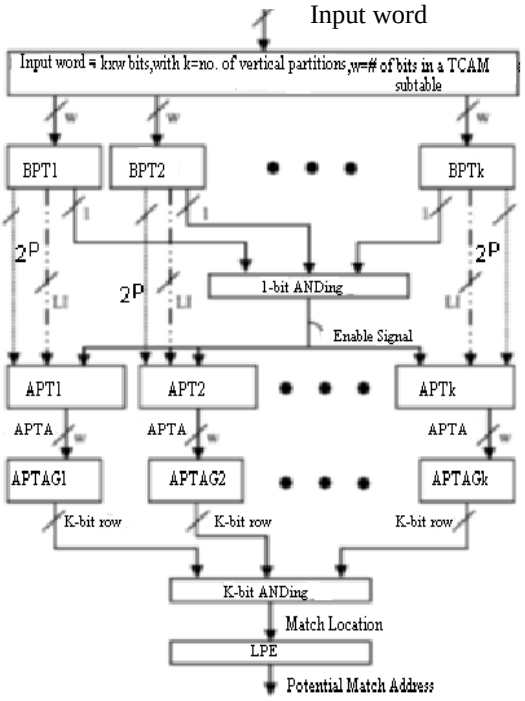

Fig. 2.Architecture of VP TCAM[13]

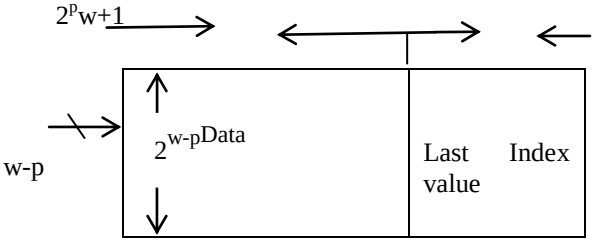

Fig. 3. BPTArchitecture

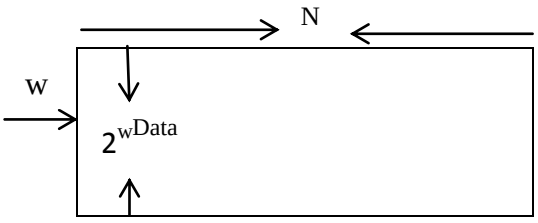

Fig. 4. APT Architecture

III.TCAM Search Operation

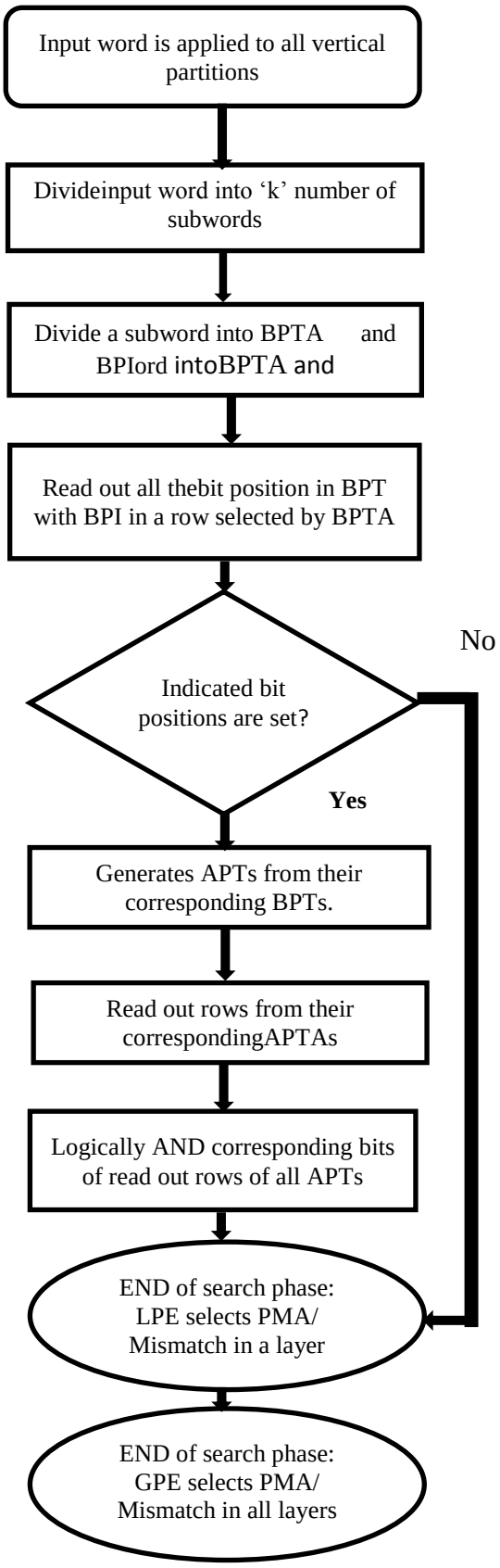

Fig 5:Flow chart of Search Phase

The first part of operation is data mapping phase. In this phase vertical (column-wise) partitioning of a conventional TCAM table is done into TCAM sub-tables, which are then further extended into their binary counterparts and handled in such a way that every sub-word in all divisions is mapped to its corresponding bit in its equivalent BPT and original address (s) of the sub-word are mapped to its corresponding bit (s) in the corresponding APT. In second phase, of the operation an input word is applied and it's MA, if exits, is sent to output. The proposed TCAM achieves search operation in a vertical partitioned is shown in fig. 6 flow diagram.

IV.SYNTHESIS RESULTS

The overall memory architecture is modeled using VHDL in Altera Quartus II 8.0sp1 software and the simulation of the design is performed using Modelsim SE 6.5 to verify the functionality of the design. Each of the modules are designed using partitioned architecture consists of BPT, APT, APTAG and priority encoder. First a 16 bit data word 1000011110000111 is applied as input. For two vertical partitions it is divided into two, 8 bit sub-words, 8 bit BPT and APT is constructing to store 64 bit entries. Which generate activation signal to indicate whether a match or mismatch occur in that partition. The internal signals are analyze individually to generate a PMA and MA. Fig 6 shows the Modelsim simulated results for a given 16 bit input that is 1000011110000111.The given input is divided into two subwords and applied to their BPTs. From these subwords BPI and BPTA values give the last index for activated bit position that is further transfer to APTAG. APTAG generated outputs are 4 & 6 corresponds to APT 1 & 2 gives values 0001000010000000 &0000000010000000.AND product of these two gives final match address that is 8 in this case.

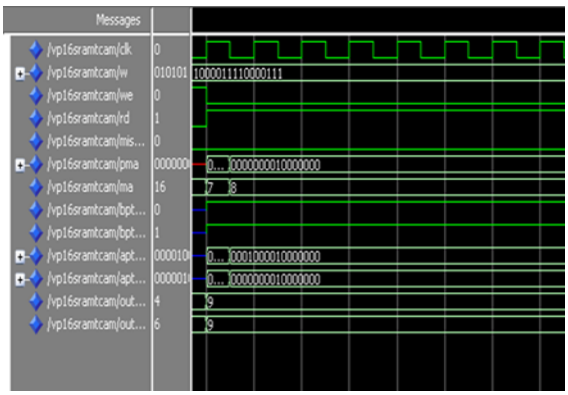

Fig 6. Simulated Results of VP-TCAM

Fig 7 shows RTL schematic for designed circuit.Here we have designing the digital circuit of TCAM using hardware description language,

so the design is engineered at a higher level of abstraction than transistor level or logic gate level. In HDLs declares the registers and describes the combinational logic by using constructs that are familiar from programming languages such as if-then-else and arithmetic operations. This level is called *register-transfer level*. The term refers to the fact that RTL focuses on describing the flow of signals between register.

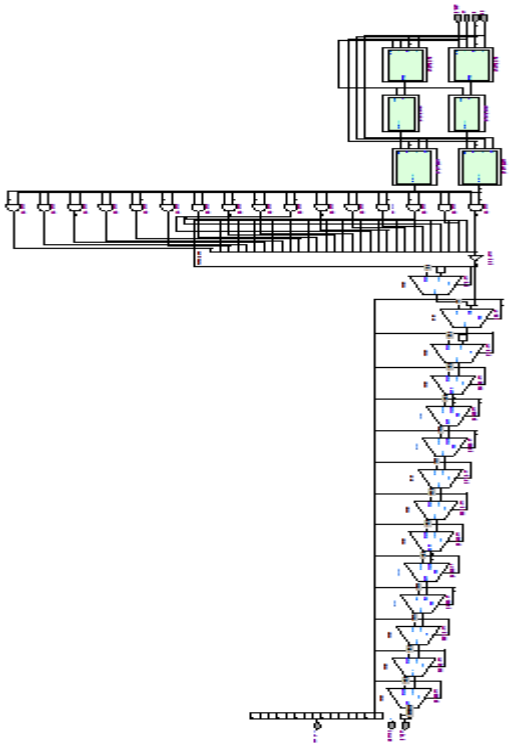

Fig 7.RTL Schematic of VP-TCAM

Table 1. Shows the synthesis results of VP-TCAM on Quartus Altera II software. Selected device family is Cyclone III, EP3C5F256C6.Device utilization summary includes the number of LUTs required to construct the design, power consumption and delay. Table 2 and Fig 8 Shows the comparison of simulated results with existing TCAM technique.

Table 1.Device Utilization Summary

Memory Dimensions : 16X16				
Device Family Selected: Cyclone III:EP3C5F256C6				
# of partitions	Method	# of LUTs	Delay (ns)	Power (mw)
k=2	VP-TCAM	106/5136 (2%)	10.583	61.37

Table 2.Comparision with Existing Technique

Memory Dimensions 16X16				
Case(L,k)	Method	# of LUTs	Delay (ns)	Power (mW)
(2,2)	HP-TCAM[15]	126	14.361	115.04
	P-TCAM[15]	138	18.199	115.13
	B-TCAM[15]	69	19.337	110.62
k=2	VP-TCAM	106	10.583	61.37

All the techniques shown in Table 2 are SRAM based and layered. P-TCAM that is parity bit based TCAM, B-TCAM that is Bank selection technique based TCAM and HP-SRAM based TCAM that is hybrid partitioned TCAM all uses hybrid structure. Only VP SRAM based TCAM is single layer techniques. L in the figure shows the number of layers and k shows the number of vertical partitions. Synthesis results of proposed VP-TCAM are compared with exiting TCAM based technique. Maximum numbers of LUTs are used in P-TCAM technique, largest delay is observed in B-TCAM where as the largest power consumer is P-TCAM technique. So, the designed VP-TCAM gives improved performance.

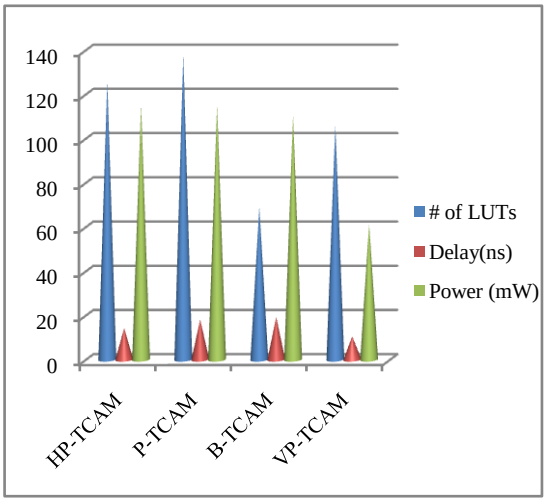

Fig 8.Comparision Graph.

V. CONCLUSION

In this paper, we worked on VP SRAM-based TCAM. On the basis of result analysis it can be said that the memory size dependent on number of vertical partitions and also on the dimensions of the conventional TCAM. In general, size of VP SRAM-based TCAM increases as number of bits in sub-word increases or alternatively when

number of vertical partitions reduced. The results shows that the VP SRAM based TCAM is better in terms of power consumption,delay and number of LUTs compared to all other techniques except the LUT utilization in Bank selection (B-TCAM)Technique.

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