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Design of a Low Power Level-up Shifter in Multi Supply Voltage Design using MTCMOS Technique

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***Abstract*— Level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage. It allows communication between different modules without adding up any extra supply pin. It is a key circuit component in multi-voltage circuits. The main objective of the work is to minimize power dissipation in shifter circuit, which is due to different supply voltages in the circuit. The proposed method uses MTCMOS technique, which is one of the low power design technique to achieve power minimization. The model presents a new low-power level shifter (LS) for logic voltage shifting from sub-threshold to above-threshold domain. The new circuit uses the multi-threshold CMOS technique to provide a wide voltage conversion . The proposed design is implemented in CADENCE Virtuoso 180-nm CMOS technology process which converts 230-mv input signals into 3-V output signals. The new LS reaches a propagation delay value of 17 ns, a static power dissipation of only 115.3 pW, for a 1-MHz input pulse.**

Index terms -Level Shifter, Sub-threshold, MTCMOS, low power, low voltage.

I. INTRODUCTION

The most direct way to reduce power dissipation in digital LSIs is to reduce supply voltage. Several low power design techniques were used. Sub-threshold LSI is the most widely used in power aware applications. However there are a number of design challenges imposed and several studies were carried out. Among the techniques known in the literature to reduce power consumption, those based on power supply voltage reduction are considered very effective even though they can severely penalize speed performances . An alternative approach, known as the multi-supply voltage domain technique , consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time-critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to improve power efficiency. For extremely low-power applications, the presence of sections of the system operating in a sub-threshold regime is a valuable option.

A key challenge in the design of efficient multiple-supply circuits is minimizing the cost of the level conversion between different voltage domains while maintaining the overall robustness of the design. To such a purpose, level shifter (LS) circuits have to be used. Traditionally, level shifter circuits were used to allow chip core signals to be transmitted to the outside world through the pad ring, which often operated with different voltage levels. More recent techniques were emerged which allows for the increased use of voltage islands within chips.

This paper is organized as follows. Section II briefly gives a complete background analysis of the existing research work . Section III describes the conventional level shifter circuit and Section IV presents the proposed level shifter circuitry along its operation. Section V shows the experimental results , simulated waveforms and the performance comparison of power . Section VI concludes the paper.

II. RELATED WORK

The traditional LS topology is the differential cascade voltage switch (DCVS) circuit. The DCVS-LS behaves as a ratioed circuit As a consequence, pull-up and pull-down strengths has to be properly balanced to ensure correct functionality of the circuit. This is difficult to achieve in practice when input signals have sub-threshold voltage levels [2].

Lütkemeier estimated that a NMOS-to-PMOS ratio of ~2400 is needed to design a fully functional DCVS-LS circuit which converts .2 V input signal into 1-V output signals, with 90-nm CMOS process technology [8].

Yejoong Kim proposed limited contention level converter circuit , which uses a pulsed control strategy to avoid contention. The circuit converts from .3 V to 2.5 V output signal. The circuit was fabricated in 130nm CMOS. It consumes 475 pW static power. The main disadvantage in this technique is the requirement of more number of transistors [11].

In [10] , a low-power negative level shifter for low voltage applications is presented. Which is used to reduce the switching delay and leakage current. Furthermore, a pull-down driver is proposed to increase driving capability under various operation modes. The circuit was designed in 130nm CMOS technology with power supply of 1.5V. Simulation results show that the switching delay and power consumption is reduced by 62% and 65%, respectively.

In [7], diode-connected and off-biased PMOS transistors are used to limit the drive strength of the pull-up network. The multi-threshold CMOS design technique is applied to trade-off speed and power consumption. But, due to the presence of off-biased PMOS transistors this approach is not easily

scalable, especially in static and dynamic energy consumption .

III. Conventional Level Shifter Method

The conventional LS (Level Shifter) circuit consists of

- a level conversion circuit and
- a logic error correction circuit (LECC) [3].

The complementary input signals (IN and INB) and the output signal (OUT) are applied to the LECC. Figure 1 shows the schematic of the conventional level shifter circuit. The operation principles of the circuits are described in the following sections.

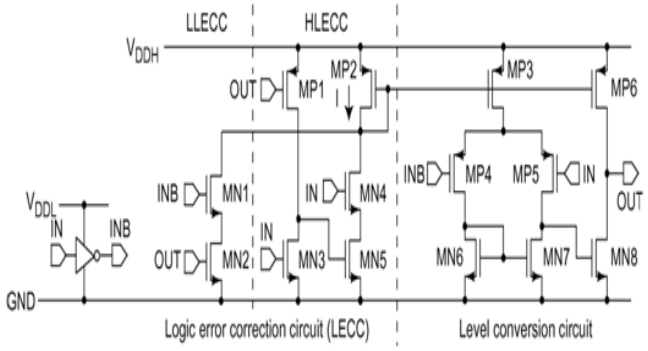

Fig. 1 Schematic of conventional Level Shifter Circuit

A. Logic Error Correction Circuit(LECC)

The LECC, which is shown on the left in Fig. 1, consists of two circuit blocks:

- a low logic error correction circuit (LLECC) and
- a high logic error correction circuit (HLECC).

The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current . When they do not correspond, the LECC detects the logic error, and the LLECC or HLECC supplies an operating current. In other words, the LECC supplies an operating current only when the input and output logic levels do not correspond to each other. When IN and OUT correspond, the LECC does not supply any current to the level conversion circuit. However, in fact, leakage current flows in the circuit. However, when the input voltage signal is high, the output node of the current mirror floats, thus negatively impacting the overall power consumption.

B. Level Conversion Circuit

The level conversion circuit, is based on a conventional two-stage comparator circuit which generates output voltage signal, OUT, according to the difference in the voltage of IN and INB. The output voltage is determined by the drive currents of pull-up transistor MP6 and pull-down transistor MN8, and the currents flowing in MP6 and MN8 depend on current flowing through MP2.

C. . Drawbacks

In this conventional comparator design, a current reference circuit needs to operate steadily. However, because the current reference circuit dissipates static current and increases power dissipation , it proves impractical to use.

IV. Proposed Level Shifter Circuit With Mtcmos Technique

The circuit diagram of proposed level shifter circuit based on MTCMOS technique is shown in figure 2.

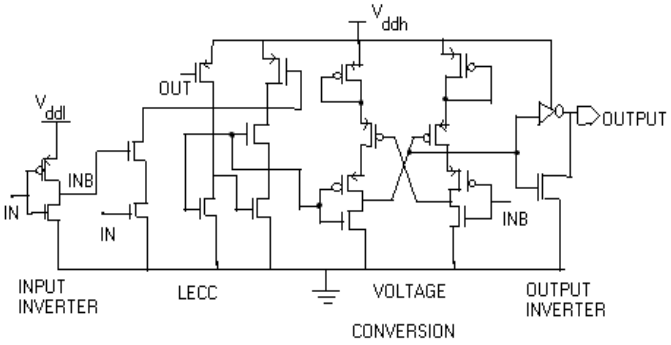

Figure 2. Schematic of Proposed Level Shifter Circuit based on MTCMOS Technique

A. Input Inverter

The input inverter consists of PMOS and NMOS transistors. They are driven by a lower supply voltage V_{DDL} . The source of the PMOS transistor is connected to low supply voltage and the drain of NMOS is connected to ground.

B. LECC (Logic Error Correction Circuit)

The LECC is driven by IN, INB, and OUT. The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current . When they do not correspond, the LECC detects the logic error.

C. Voltage Conversion Stage

The brief description of voltage conversion circuit is described as follows. It is based on DCVS (Differential Cascode Voltage Switch) logic. Figure 3 shows the detailed explanation of the voltage conversion circuit. The circuit is designed with low-voltage threshold (*lvt*), standard voltage threshold (*svt*), and high-voltage threshold (*hvt*) transistors. To provide fast differential low-voltage input signals and to increase the strength of the pull-down network of the main voltage conversion stage, the input inverter was created using *lvt* devices. To reduce the effect of cross bar current flowing in the nodes NH and NL, two *lvt* PMOS devices (MP2 and MP3) are adopted. MP4 and MP5 were chosen as *hvt* transistors. This helps in weakening the pull-up networks of the main voltage conversion stage.

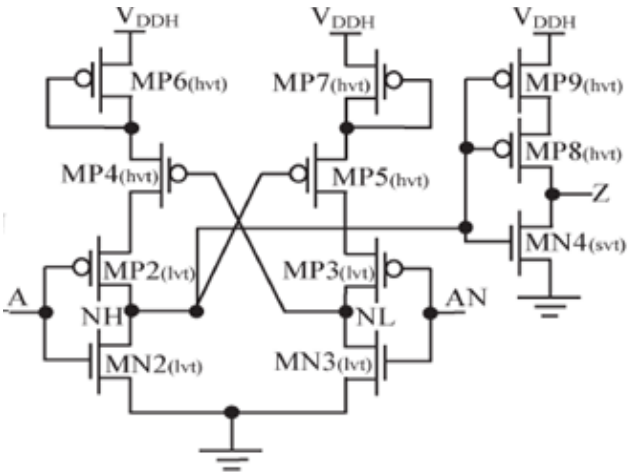

Figure 3 . Voltage Conversion Circuit

Finally, to ensure reliable voltage conversion, two diode-connected *hvt* PMOS devices (MP6 and MP7) were placed between the pull-up logics and the supply rail *V*DDH. These devices limit the pull-up strength, but also lead to considerable reduced static power. We now briefly describe the running of the proposed circuit with particular attention to the differences between the new architecture and the conventional DCVS one. A high to low transition of the main input causes MP4 being turned on. Its drain current brings the diode-connected MP6 device into the saturation region. This creates a voltage drop (i.e., *V*th,MP6) across MP6 terminals that produces a correspondent bulk source voltage drop on MP4. Due to the bulk effect, this increases the MP4 threshold voltage. The reduced voltage level (VDDH-*V*th,MP6) on the source terminal of MP4 limits its *V*GS, thus further weakening the MP4 action. All the above effects reduce the contention on the node NH, thus allowing faster discharging to be achieved.

D. Output Inverter

When MP4 is turned on, MP5 is consequently turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 on. For this reason, MP5 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current. The diode-connected MP7 device participates in minimizing the leakage current, also by increasing the threshold voltage of MP5. In fact,MP7 causes the source of transistor M5 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect.

V. RESULTS AND DISCUSSION

The proposed circuit is implemented in CADENCE – Virtuoso tool and implemented in 180 nm CMOS technology. Figure 4 shows the schematic drawn in Cadence tool. The circuit dissipates 115.3pW of static power with the supply voltage of less then 2V(1.8V). The fig.5 and fig. 6 shows the simulated waveform in Cadence and level shifted output waveform. Table 1 shows the performance comparison of various level shifter circuits. The table shows a considerable reduction in static power

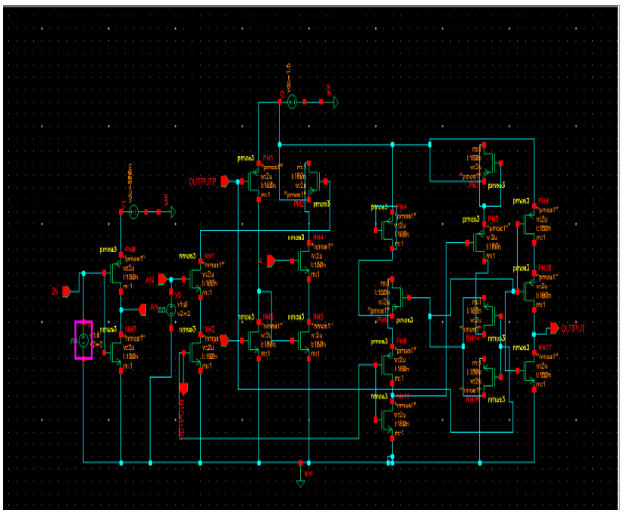

Figure 4. Schematic Circuit drawn in Cadence

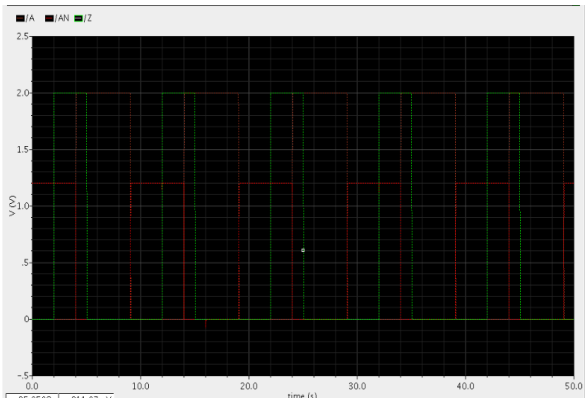

Figure 5. Simulated output Waveform in Cadence

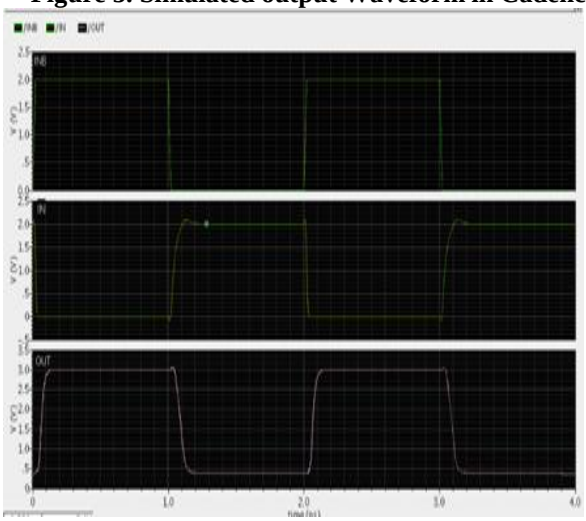

Figure 6. Level Shifted Waveform in Cadence

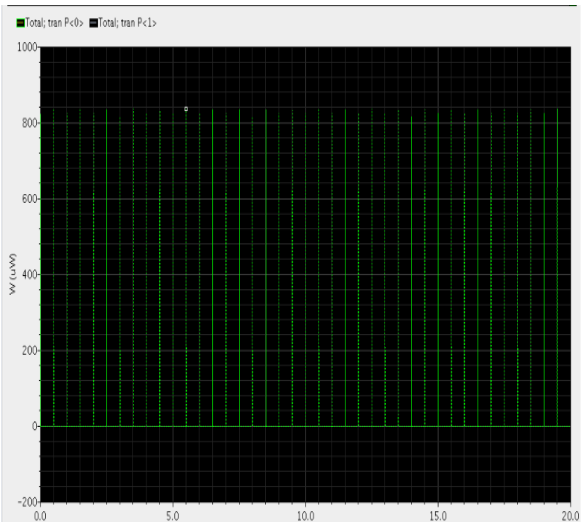

Figure 7. Power Spectral Graph of Proposed Circuit

The power dissipation of the proposed LS circuit can be expressed as

$$P = P_{dyn} + P_{int}$$
$$= C_L V^2_{DDH} f_{IN} + I_{AVG} V_{DDH}$$
$$= C_L V^2_{DDH} f_{IN} + (\Im I f_{IN}) V_{DDH}$$

$$P = (1 + \alpha) C_L V^2_{DDH} f_{IN} \quad (1)$$

where I_{AVG} is the average current flowing through the circuit. Equation (1) shows that P is independent of V_{DDL} and depends on f_{IN} and the square of V_{DDH} .

Parameter	Conventional LS	Proposed LS
Type of technology	350 nm	180 nm
Type	Comparator	DCVS
V_{DD} (V), f_{IN} (Hz)	0.4, 10 kHz	0.23, 1 kHz
V_{DDL} (V)	0.23 V	0.2 V
V_{DDH} (V)	3 V	2.5 V
Static Power (nW)	58 nW	115.3 pW

Table 1. Performance Comparison Table

VI. CONCLUSION

The proposed level shifter circuit with MTCMOS circuit is presented and it is simulated in Cadence Virtuoso tool. The proposed circuit with MTCMOS technique is implemented in 180-nm CMOS technology. The static power dissipation achieved was 115.3 pW with the supply voltage of 0.2 V.

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Authors Profile

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