International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:2682
Vol.4, No.2, February 2015 DOI:10.15693/ijaist/2015.v4i2.452-457

Design of Explicit Pulse Triggered Flipflops Using PTL Based AND Gate

V.VijayaRathina R.Subbulakshmi,M.E.
PG-Scholar, VLSI design,Department of ECEAssistant professor, Department of ECE
Sri vidyacollege of engineering and technologySri vidya college of engineering and technology
Virudhunagar, IndiaVirudhunagar, India

***Abstract*–In this paper a low power and low area pulse triggered flip flop has been analyzed. In low power application mainly, Power has become an important issue in modern Technology. The dominant part of this VLSI Process Design is power consumed by the clock. In all kinds of digital designs, flip-flop is the basic element of memory element and clocked signal. The Conventional TSPCFF is to use one extra NMOS transistor to shorten the delay and power. The conventional design removes the long discharging problem and reduces D to Q delay. Thus, the proposed design reduces the number of NMOS transistors stacked in the discharging path. The proposed design is compared with some conventional designs EP-DCO, CDFF, SCDFF, MHLFF and TSPCFF and the schematic and post-layout simulations have been done using tanner tool at 250nm VLSI technology .The proposed design has resulted in reduction of overall power consumption in comparison to some conventional technique EP-DCO, CDFF, SCDFF, MHLFF and TSPCFF respectively. The results also shows some reduction in leakage power**.

Key words – Flip-Flop (FF), Pulse-triggered, Low power.

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. The article concludes with the future challenges that must be met to design low power, high performance systems.

Based on pulse generation method, Pulse triggered flip-flops are classified into two types [1]. Implicit pulse-triggered flip flop and Explicit pulse-triggered flip flop. In implicit triggered flip-flop, the pulse is generated implicitly inside the flip-flop. In Explicit triggered flip-flops the pulse is generated externally [1]. This concept is illustrated in fig. 1. In this, clock pulse is generated first from clock (CLK) signal,which is then applied to the pulse-triggered flip-flop. In Explicit triggered flip-flops, the pulse generator can be shared by the neighboring flip-flops as shown in fig.1. It is energy efficient but it consumes more power for operating the circuit and hence not suitable for low power significant designs. Also due to the presence of large capacitive loads at the output i.e. if a pulse generator drive many number of flip-flops, the problem becomes more significant. It has some pulse width control issues also on applying low power techniques like conditionaldischarge technique.

In spite of this implicit triggered flip-flops are efficient for low power designs. But due to the presence of longer discharge paths it has some inferior timing characteristics. On applying some low power techniques, the timing characteristics become worse. So there is a need to enlarge the transistor sizes to produce wider pulses to trigger the data capturing of the flip-flops.

An explicit type flip-flop requires additional circuitry for pulse generation as the pulse trains are generated physically. The concept of pulse generation, explicit pulse triggered flip-flops consumes more energy than implicit one due to explicit pulse generator in explicit- FF.

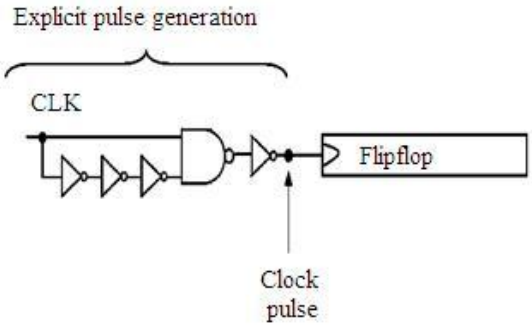

Fig 1. Illustration of Explicit Pulse Generation in Explicit pulse triggered flip flop.

The pulse generator can be shared by the neighboring flip-flops.A pulse-triggered FF consists of a pulse generator for strobe signals and a latch for data storage. Since the pulses are generated on the transition edges of the clock signal and very narrow in pulse width, the latch acts like an edge triggered FF. The circuit complexity of a pulse-triggered FF is thus greatly simplified since only one latch, as oppose to two latches in master-slave configuration, is needed. It can thus provide higher toggle rate than the conventional FF can and is found useful in high speed applications. Another advantage of pulse-triggered FFs is that they allow time borrowing across cycle boundaries and feature zero or even negative setup time.

II. CONVENTIONAL EXPLICIT TYPE PULSE TRIGGERED FLIP-FLOP DESIGNS

A.EP-DCO

EP-DCO is known as the Explicit Data Close to Output [7]. The schematic diagram of EP-DCO is shown in the fig.2. It consists of two charge keeper circuit. The pulse width of pulse generator depends on delay of the three inverters. In the circuit inverter I3 and I4 is used to latch the data and I1 and I2 is used to hold the internal node. It has serious drawback, when the input data does not change then the internal node X charges ad discharges at every clock cycle. The switching power dissipation is larger due to charging and discharging. The glitches also appeared at the output that would cause noise problems. To overcome this problem many other circuit developed like conditional discharge, conditional capture technique [8]-[11].

B. CDFF

CDFF is known as Conditional discharge flip-flop [14-18]. The schematic diagram of CDFF is shown in the fig. 3. It consist one extra NMOS transistor and the Q_fbk is connected to the input of this transistor. When the input Data is high than Q_fbk is low so N1 is off so there is no discharging path at every clock cycle. Hence the switching power is reduced. If the input changes from „0" to „1"the internal node X is discharge through MN1, MN2 and MN3 as-summing that (Q, Q_fbk) were initially (low, high).

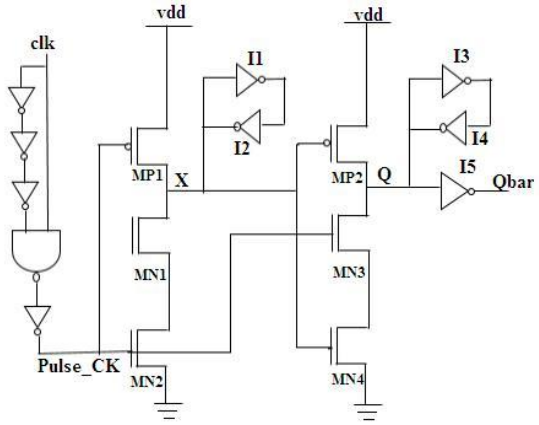

Fig. 2 Explicit type Data close to output pulse triggered flip-flop

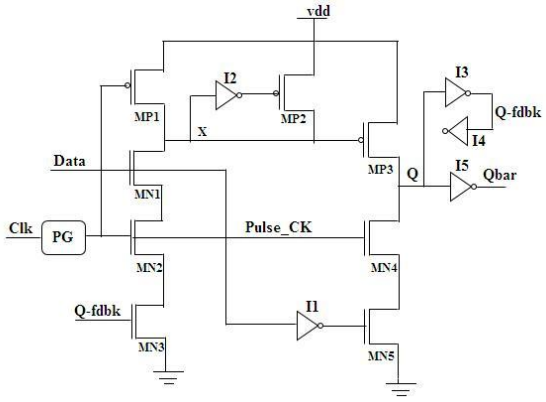

Fig. 3 Conditional Discharge Flip-flop

As the internal node X is discharged it pulled MP2 ON and the output will be charged. If the input changes from„1" to „0", then the first stage is disabled and node X retains its pre-charge state, and node Y will be high so the output Q is discharged through MN4 and MN5.Since node X is not charging and discharging periodically at every cycle no glitches will appear on the output node Q when the input Data stays high.

C. SCDFF

SCDFF is known as static conditional discharge flip-flop [17].The schematic diagram of SCDFF is shown in the fig. 3.It is using a static latch structure but it differs from the CDFF design. The node *X* is completely removed from periodical pre-charges. It exhibits a longerdata-to-Q (D-to-Q) delay than the CDFF design. It is caused by a discharging path consisting of three stacked transistors because the both designs face a worst case delay, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption.

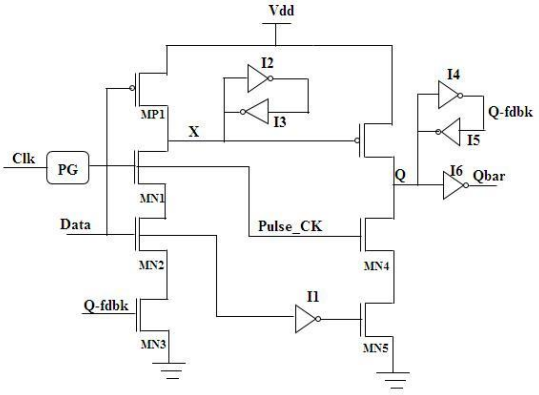

Fig. 4. Static Conditional Discharge Flip-flop

D. MHLFF

MHLFF is known as modified hybrid latch flip-flop [19]. The schematic diagram of MHLFF shown is the fig 5. The MHLF is implicit type pulse triggered flip-flop. In this three inverter and one NMOS is used to generate the pulse. In the output node Q, the Inverter I1 and I2 is used to latch the data. In this design, a weak pull-up PMOS MP1 transistor used which is controlled by output signal Q. It is used to maintain constant to the node level X at high transition when Q is zero. This MHLFF design completely removes periodically discharging of node X. Hence, switching power is reduced. But it takes longer Data to Q delay during „0" to „1" transition because node X is not pre-charge. Larger transistor MN1 and MN2 is required to enhance the discharging capability. Another drawback of this design that node X becomes floatingwhen output Q and input data both equal to „1" [18].

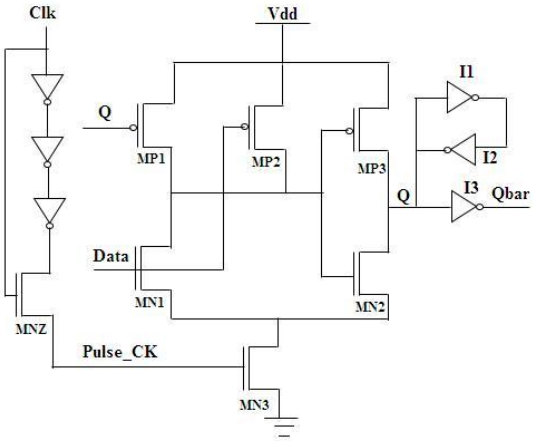

Fig. 5 Modified hybrid latch flip-flop

E. TSPCFF

In these three circuits worst case occurs when data change from„0" to „1".The design is to use one extra NMOS. The circuit has several advantages over earlier circuits. In this circuit,a weak pull-up PMOS transistor MP1 is used so that the internal node X is easily charged. The circuit also called as pseudo-NMOS logic design and it also reduces the load capacitance at node X [20-21]. Second a pass transistor MNX is used which is controlled by clock pulse. The Data to Q delay is reduced, if the input data directly goes to the output. Third, the pull down network of the second stage is completely removed and pass transistor MNX provides a discharging path.

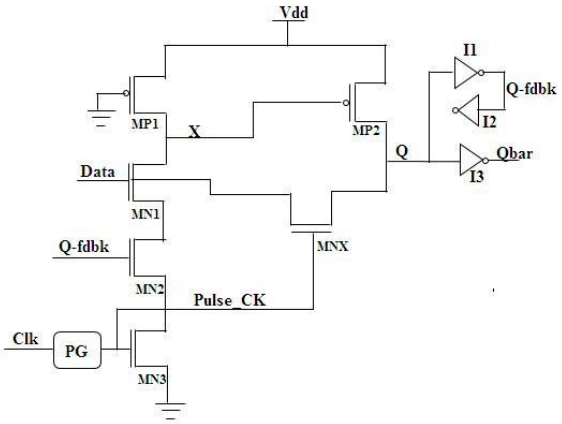

Fig .6.True Single Phase Clock Flip-Flop

III. PROPOSED EXPLICIT TYPE PULSE TRIGGERED FLIP-FLOP DESIGNS

The Proposed pulse triggered flip-flop design shown in figure 6. It employs a static latch structureand at

two-input pass transistor logic (PTL)-based AND gate is implemented we are designing this circuit as well as by using the pass transistor logic with NMOS pass transistor in existing pulse triggered with signal feed through scheme. By using the Pass Transistor Logic family idea we are using only one clocking transistor so it will be consuming only less power in the clock network of the flip-flop when compared to all other circuits. As well as proposed pulse triggered flip-flop having only 16 Transistors.

In proposed flip-flop, the clocking transistor is used to control the charge of transistor N5.Since the two inputs of AND logic to control the discharge of transistor N1 are mostly complementary (except during the transition edges of the clock), the output node Z (in between N2 and N3) is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N3 and N4 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N5 by a time span defined by the delay inverter I3.The switching power at node Z can be reduced due to a diminished voltage swing.

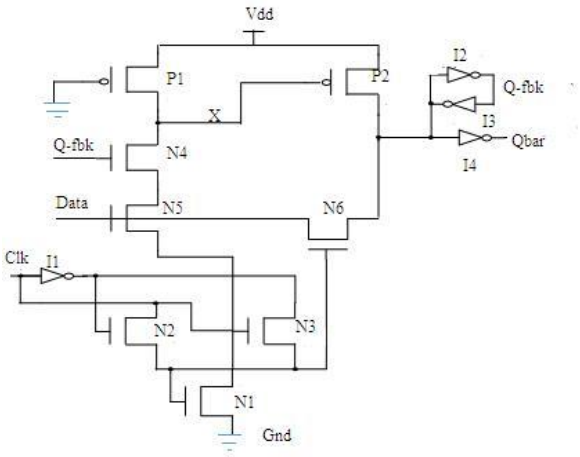

Fig.7. Proposed pulse triggered flip-flop

The switching power at node Z can be reduced due to a diminished voltage swing. When a clock pulse arrives, if no data transition occurs, i.e., the node Q and the input data are at the same level, on current passes through pass transistor N6, which keeps the input stage of the Flip-flop from any driving effort. If a "0" to "1"data transition occurs, node X is discharged to turn on transistor P2, which then pulls node Q high. Since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

In the proposed pulse triggered flip-flop design the area and average power consumption can be reduced when compared to existing data close to output flip-flop and modified hybrid latch flip-flop design. It will be having muchreduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

The simulation is performed for various pulse triggered flip-flops such as explicit data close to output, conditional discharge flip-flop, static conditional discharge flip-flop, modified hybrid latch flip-flop, true single phase clock design to demonstrate the effectiveness of our proposed design.

IV. RESULTS COMPARISON

By comparing the EPDCO, CDFF, SCDFF, MHLFF and TSPCFF, we are obtaining the minimized no of transistors, low voltage andpower consumption.

V. CONCLUSION

In this Paper, the proposed pulse triggered flip-flop is designedwith two-input pass transistor logic (PTL)-based AND gate isimplemented in existing pulse triggered flip-flop with signalfeed through scheme of pseudo n-MOS logic pass transistor.This design is combination of conditional pulse enhancementscheme and existing pulse triggered flip-flop with signal feedthrough scheme. The average power consumption and numberof transistor count should be reduced by proposed pulsetriggered flip-flop design. It will be having much reducedpower and area when compared to the other two designs. Atthe same time due to the reduced no of transistor count we canreduce the delay oriented things also. Thus we are reducingthe overall switching delay and power, area consumption. Sothis circuit will be acting as good sequential elements whencompared to other flip-flop design.

VI. FUTURE WORK

In future work of the paper, theembedded logic function will be design and implement usingproposed pulse triggered flip-flop design. To analysis andreduces the average and leakage power

consumption of theembedded based logic function of pulse triggered flip-flopdesign and to achieve high performance pulse triggered flip-flopdesign.

REFERENCES

[1] Kayalvizhi S, Devaki M, " Energy efficient pulse triggered flip flop design for low power application," !JEST, vol. 5, no. 4, pp. 21-26, April 2013. 774 20.

[2] K. Chen, "A 77% energy saving 22-transistor single phase clocking D flip-flop with adoptive-coupling configuration in 40 nm CMOS," in *Proc.IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.

[3] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional pushpullpulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 482–483.

[4] H. Partovi, R. Burd, U. Salim,F.Weber, L. DiGregorio, and D.raper, "Flow-through latch and edge-triggered flip-flop hybrid elements,"in*Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 138–139.

[5] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEEJ. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[6] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems,"
IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[7] J. Tschanz, S. Narendra, Z. Chen, S.Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207 212.

[8] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, "The implementation of the Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[9] S. Sadrossadat, H. Mostafa, and M. Anis, "Statistical design framework of sub-micron flip-flop circuits considering die-to-die and within-die variations," *IEEE Trans. Semicond. Manuf.*, vol. 24, no. 2, pp. 69–79, Feb. 2011.

[10] M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometer flip-flops in the energy-delay space," *IEEE Trans. CircuitsSyst.*, vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[11] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," *IEEETrans. Circuits Syst.*, vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[12] M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I - methodology and design strategies," *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst.*, vol. 19, no. 5, pp. 725–736, May 2011.

[13] M. Alioto, E. Consoli and G. Palumbo, "Analysis and comparison inthe energy-delay-area domain of nanometer CMOS flip-flops: Part II-results and figures of merit," *IEEE Trans. Very Large Scale Integr. (VLSI)Syst.*, vol. 19, no. 5, pp. 737–750, May 2011.

[14] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8,
pp. 1263–1271, Aug. 2001.

[15] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional prechargetechniques for power-efficient dual-edge clocking," in *Proc. Int. Symp.Low-Power Electron. Design*, Aug. 2002, pp. 56–59.

[16] P. Zhao, T. Darwish, and M.Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484,May 2004.

[17] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edgetriggered flip-flop using an output-controlled discharge configuration,"in*Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 2429–2432.

[18] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulsetriggeredflip-flop design with conditional pulse enhancement scheme,"*IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 2, pp. 361–366, Feb. 2012.

[19] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for highspeed applications," *IEE Proc. Circuits Devices Syst.*, vol. 152, no. 2,pp. 118–122, Apr. 2005.

[20] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," *IEEETrans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, no. 1, pp. 33 44, Jan. 2009.

[21] P. Zhao, J. McNeely, S. Venigalla, G. P. Kumar, M. Bayoumi, N. Wang, and L. Downey, "Clocked-pseudo-NMOS flip-flops for level conversion in dual supply systems," *IEEE Trans. Very Large Scale Integr. (VLSI)Syst.*, vol. 17, no. 9, pp. 1196–1202, Sep. 2009.

[22] V. G. Oklobdzija, "Clocking and clocked storage elements in a multi gigahertz environment," *IBM J. Res. Devel.*, vol. 47, no. 5, pp. 567–584, Sep. 2003.