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Design of Convolution Encoder using Ancient Indian Vedic Sutra

Ms. Shreyasi P. Bhat
PG Scholar/Deptt.of E&T
BDCE, Sevagram, India

Prof. R. D. Kadam
Assistant Prof./Deptt. of E&T
BDCE, Sevagram, India

Prof. P. R. Indurkar
Associate Prof./Deptt. of E&T
BDCE, Sevagram, India

***Abstract*— In mathematics, multiplication is the most commonly used operation. This paper explores the design approach of a convolution encoder using booth multiplier and vedic multiplier which leads to improve delay and faster speed. Here, the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. The combinational path delay of 16x16 bit Vedic multiplier and Convolutional encoder based on Vedic obtained after synthesis is compared with Booth multiplier and Convolutional encoder based on Booth, it is found that the proposed Vedic multiplier circuit and Convolutional encoder based on Vedic seems to have better performance in terms of speed. The coding is in VHDL and synthesis is in Xilinx 13.1i ISE simulator.**

***Index terms - Convolutional Encoder, Multiplier, Urdhava Tiryakbhyam, Vedic Mathematics, VHDL, XILINX*.**

I. INTRODUCTION

Multiplication is most important function in arithmetic operations. Since multiplication decreases the execution time of most algorithms, hence there is a need of high speed multiplier. The Vedic Mathematics is very different method which reduces human mind works. Vedic mathematics is the name given to the ancient system of mathematics, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved like arithmetic, algebra, geometry or trigonometry. Performing arithmetic calculations especially multiplication, a computer spends a considerable amount of its processing time, an improvement in the speed for performing multiplication will increase the overall speed of the computer. Usually, multiplier is a large block of a computer system. Developing an efficient multiplier architecture that performs partial product generations and additions. Here, the computation time involved is less as compared to conventional multipliers like booth multiplier. The combinational path delay and the device utilizations obtained after synthesis is compared. The proposed Vedic multiplier based Circuit seems to have better performance in terms of speed also.

For control of distortion during transmission of data in digital communication systems, error control coding is generally used in various communication systems. The main function of an error control encoder is to increase the reliability of message during transmission of information. In communication, the channel introduces noise and interference which corrupt the transmitted signal. Errors in bit result during transmission and the number of bit errors depends on the amount of noise present and interference in the communication channel.

Convolutional codes are the most widely used channel codes in communication systems. These codes are developed with a separate strong mathematical structure. Convolutional codes is used to convert the entire data stream into one single code word and those encoded bits depend not only on the current 'k' input bits but also on past input bits of the sequence. In convolution encoder technique, condition is that number of input bits 'k' must be less than output 'n' of convolution encoder. In this work, the synthesis and simulation of Convolution encoder using booth multiplier and Vedic multiplier is described. This work shows that convolution encoder using Vedic multiplier is more efficient than convolution encoder using booth multiplier.

Convolutional codes protect information by adding redundant bits to any binary data. The convolution encoder computes each n-bit symbol (n >k) of the output sequence from linear operations on the current input k-bit symbol and the contents of the shift register(s). Thus, a rate k/n convolution encoder processes a k-bit input symbol and computes an n-bit output symbol with every shift register update. Convolution codes are commonly specified by three parameters; (n,k,m).

n = number of output bits
k = number of input bits
m = number of memory registers

Figure 1 illustrated the example of convolution encoder, which proves that input stream 'k' is less than output 'n'.

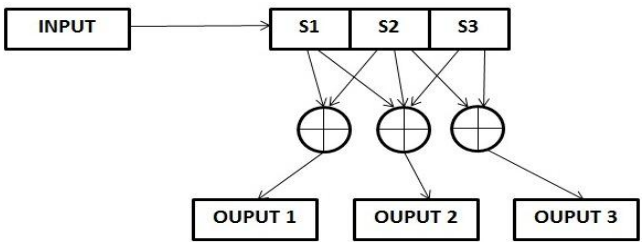

Figure 1. Example of Convolution Encoder

II. CONVOLUTION ENCODER USING BOOTH MULTIPLIER

Booth's algorithm is most popular method for 2's complement multiplication. It increases the speed of the process by analysing multiple bits of multiplier at a single time. This scheme was designed by Andrew D. Booth in 1951. Booth algorithm is an easiest way for this type of multiplication which treats both positive and negative operands. It allows n-bit multiplication to be done using fewer than n additions or subtractions, hence it makes faster multiplication. It operates on the principle that strings of 1's in the multiplier require no addition but just shifting and a string of 1's in the multiplier from bit weight 2k to weight 2m can be treated as 2k+1 to 2m.

The steps for performing booth multiplication are as follows:

- Let the multiplicand be 'B' and multiplier be 'Q'.
- Assume initially value of 'A' and 'Q-1' is zero.
- The main step is to check last two bits.
- There will be iterations according to the number of multiplier.
- For example, if the multiplier is of 2-bit then 2 Iterations will be done, for 4-bit multiplier 4 iterations are done, and so on.
- Now, the algorithm starts, first the last two digits are checked and if the two bits are "00" or "11" the only Arithmetic Right Shift is done.
- And if the last two bits are "01", then A is added with B, and result is stored into A.
- If the last two bits are "10", then A is subtracted from B, and result is stored into A.
- Finally, the result obtained is coded in binary form which gives the desired output.
- In this way multiplication of any two numbers is performed using booth algorithm.

Figure 2 shows the proposed convolution encoder design using booth multiplier.

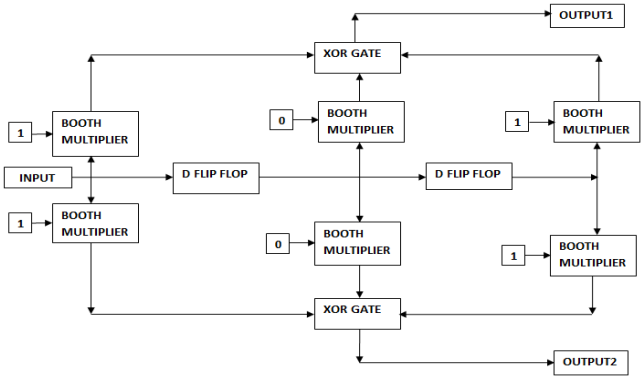

Figure 2. Block Diagram of Convolution Encoder Using Booth Multiplier [7]

Here, Six Booth multipliers are used, which are used for multiplication of two numbers, one number comes from the input of convolution encoder as an input stream and second number is as a input of Booth multiplier. All the Booth multipliers output is given to XOR gate. The function of XOR gate is to perform XOR operation. The function of D flip flop is when clock is '1' then it gives output, otherwise no output is obtained. Finally, the circuit gives two outputs as Output1 and Output2.

III. CONVOLUTION ENCODER USING VEDIC MULTIPLIER

Multiplication using Urdhva tiryakbhyam Sutra is shown in Figure 3. The numbers to be multiplied are written on two consecutive sides of the square. Each of the small squares is divided into two equal parts by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the same box. All of the digits lying on boxes are added and producing sum and carry digits simultaneously. Finally, results are obtained by the addition of sum digits and the previous carry digits. Carry for the first step is assumed to be zero.

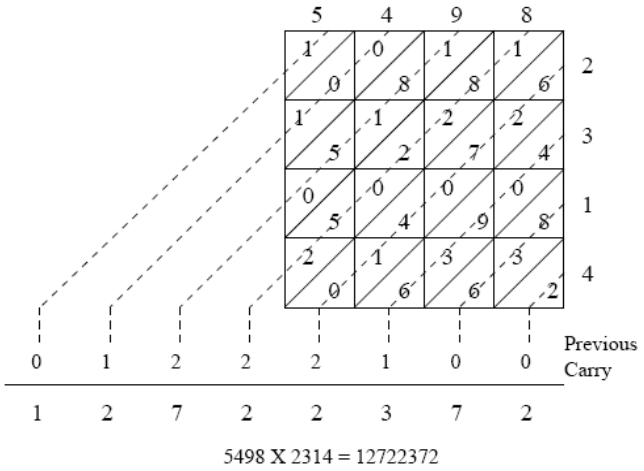

Figure 3. Multiplication Implementation Using Urdhva Tiryakbhyam Sutra [1]

Vedic Multiplier for 16x16 bit

The architecture of 16X16 Vedic multiplier using Urdhva Tiryagbhyam Sutra is shown in Figure 4. The 16X16 Vedic multiplier architecture is implemented using four 8x8 Vedic multiplier modules and two16 bit binary adder stages. The resultant output is given as,

X×Y=(Z3 1-Z1 6)&(Z1 5-Z8)&(Z7-Z0)

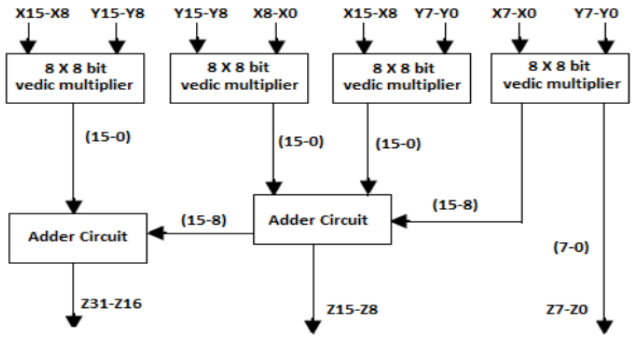

Figure 4. Hardware Realization of 16x16 Bit Multiplication Using Urdhava Tirya Kbhyam Sutra [14]

Figure 5 shows the proposed convolutional encoder design using vedic multiplier.

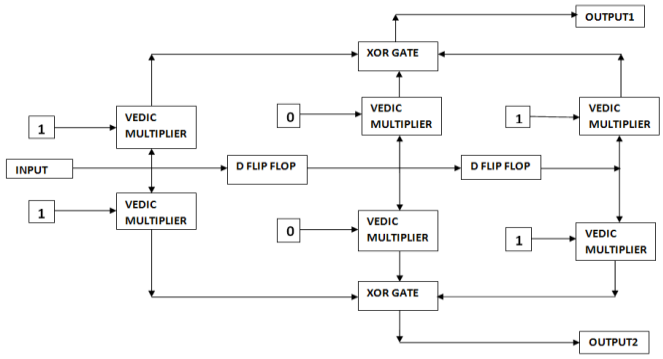

Figure 5. Block Diagram of Convolution Encoder Using Vedic Multiplier

Here, Six Vedic multipliers are used, which are used for multiplication of two numbers, one number comes from the input of convolution encoder as a input stream and second number is as a input of Vedic multiplier. All the Vedic multipliers output is given to XOR gate. The function of XOR gate is to perform XOR operation. The function of D flip flop is when clock is '1' then it gives output, otherwise no output is obtained. Finally, the circuit gives two outputs as Output1 and Output2.

IV. EXPERIMENTAL RESULTS

Figure 6 shows RTL VIEW of Convolution Encoder using 16Bit Booth Multiplier. Here, Six Booth Multipliers are used in Convolution design and two XOR gates are used. This design shows single input stream and two outputs, which proves that 'k' is less than 'n'.

RTL VIEW

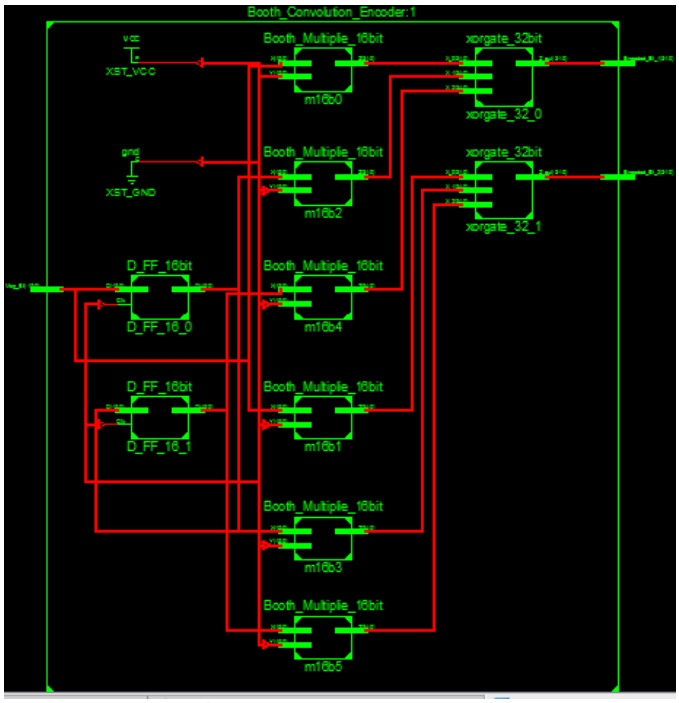

Figure 6. RTL View of Convolution Encoder Using 16-bit Booth Multiplier

Figure 6 shows RTL VIEW of Convolution Encoder using 16-Bit Booth Multiplier. Here, Six Booth Multipliers are used in Convolution design, two D-f/f and two XOR gates are used. This design also shows single input stream and two outputs, which proves that 'k' is less than 'n'.

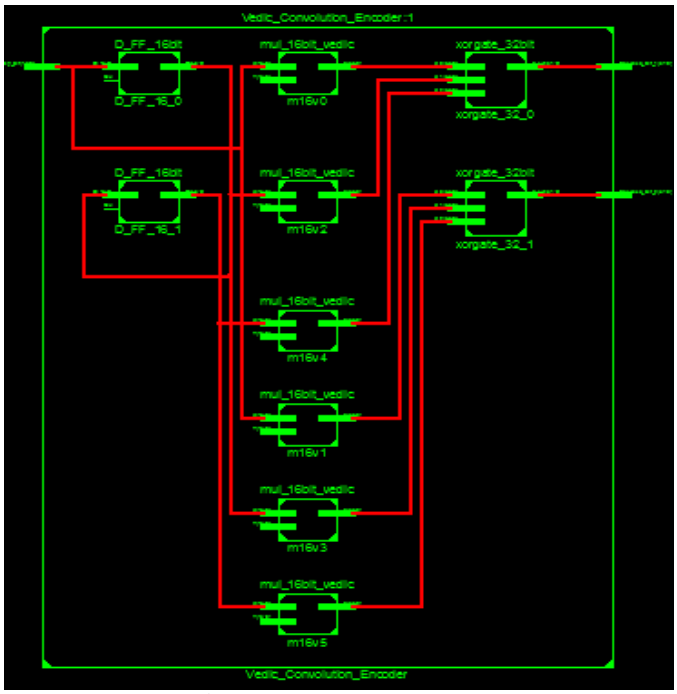

Figure 7. RTL View of Convolution Encoder Using 16-bit Vedic Multiplier

Figure 7 shows RTL VIEW of Convolution Encoder using 16Bit Vedic Multiplier. Here, Six Vedic Multipliers are used in Convolution design and two XOR gates are used. This

design also shows single input stream and two outputs, which proves that 'k' is less than 'n'.

SIMULATION RESULT

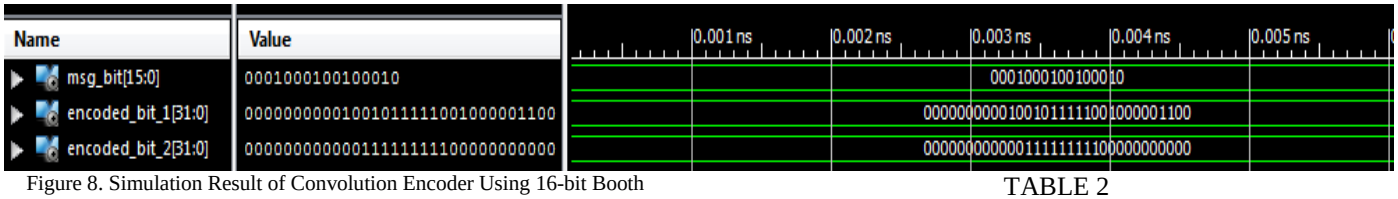

Figure 8. Simulation Result of Convolution Encoder Using 16-bit Booth Multiplier

Figure 8 shows simulation result of Convolution Encoder using 16-bit Booth Multiplier. Here, message bit (msg_bit) is considered as input stream of 16-bit, which gives two outputs encoded_bit_1 and encoded_bit_2 as 32-bit.

Figure 9 shows simulation result of Convolution Encoder using 16-bit Vedic Multiplier. Here, message bit (msg_bit) is considered as input stream of 16-bit, which gives two outputs encoded_bit_1 and encoded_bit_2 as 32-bit.

Table 1 below shows the delay comparison between booth multiplier and Vedic multiplier which shows that Vedic multiplier is more efficient than booth multiplier for multiplication of 4-bit, 8-bit as well as 16-bit. The multiplier can perform multiplication of higher bits and for that purpose multipliers based on booth algorithm and Vedic formulas will be design using the same approach.

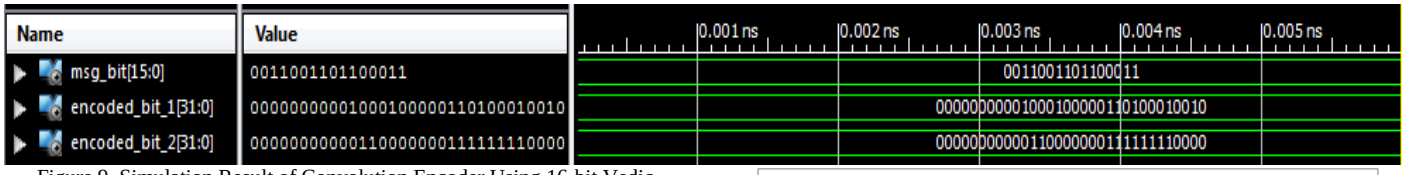

Figure 9. Simulation Result of Convolution Encoder Using 16-bit Vedic Multiplier

TABLE 1

No. of Bits	Structural Code	
VERTEX 6	Vedic	Booth
4X4	4.643 ns	19.260 ns
8X8	9.401 ns	18.316 ns
16X16	15.276 ns	609.278 ns

Table 2 below shows the delay comparison between convolution encoder using booth multiplier and convolution encoder using Vedic multiplier which shows that convolution encoder using Vedic multiplier is more efficient than convolution encoder using booth multiplier for encoding of 4-bit, 8-bit as well as 16-bit data. The convolution encoder can work on higher bits and for those purpose convolution encoders based booth and Vedic multipliers will be design using the same approach.

TABLE 2

No. of Bits	Structural Code	
VERTEX 6	Vedic	Booth
4X4	1.022 ns	25.480 ns
8X8	4.740 ns	65.728 ns
16X16	8.429 ns	456.441 ns

Figure 10 below shows the delay comparison between booth multiplier and Vedic multiplier in graphical form.

From the graph it has been shown that Vedic multiplier is more efficient than booth multiplier, as it is designed by using Vedic sutra from ancient Indian mathematics and the booth multiplier has been designed by using booth algorithm. It shows that logic capabilities of any system make the system faster as compare general systems. So, Design of convolution encoder using Vedic multiplier is a necessary choice.

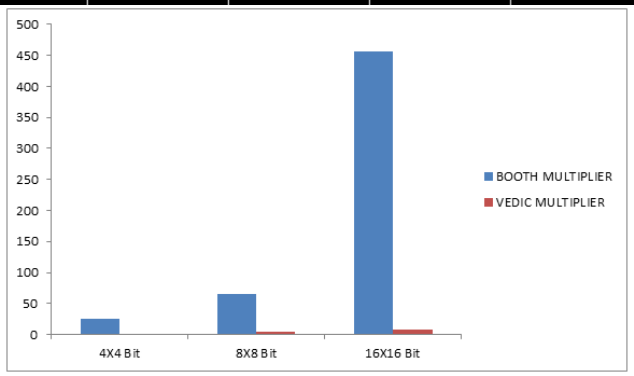

Figure 10. Comparison Between Booth Multiplier And Vedic Multiplier

Figure 11 below shows the delay comparison between convolution encoder using booth multiplier and convolution encoder using Vedic multiplier in column graph.

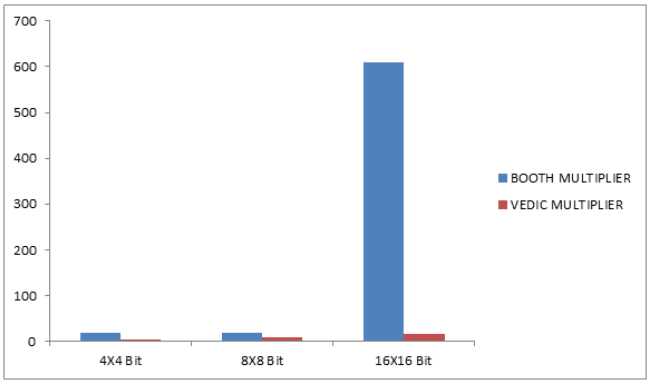

Figure 11. Comparison Between Convolution Encoder Using Booth Multiplier And Vedic Multiplier

V. CONCLUSION

In this research, we have presented the design and simulation of the Convolution encoder using booth multiplier and Vedic multiplier. This design has been synthesized and simulated on VERTEX6 using XILINX 13.1i ISE Simulator. The combinational path delay obtained for 16-bit convolution encoder using Vedic multiplier is 8.429ns and using booth multiplier is 456.441ns, this comparison shows that convolution encoder using Vedic multiplier is more efficient than convolution encoder using booth multiplier. Power supply obtained is 1.295W. This proposed architecture is efficient in speed and area (1ess resources used, such as less number of multipliers and adders) and is Flexible in design. For example, the same architecture can be extended for 32-bit, 64-bit, etc multiplication.

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Authors Profile

Miss. Shreyasi P. Bhat was born in Wardha, India on 23rd October 1989. She received her Bachelor Degree in Electronics and Telecommunication Engineering, from RTMNU University, Nagpur, Maharashtra, India in the year 2012. Currently she is doing M.TECH.in VLSI DESIGN from, BDCE, Sevagram, RTMNU, Nagpur, Maharashtra, India. She has Research Publications in various International Journals. Her interested areas of research are Computer Networks, Digital Electronics and VHDL.
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Mr. Ravindra D. Kadam Was born in Maharashtra on 5th day of Feb 1972.He received Bachelor of Engineering & M tech in Electronics from Bapurao deshmukh college of Engineering Affiliated to RTMNU, Nagpur. He has a

teaching experience of 13 + years, he also has an industrial experience of about 1.5 years. Currently he is working as Asst. Prof (Sr. Scale) in the department of Electronics & Telecommunication at B.D College of Engineering, Sevagram Wardha. He has taught various subjects for UG as well as PG. He has guided number of projects at UG & PG level .He has around 9 papers in various international conferences around the world. He also has 2 publications in international journals. His areas of interest are VLSI, VHDL and wireless communication.

Mr. Prashant R. Indurkar was born in Maharashtra. He received Bachelor of Engineering & M-tech in Electronics form RTMNU, Nagpur. He has a teaching experience of 21 + years .Currently he is working as Associate Professor in the department of Electronics & Telecommunication at B.D College of engineering, Sevagram, Wardha. He has taught various subjects for UG as well as PG. He has guided number of projects at UG & PG level. He also has research publications in international journals around the world. His areas of interest are Digital, Embedded System.