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Design and Analysis of Charge Pump for PLL Applications using 70nm Technology

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***Abstract*—This paper presents a CMOS Charge Pump using 70nm technology that operates at 0.7V. The proposed circuit has simple symmetric structure and provides more stable operation deals with different approaches to design a high speed CMOS charge pump circuit for PLL application. A charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Its frequency range is 500MHz to 1GHz.Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO.**

Keywords—charge pump, PFD, loop filter, phase-locked loops (PLL).

I.INTRODUCTION

A charge pump IC converts, and optionally regulates, voltages using switching technology and capacitive-energy storage elements. Charge pumps offer high-efficiency and compact solutions for applications with generally low-output current requirements. Charge pump maintain constant output with a varying voltage input. A charge pump based Phase lock loops (PLL) are widely used as a clock generator in a variety of applications including microprocessor, wireless receivers, and disk drive electronics [3]. As technology changes, our demands are also increases, high speed, portable and low power consumption communication system has become increasingly day by day. These systems require high-precision local clock generator (local oscillator) and difficulty is deal with the help of PLL circuit design. Due to the irreplaceable advantages, this technology is most widely in CMOS charge pump phase lock loop (CPLL). CPLL is a very simple and efficient method of designing PLL having low jitter and low power, zero static phase error and high speed [14]. The charge pump circuit is the heart of PLL. The charge pump (CP) based PLL is the most popular architecture. The CP-PLL derives its name from the fact that the phase detector (PD) output is a current source as opposed to a voltage source and "pumps" current into and out of the loop-filter. This form of PLL is popular because it is adaptable to integration in microcircuit devices. This type of the CPLL consists of a phase frequency detector (PFD), a CP, a passive loop filter (LF), and a voltage controlled oscillator (VCO). In a PLL the phase difference between the reference signal (often from a crystal oscillator) and the output signal is translated into two signals – UP and DN. The output of the PFDis fed to a charge pump circuit to get a constant current at the output. The charge pump output is passed through a low pass filter to generate the control voltage for the VCO circuit. Figure1 show block diagram of PLL [3].

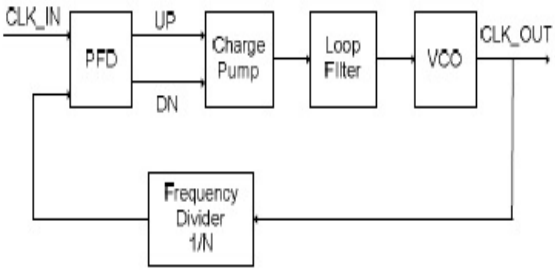

Figure 1: Phase Locked Loop

Hence there are five functional blocks in a PLL circuit such as phase frequency detector (PFD), Charge Pump, loop filter, voltage controlled oscillator (VCO) and frequency divider.
In this paper explain Charge Pump circuit and also taken result of many research worker.

II.OVERVIEW OF BASIC CHARGE PUMP

A charge pump is a three position electronic switch which is controlled by the three states of PFD. Current sources I_1 and I_2 are identical. Two outputs of PFD QA and QB are given to the X and Y inputs of charge pump (CP) respectively. Capacitor Cp serves the purpose of loop filter. Figure 2 shows the combined architecture of the charge pump and loop filter [6].
If QA=QB=0, then S1 and S2 are off and Vout (or Vcont) remains constant. If QA is high and QB is low, then I_1 (UP current) charges Cp. Conversely if QA is low and QB is high, then I_2 (DOWN current) discharges

Cp. Hence, if suppose, A leads B, then QA continues to produce pulses and V_{out} rises steadily.

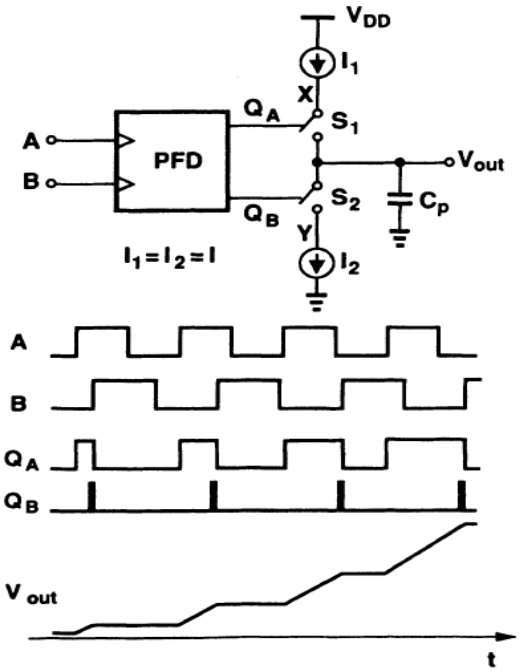

Figure 2: PFD-CP-Loop Filter Combination

III. PROPOSED CHARGE PUMP DESIGN

There are number of charge pump circuits were designed to reduce jump phenomenon and current mismatch. The proposed circuit is low voltage and increases the performance of the charge pump.Improved charge pump circuit is shown in figure 3.

First when the signal UP is at a high logical level transistor P1 is off, and the current I_{UP} is steered to transistor P2. Since the power supply is 0.7V, when transistor P2 is ON, transistor P4 will not have enough voltage headroom between its gate and source to be ON.Since transistors P2 and P3 form a current mirror, a current I_{UP} will be pushed into the capacitor C, raising the voltage $V_{C.}$ Now when the signal UP is at logical zero transistor P1 and P4 turn ON. The current steered in P2 and therefore P3 negligible. The voltage at the capacitor should, ideally remain stable. P5 and N1 are used to pre-discharge to the gate of P3. When the UP signal is switched from 0 to 1, the charging time of P3 is relatively long, which result in delaying open speed of P3. So to overcome this problem, P5 and N1 are taken advantage at the gate of P3. Then the voltage at the gate of P3 is rapidly pulled down once the UP signal switches from 0 to 1 opening P3 in a much shorter time. In other hand DN=1 pull-down network is ON and the capacitor C_P will be discharged.

When they are both ON, they operate in the saturation region. So to carry same currents, P5 and N1 have to be perfectly matched.

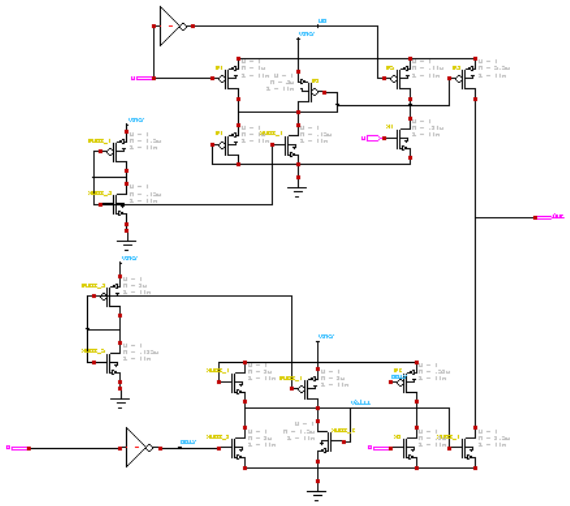

Figure 3: Propose Charge Pump

IV. PROPOSED PFD

The PFD circuit is used to find the difference in phase and frequency between the two input signals reference frequency and input frequency which is feedback from the output of the VCO. The PFD generates two output signals UP and DOWN that switches the output current of the pump. PFD circuit generally implemented using D flip-flops (DFFs). The output of the PFD depends upon both phase and frequency of the input signals. Initially both the signals will be low. When one of the PFD input rises the corresponding output becomes high. The simulationswaveforms are shown in fig. the diagram of PFD are shown below in fig.4 (a) which is implementing on Tanner Tool.

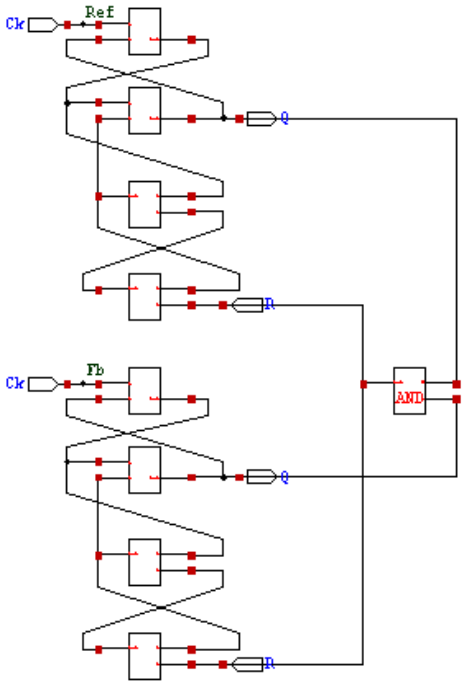

Figure 4(a): PFD using DFF

UP and DOWN signals generated by the PFD are shown in fig 4(b). PFD is simulate using tanner tool, and the supply voltage is 0.7V.

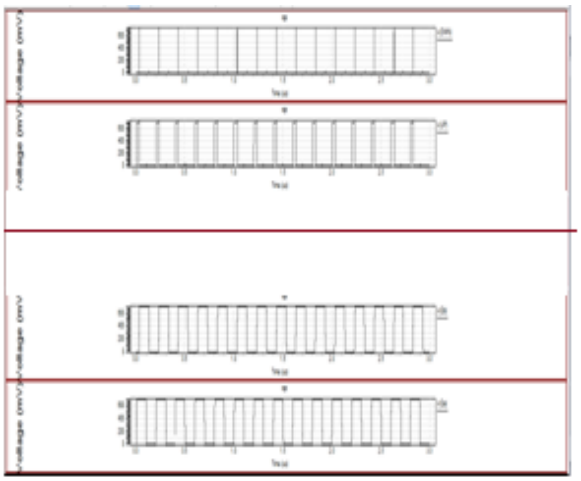

Figure 4(b): Up and Down Signals

V. SIMULATION RESULTS

The proposed charge pump was designed using 70nm CMOS technology. All results are reported are with a 0.7V power supply. Simulations were done using Tanner tool. The pull UP current I_1 and pull down current $I_2$are both set to 70µA.the operating frequency is 500MHz.

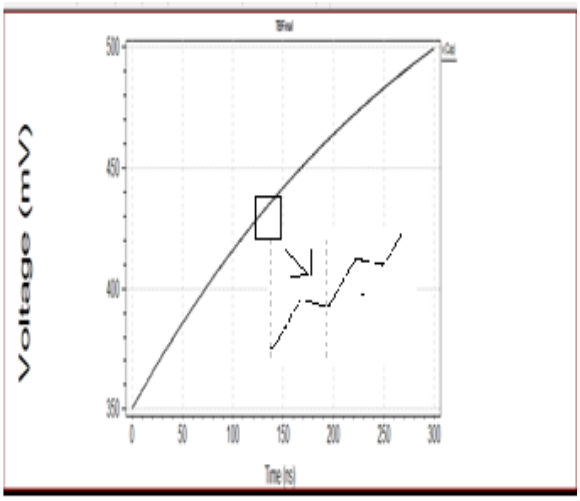

Figure 5: Pumping Up the Output Voltage

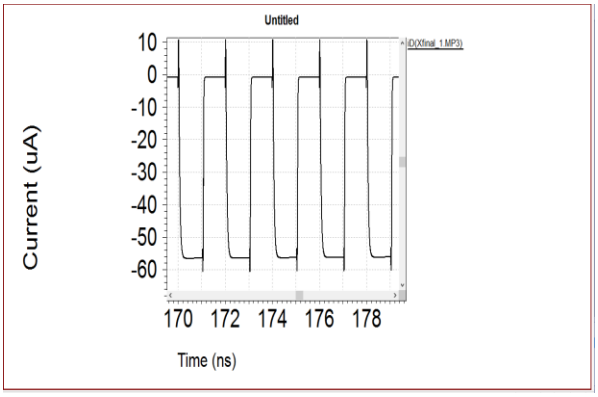

Figure 6: UP current when charging the capacitor

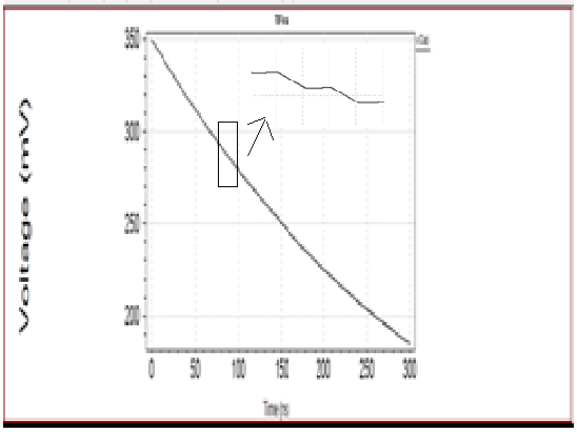

Figure 7: Pumping Down the Voltage

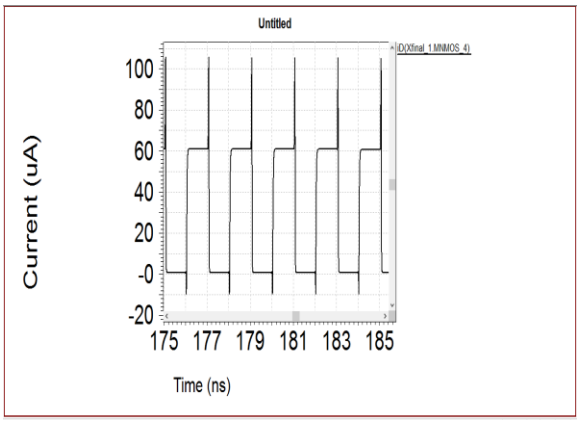

Figure 8: Down Current When Discharging the Capacitor

Table I
PERFORMANCE SUMMARY

Parameter	Results
Technology	70nm
Power supply	0.7V
Frequency	500MHz to 1000MHz
Power consumption	0.41mW
Output voltage	200mv to 500mv
Up and down Current	70µA

VI. CONCLUSION

We are presented a new charge pump circuit, optimized for very low voltage PLL applications. The circuit was designed using 70nm technology. It operates from a lower power supply voltage 0.7V, compared to recently reported designs. Simulation results showed that the circuit is suitable for high frequency operation (500MHz to 1GHz) with lower power consumption 0.41mW).This circuit is implementing using Tanner Tool.

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