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Design And Implementation Of An Fpga-Based Real-Time Very Low Resolution Face Recognition System

1C.Senthilsingh , 2 M.Manikandan.
1C.Senthilsingh , Research Scholar, Department of Electronics, MIT, Chennai
2Dr.M. Manikandan Associate Prof., Department of Electronics , MIT, Chennai

***Abstract*-Face Recognition is a successful application of Image analysis. There are atleast some reasons for such trend: VLR(Very Low Resolution) problem. VLR problem happens in many face application systems. Existing algorithms performance is not satisfactory. To overcome the VLR problem, this paper proposes an approach to learn relationship between the high resolution space and the VLR image space for face. Based up on the new approach the face recognition applications under the VLR problem is designed for good visuality. The code will be developed in Verilog using Modelsim and then implemented on Virtex5 FPGA kit. The proposed system provide both highly accurate and extremely fast processing of the image data.Experimental results show that proposed method outperforms existing methods.**

Keywords-Very Low Resolution, Super Resolution, relationship-learning based SR , High Resolution, Low Resolution

I.INTRODUCTION

A facial recognition system is an application for automatically identifying or verifying a person from a digital image or a video frame. One of the ways to do this is by comparing the face features from [1]the image and a facial database. [2] have been implemented to carry out this application. In this applications camera is installed in a way but the viewing area is maximized but the face region is very small. To recognize a face from camera,it is to handle low resolution face image with variations such as pose, illumination and occlusion. An Algorithm[1] is proposed for Super Resolution(SR) for face image. By applying this Algorithm, the low resolution face image is reconstructed into high resolution face image. But this algorithm works well when the image is in good illumination.

When a person is not close to the camera then the resolution for the face image is less than 16x12 pixels its showed in fig.1.In the above figure it gives limited information and many information is lost.

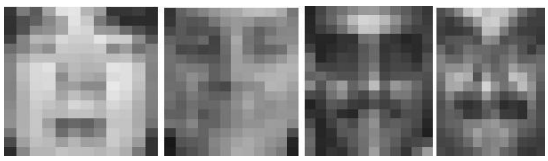


Fig.1 Face image

Working on such kind of problem is called as Very Low Resolution(VLR) problem. To solve this problem lot of Super Resolution Algorithms [6][9][10][11] are proposed. But the existing super resolution algorithms may not be employed under the VLR problem.To solve the VLR problem is to recover the missed information of the face image. Existing algorithms are classified into two approaches namely maximum a posteriori and example-based approaches[2].Both these approaches perform error evaluation for the reconstructed HR images, which is called a data constraint[3]. But the data constraint is used for comparing the images by calculating the distance in the low-resolution image space for Super Resolution Processing. Baker and Kanade's method[4] works well if the distance metric in the VLR image space reflects the actual face similarity in the HR image space.This paper proposed a technique ,relationship-learning based SR(RLSR) approach for solving the VLR problem.

II.STEPS IN FACE RECOGNITION

The generic face recognition system consist of three main processing steps as shown in fig.2.

i) Face detection that involve detecting and separation of the face region from submitted face image or video (which is an image sequence). ii)Feature extraction which identifies and extract features of the submitted images. Features can be local features such as lines or fiducial points, or facial features such as eyes, nose, and mouth.iii)Recognizing faces by matching input image against the faces in database.

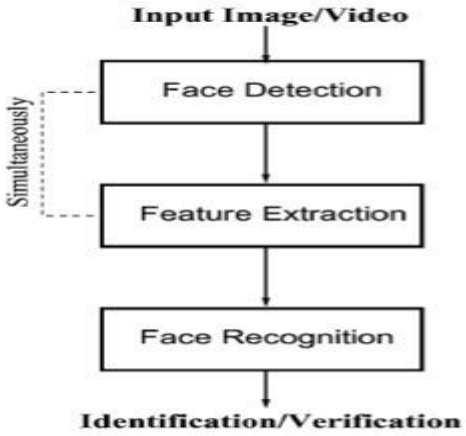
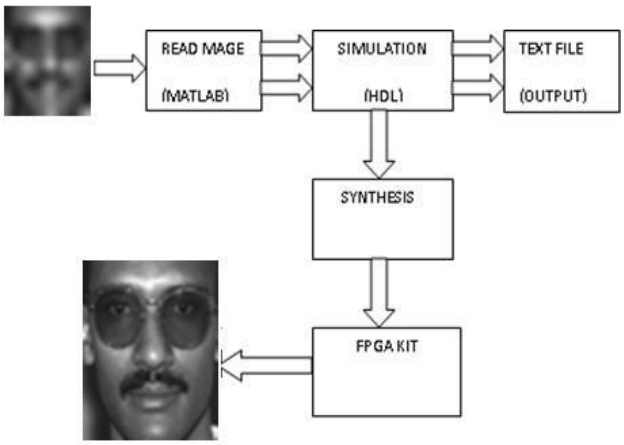


Fig.2 Configuration of a face recognition system

The face recognition system is classified into two types,i)Global approaches-the whole image serves as a feature vector.Its also analyzing the statistical properties of the face based on a large set of training images ii)Feature based face recognition-a number of fiducial or control points are extracted and used for classification.

III.DESIGN METHODOLOGY



A.Matlab Image Reading

This is a simple image reading and resizing module written in MATLAB. It reads two images from database for comparison. One of which is High Resolution(HR) image and another having noise image (i.e.)Low Resolution(LR) image. The two image file will generate a test input file which we can use as input to Verilog module.

B. RLSR Algorithm

Using this proposed algorithm it makes use of the information available during the training phase and proposes a new learning-based face SR approach. Most of the existing methods recover the images directly from the VLR images and the training images. This algorithm first determines relationship between VLR and HR image spaces and then applies it on VLR images to recover the HR ones. The proposed new approach offers additional advantages. The SR algorithm can recover images with more details and handle the VLR problem better.The linearity clustering ensures data linearity in each cluster. The linearity clustering-based relationship learning method can handle complex nonlinear case. The determined relationship, R is generic for all VLR testing face images.

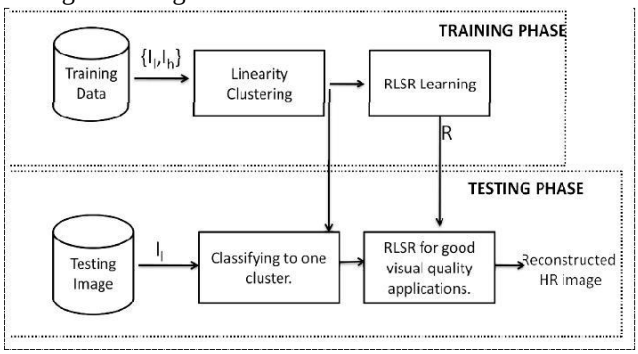


Fig.3 Block Diagram of RLSR

1.Training Phase

In the fig.3 the training phase consists of two steps namely, linearity clustering and relationship learning. In the first step, a clustering algorithm is proposed as a preprocessing step. After clustering, the Very Low Resolution (VLR) –High Resolution (HR) image pairs in each cluster are nearly linear, i.e., the relationship can be approximately represented by a matrix. In the second step, the relationship mapping from the VLR to the HR face image spaces within the cluster is determined.

A standard High Resolution database is used. All the images are taken against a bright homogenous background with the subjects in an upright, frontal position. The files are in JPEG

format. The size of each image is 16 x 12 pixels, with 256 grey levels per pixel. Both male and female subjects are present in this database. To create the Very Low Resolution (VLR) image corresponding to each of these High Resolution (HR) images, the HR images are resized to 64 x 48 pixels.

2. Linearity Clustering

Clustering is the task of assigning a set of objects into groups (called clusters) so that the objects in the same cluster are more similar to each other than to those in the other clusters. The appropriate clustering algorithm and parameter settings depend on the individual data set and the intended use of the results. Here, a linearity clustering algorithm is proposed to ensure that the clustered training image pairs have a linear relationship. This clustering algorithm reduces the complexity of the relationship learning process. The block diagram shows the steps involved in the clustering algorithm.

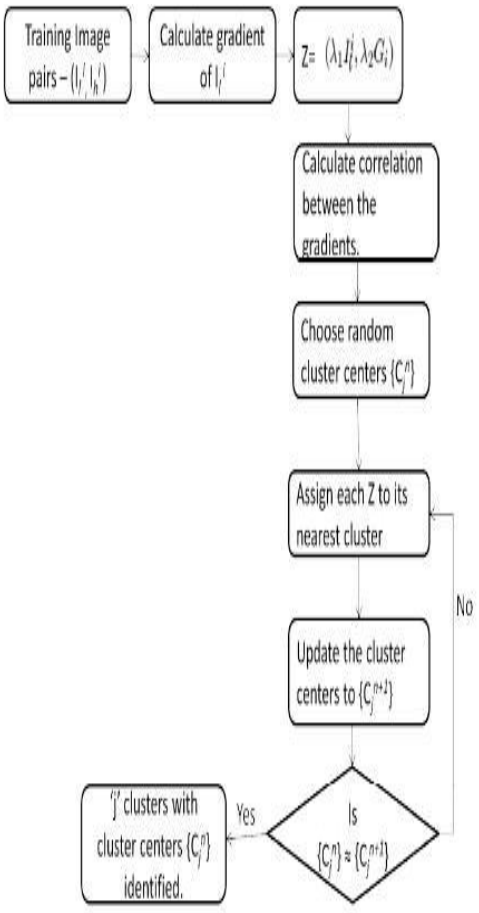


Fig.4 Block Diagram of Clustering Algorithm

The clustering algorithm utilizes the following two parameters :(a) The gradient of the low resolution image(b) The low resolution image. The contribution of the above two parameters is balanced by two constants – $\lambda 1$and $\lambda 2$.

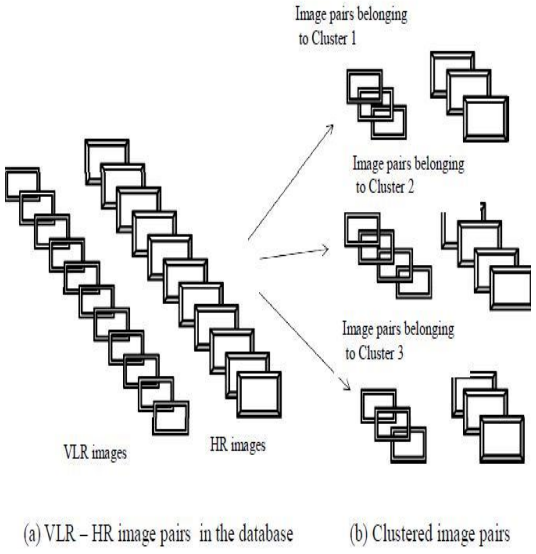


Fig.5

Fig.5 (a) depicts the HR images paired with their corresponding Very Low Resolution image in the database. Once subjected to the linearity clustering algorithm, the images showing maximum similarity between their gradients are clustered together. This is depicted in fig.5 (b)

3.Relationship Learning

Each cluster now holds the training image pairs i.e., VLR-HR image pairs that have a linear relationship. Let *R* be the relationship mapping between between the VLR to HR face image spaces within the cluster, then I*hi* = *R* (I*l i*). After determining R, the HR image can be recovered by applying R on the VLR image. After clustering, a matrix R is used to represent relationship mapping *R*. The relationship being represented as above, from the image pair in each of the cluster, the relationship operator R can be derived as R=inverse(LR) * HR. From this, the relationship matrix corresponding to each of the image pair is determined. The linear clustering aids in obtaining a unique relationship operator for each of the cluster. So, the relationship operators of the images in a particular cluster are extracted. The relationship operator corresponding each cluster – Rcluster is selected such that reconstruction error is minimum.

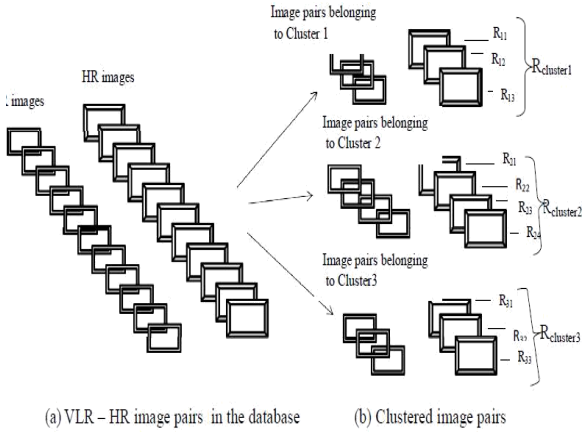


Fig.6 used to generate $R_{cluster}$

Fig.6 gives a pictorial representation of how the unique relationship operator - Rcluster, corresponding to each cluster is obtained. The straight forward method for this is minimising the reconstruction error. The reconstruction error is measured in the HR image space by the data constraint *e* R.

$$\mathbf{eR(Ih) = ||Ih – Ih'||}$$

Here, *Ih* and *Il* represent the HR and VLR image respectively.A minimum mean square error is employed to learn R is represented as

$$\mathbf{minR\ 1/N\ \Sigma\ ||\ Ihi– RIli||}$$

Utilizing the above two equations in the learning process ensures that the Rcluster chosen incurs minimum reconstruction error. Another mechanism used to choose the optimum Rcluster is by computing the average of the relationship operators belonging to each cluster.

4.Testing Phase

The test image is of dimensions 16 x 12 pixels with 256 gray levels in each pixels i.e., a VLR image is given as the test image. The gradient of this image is then calculated as *Gtest*. Since the parameter of the linear clustering algorithm is used in the training phase is the gradient, *Gtest* can be used to classify the VLR image into the appropriate cluster '*i*'. Once the cluster '*i*' is identified, the corresponding the R *cluster-i* is applied on the input testing image. The linearity of the clustered data pairs is equivalent to minimizing the difference of the gradient between the data pairs.

IV. SIMULATON RESULTS

The modules are designed using verilog as stated above and they are simulated within the Xilinx ISE 9.2i based Model Sim 6.3g environment.The Figure 7 shows the Simulation results of Clustering basd on linearity and stored the data in the RAM. Figure 8 shows the input and output of the image with simulation.

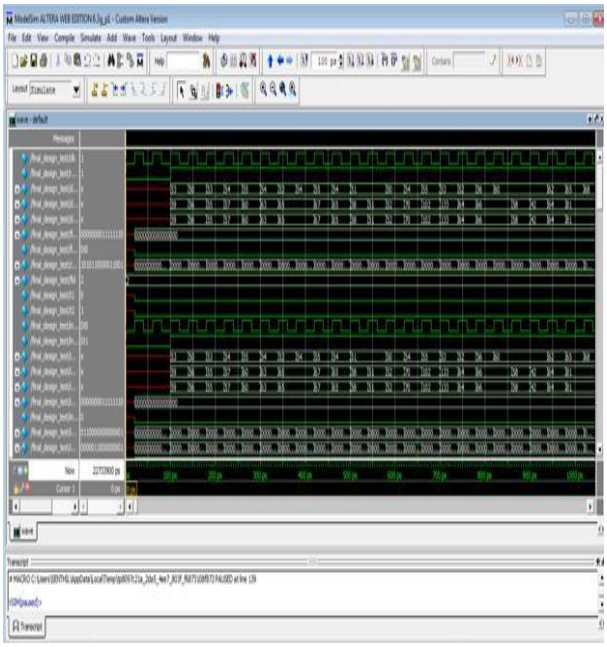


Fig.7 Clustering Based on Linearity

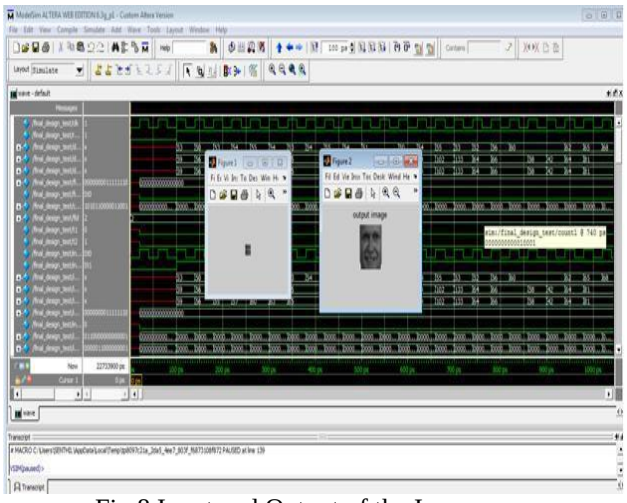


Fig.8 Input and Output of the Image

A.FPGA Implementation

The top order module, is synthesized within the Xilinx ISE 9.2i based Model Sim 6.3g software tool and it is programmed to the targeted Xilinx Virtex5 family of FPGA Device. The various levels of implementation such as Synthesis report, RTL View, Place and Route Report and Device Programming has been explained and visualized in the following sub sections.

B.Synthesis Report

The Table 1 shows the synthesis Summary of top order module. It is observed from the Table 1 that the total equivalent gate count required for this design is 2316547gates. From the same table we can get the information about the target FPGA device utilization.

Number of BlockRAM/FIFO	16	32	50%	
Number using BlockRAM only	16			
Total primitives used				
Number of 36k BlockRAM used	16			
Total Memory used (KB)	576	1,152	50%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Total equivalent gate count for design	2,316,547			
Additional JTAG gate count for IOBs	2,448			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Thu Nov 15 12:03:51 2012	0	328 Warnings	49 Infos
Translation Report	Current	Thu Nov 15 12:03:55 2012	0	0	0
Map Report	Current	Thu Nov 15 12:05:15 2012	0	3 Warnings	7 Infos
Place and Route Report	Current	Thu Nov 15 12:05:44 2012	0	0	3 Infos
Static Timing Report	Current	Thu Nov 15 12:05:54 2012	0	0	3 Infos
Bitgen Report					

IMG_PROCESS.twx | Design Summary

Table 1: Synthesis Summary

C. RTL View

This section gives the visualization of Resister Transistor Logic (RTL) views in the form of schematic diagrams which are shown in Figure 9 respectively. Figure 9 which gives RTL schematic diagram reveals the pin diagram of Top order module with the equired specified notes .

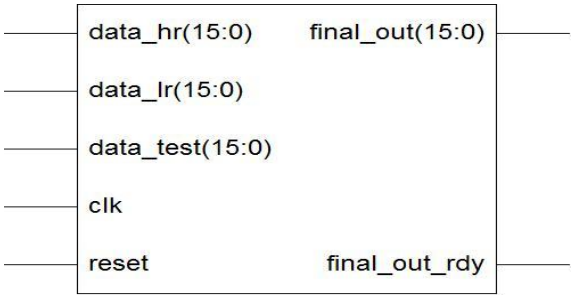


Fig.9 RTL Schematic diagram

D. Place and Route Report

This section concentrates on target FPGA device utilization summary which reveals the information required for proper layout at the level of manufacturing in the form of Place and Route report. Further it gives the timing synchronization of CPU with the REAL time environment

1.Device Utilization Summary

Number of Slice Registers : 302 out of 19200 1%

Number of Slice LUTs : 2643 out of 19200 13%

Number used as Logic : 1011 out of 19200 5%

Number used as Memory : 1632 out of 5120 31%

Number used as RAM : 1632

Minimum period : 4.831ns (Maximum Frequency: 207.009MHz)

Minimum input arrival time before clock : 2.163ns

Maximum output required time after clock: 4.013ns

E. Device Programming

After successful process of synthesis the Target device xc5vlx30-3ff324 of Virtex5 is connected to the system through USB port. The pin assignment is specified in the User Constraint File (UCF). The functional verification is carried out by using a pattern generator.

IV. CONCLUSION

In this paper the VLR face recognition problem has been defined and discussed . For good visual quality applications, a new data constraint that measures the error in the HR image space was developed, and RLSR was proposed.Experimental results show that as the number of clusters in the algorithm increases. The results obtained are more visually satisfactory.Results also show that the relationship operator obtained from averaging the relationships in each cluster consumes less time than the relationship operator got by minimizing the reconstruction error, but, at the cost of over learning.

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