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Carry-Save Arithmetic Using Generalized Parallel Counter

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Abstract-Carry-save arithmetic occurs naturally in a variety of DSP application. "field programmable counter array" (FPCA), an accelerator for carry-save arithmetic intended for integration into an FPGA as an alternative to DSP blocks. In addition to multiplication and multiply accumulation, the FPCA can accelerate more general carry-save operations, such as multi-input addition and multipliers that have been fused with other adders. A set of arithmetic-oriented data flow transformations that can be applied to a computation in order to maximize the use of carry-save arithmetic. Each cluster of adders is then replaced with a compressor tree. It is reduces n integers , down to two, sum and carry.A carry-propagate adder (CPA) has two-input adder, then performs the final addition, , to compute the result. FPCA accelerates a wider variety of applications than DSP blocks and improves performance, area utilization, and energy consumption.

***IndexTerms*—Carry-save arithmetic, field-programmable gate array (FPGA), generalized parallel counter (GPC).**

I. INTRODUCTION

FPGA performance is lacking for arithmetic circuits. Generally, arithmetic circuits do not map well onto lookup tables (LUTs), the primary building block for general logic in FPGAs. To address this concern, FPGAs offer two solutions: First, LUTs are now tightly integrated with fast carry chains that perform efficient carry-propagate addition; second, FPGAs contain DSP blocks that perform multiplication and multiply accumulation (MAC). Although an improvement over LUTs alone, these enhancements lack generality; specifically, they cannot effectively accelerate carry-save arithmetic.Carry-save arithmetic is a technique to add sets of numbers that eliminates much of the carry propagation that would otherwise occur. Carry-save arithmetic has been the method of choice for partial-product reduction in parallel multipliers for more than 40 years [1], [6]. More recently, [2] developed a set of arithmetic-oriented data flow transformations that can be applied to a computation in order to maximize the use of carry-save arithmetic.

These transformations systematically reorder the operations in a circuit in order to cluster disparate adders together and to merge adders with the partial-product-reduction trees of parallel multipliers. Each cluster of adders is then replaced with a *compressor tree*, i.e., a circuit that reduces n integers,Ao.A1……An-1 , down to two,S (sum) andC (carry), such that

$$S+C = \sum_{i=0}^{n-1} A_i$$

A carry-propagate adder (CPA), i.e., a two-input adder, then performs the final addition, S+C , to compute the result. Aside from the transformations of [2], compressor trees occur naturally in a variety of applications [3]–[4]. The arithmetic capabilities of FPGAs are not well attuned to the needs of carry-save arithmetic. Programmable LUTs have been augmented with fast carry chains that are good building blocks for CPAs but cannot be used for carry-save arithmetic. The fastest methods to synthesize compressor trees on FPGA general logic [5], [7] do not use the carry chains except for the final CPA.

FPGAs also integrate DSP blocks, which perform integer multiplication and MAC. Although useful, DSP blocks cannot accelerate multi-input addition; likewise, when the transformations merge multipliers with adders, the resulting operation can no longer map onto a DSP block. That being said, certain multiplication operations whose bitwidths do not match up well with the bitwidths of the DSP blocks are faster when performed on the general logic of an FPGA [8].

This paper advocates the use of a field programmable counter array (FPCA) for carry-save arithmetic on FPGAs. The FPCA is a programmable accelerator that can be integrated into an FPGA as an alternative to DSP blocks. An early FPCA, introduced[9] , is a lattice of m:n counters. An m:n counter is a circuit that takes m input bits, counts the number of them that are set to 1, and outputs the result, a value in the range [0,m], as an n-bit unsigned binary number. The number of output bits is

$$n=[\log_2(m+1)$$

The FPCA described in this paper, in contrast, is built using generalized parallel counters (GPCs) , an extended type of counter that can sum bits having different input ranks; GPCs are built using counters as building block

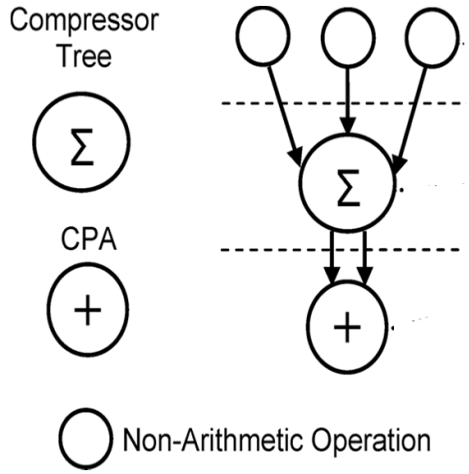


Fig. 1 shows our approach.A circuit transformed as described previously is partitioned into a (set ofcompressor tree(s) with corresponding CPA(s) and a set of nonarithmetic operations. The compressor tree is mapped onto an FPCA, which is embedded
within a larger FPGA.

II.RELATED WORK

A.Commercial FPGA Architectures and Mapping

This section summarizes the arithmetic features in the *Altera Stratix III* and *Xilinx Virtex-5* FPGAs, both of which are high-end FPGAs realized in 65-nm CMOS technology. The logic architectures of both of these FPGAs feature six-input LUTs with carry chains that perform efficient carry-propagate addition without using the routing network. The *Stratix III* carry chain is a ripple-carry adder; the *Virtex-5* carry chain includes an XOR gate and a multiplexor (mux) which enable carry-lookahead addition. *Stratix II* introduced a method to combine the LUTs with the carry chain to perform ternary (three-input) addition, which remained in place for the *Stratix III*; the *Virtex-5* similarly supports ternary addition. Due to the peculiar nature of FPGA architectures, it has long been thought that multi-input addition is best realized using trees of adders rather than compressor trees. The use of ternary adders rather than binary (two-input) adders could reduce the height of the trees, thereby reducing delay and/or pipeline depth.

B. FPGA Enhancements to Improve Arithmetic Performance

Numerous enhancements for FPGAs have been proposed in the past, particularly to improve arithmetic performance. For example, several researchers have proposed hard IP cores: application- specific integrated circuit (ASIC) components that implement common operations that are embedded into the FPGA. The most prevalent of these IP cores include block memories, Although the FPCA is similar in principle to the IP cores described previously, it is not completely hard: It is programmable and has its own routing network.

Although it is intended to implement just one class of circuits—compressor trees, the FPCA is flexible and is not fixed to a specific bitwidth; this distinguishes the FPCA,Recently proposed an alternative FPCA architecture. Theirs is radically different than the one described here; the most important distinguishing feature is that it uses direct programmable connections but does not employ a global routing network; as such, it offers less flexibility than the architecture proposed here, but with the potential of reduced delay, area, and power consumption due to the absence of global routing. Future work will compare and contrast these two architectures to better understand the differences between them.

III GPCs

A *generalized parallel counter (GPC)* is a counter that can sum bits having different ranks; all of the input bits of the same rank are referred to as a *column*. In principle, we could design a GPC that produces more than one output bit of each rank; to simplify our heuristic, however, we only consider GPCs that produce a single output bit of each rank. An *m:n* counter can implement a GPC by connecting all input bits of rank *i* to *2i* inputs of the counter. Of course, it is also possible to construct a GPC from basic gates as well; it turns out that *k*-input GPCs map quite well onto *k*-LUTs.

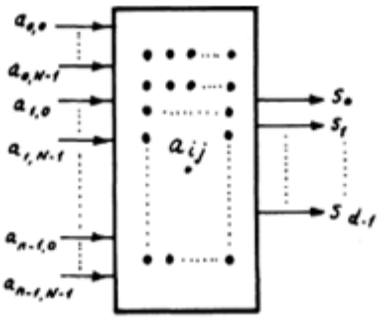


Fig. 2. (n X N; d) counter scheme.

We assume that a GPC has at most *M* input bits and *N* output bits. Formally, a GPC is a tuple: *(KN-2, KN-1, …, K0; S)*, where the output *S* is an *N*-bit number. There are *N-1* columns, from rank *0* to *N-2*, with *Ki > 0* input bits in the *ith* column.

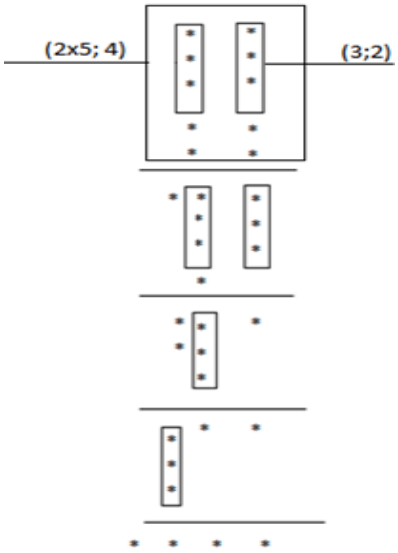


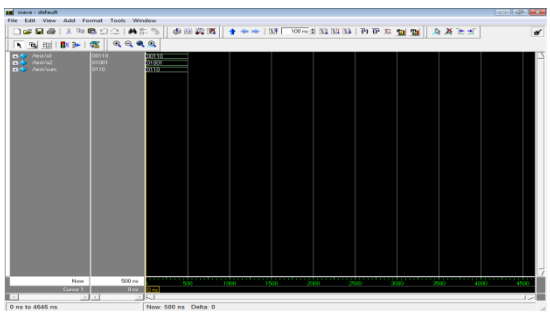
Fig.3. Synthesis of a counter (2x 5; 4)

Counters of this type are denoted as: (n X N; d) and are graphically represented as shown in Fig. 2.Equal columns consume a rectangular matrix segment of n columns by N rows. This type of counter (that they call a maximally efficient equal column counter) is very useful in the synthesis of parallel digital multipliers because in the reduction scheme it produces a uniform output matrix while consuming the largest possible regular portion of the input matrix.

Fig. 3 shows the reduction scheme for the construction of the generalized parallel counter (2 X 5, 4) using primitive networks (3;2) and it also shows the interconnections of these primitive networks.

IV RESULT

A scheme for generating generalized equal column counters from smaller ones has been described. The method proposed gives a specific extension and (2x5;4) counter was obtained using generalized parallel counter



V. CONCLUSION AND FUTURE WORK

The FPCA is a programmable IP core that can accelerate compressor trees on FPGAs. For parallel multiplication, the FPCA retains many of the advantages of the embedded multipliers in the DSP blocks; however, it suffers a disadvantage in terms of area utilization because the partial products must be synthesized on the FPGA general logic. For parallel multiplication, the FPCA retains most of the benefits of the embedded multipliers in the DSP blocks, while providing a variable-bitwidth solution for multiplication operations that do not match the fixed bitwidth of the DSP blocks. Moreover, the FPCA can accelerate multi-input addition operations, while the DSP blocks cannot, particularly when used in conjunction with transformations to expose compressor trees at the application level. Furthermore, the FPCA reduces the critical path delay and energy consumption compared to the best methods to synthesize compressor trees on the FPCA.

The DSP block will generally outperform the FPCA for applications containing many multiplications whose bitwidths match precisely that of the ASIC multipliers in the embedded DSP blocks and for which the transformations are ineffective. For virtually all other applications that contain compressor trees—naturally or via transformation, the FPCA performs
significantly better than current FPGAs.

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