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Architecture Of 512 Bit Csla

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Abstract:
The design of a 512-bit CLSA to achieve minimum delay and low power requirement is presented in this paper**.**Adder is the basic block of every digital operation. All other arithmetic operations such as subtraction, multiplication and division are based on the addition operation.But carry generation is difficult in the design of adders. Power dissipation is one of the most important design objectives in integrated circuits, after speed.Depending on the delay and power dissipation requirements, several adders blocks using in architecture such as carry look-ahead (CLA), carry-skip adder (CSA) and ripple carry adder (RCA). In this paper RCA is used for design of high speed and low power require architecture. By using different form of D-latch structures we obtain this CSLA.

1.**INTROTECTION:**

In the most of digital signal processing (DSP) applications based on the operations of the adder, multiplier and accumulator. Every digital operation depends upon the addition, such as DSP or control system. Therefore a fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also very significant component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. RCA is the basic block for my our paper . The normal carry select adder obtain by without using MUX. For a high performance mux are used in the architecture.Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders.Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas ofresearch in VLSI system design. In digital adders, the speed ofaddition is limited by the time required to propagate a carrythrough the adder. The sum for each bit position in an elementaryadder is generated sequentially only after the previous bitposition has been summed and a carry propagated into the nextposition.. The CSLA is used in many computational systems toalleviate the problem of carry propagation delay byindependently generating multiple carries and then select a carryto generate the sum.

2.**ADDER:**

The full adder is the basic block of RCA. An one bit full adder is shown in the below figure. There are three inputs for an one bit FA. From the full adder one sum and one carry are taken.

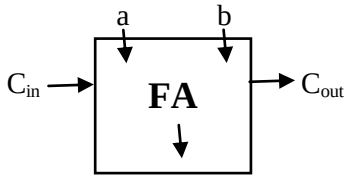


Figure 1. one bit full adder.

$sum=a \oplus b \oplus c$;

$C_{out=}(a.b)+(b.C_{in})+(a.C_{in})$.

3.**RIPPLE CARRY ADDER:**

The ripple carry adder block consist of number of full adders. 4-bit ripple carry adder shown in the figure. In the blocks the output carry the full adder given as the input of the next full adder. So from the RCA four sum bits and one carry bit taken as the output.

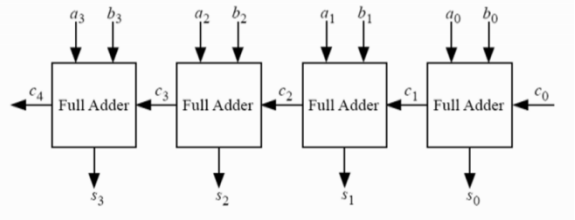


Figure 2. 4-bit ripple carry adder.

In the logic diagram of the RCA carry propagation delay and generation delay are consider ,they represented as P_i,G_i. The equations for delay of the each full adder is

c1=G0+P0.c0 ;

c2=G1+P1.G0+P1.P0.c0 ;

c3=G2+P2.G1+P2.P1.G0+P2.P1.P0.c0 ;

c4= G3+ P3.G2 + P3.P2.G1 + P3. P2.P1.G0 + P3.P2.P1.P0.c0 .

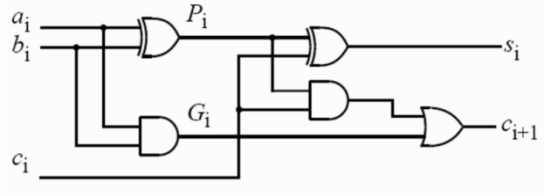


Figure 3. FA logic gates circuit used in RCA.

4. LATCH:

D-latches are also used in the CSLA architecture. Latch when D-Latch en=1 the input to the d-latch pass transistor should be D and when en=0 the input to the pass transistor should be value of D just before the transition of clock from 1 to 0.

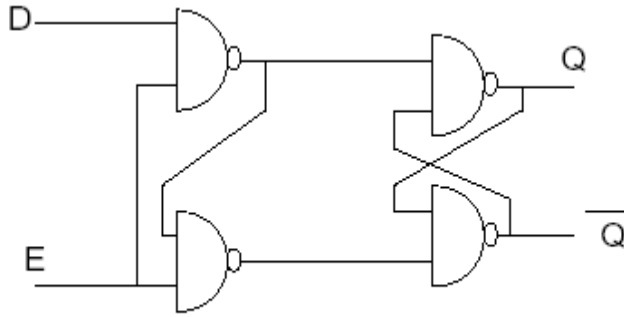


Fig.1D-Latch

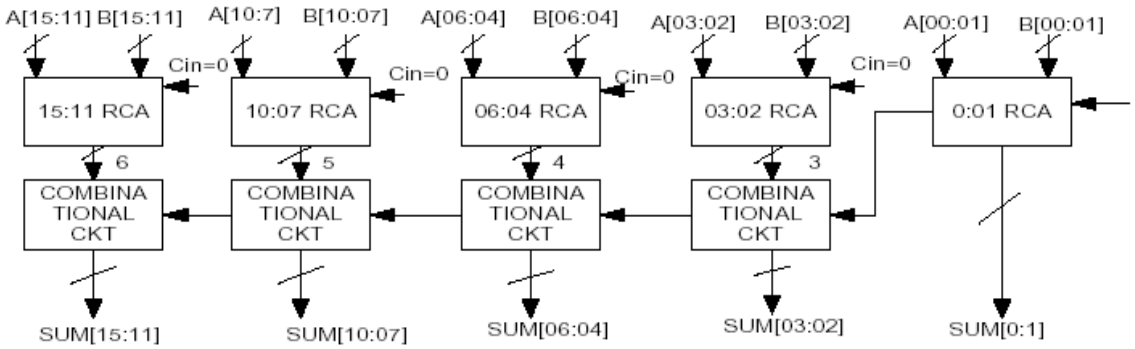
A single enable D-latch shown in the figure. In this D-latch circuit single enable and single input given. The basic gates of the D-latch is NAND gate . There four NAND gates are used in the 1D-latch.

As from figure enable is common input for first two gates.

5. MODIFIED 16-B SQRT CSLA (WITHOUT USING MUX):

In this method CSLA with cin=1 and multiplexer is replaced by the simple combinational circuit which consists of XOR and AND gates. By using this method area and power is reduced when compared to regular CSLA and modified CSLA(BEC). The modified

16-bit CSLA without using mux is shown in fig.5 REF[4]. The structure is again divided into five groups with different bit size RCA and Combinational. Initially RCA structure is calculate for cin =0 the output of full adder is given to the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using Xor and And gates structure. The group 2to 5 of the modified 16-bit CSLA is shown Fig. 8.Comparing the group 2 to 5 of regular, modified BEC and WITHOUT MUX CSLA, it is clear that in this structure area and power is reduced. But the disadvantage of WITHOUT MUX method is that the delay is increasing than the regular CSLA.



6. **PROPOSED CSLA USING D-LATCH:**

In this method replace any one of the RCA structure (i.e. cin =1 or cin =0) by parallel structure of D-latches. For n bit RCA structure it required n D-latches with enable pin as a clk. Latches are used to store one bit information. The RCA structure cin is replace by enable pin, where enable signal is clk signal. When enable pin en =1 then the RCA structure is calculate for cin=1 that result is stored in D-latch. When en =0 then it will calculate for cin =0 and the D-latch output and full adder output is given to the mux. By using selection line it will gives the proper output. Where the enable time period for '1' is very less when compared to the enable pin '0'. Initially RCA structure will calculate for en=1 and then en =0. The architecture of proposed 16-b CSLA is shown in Fig. 7. It has different five groups of different bit size RCA and D-Latch. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. 6, it can understand that latch is used to store the sum and carry for Cin=1. Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16 bit adder.

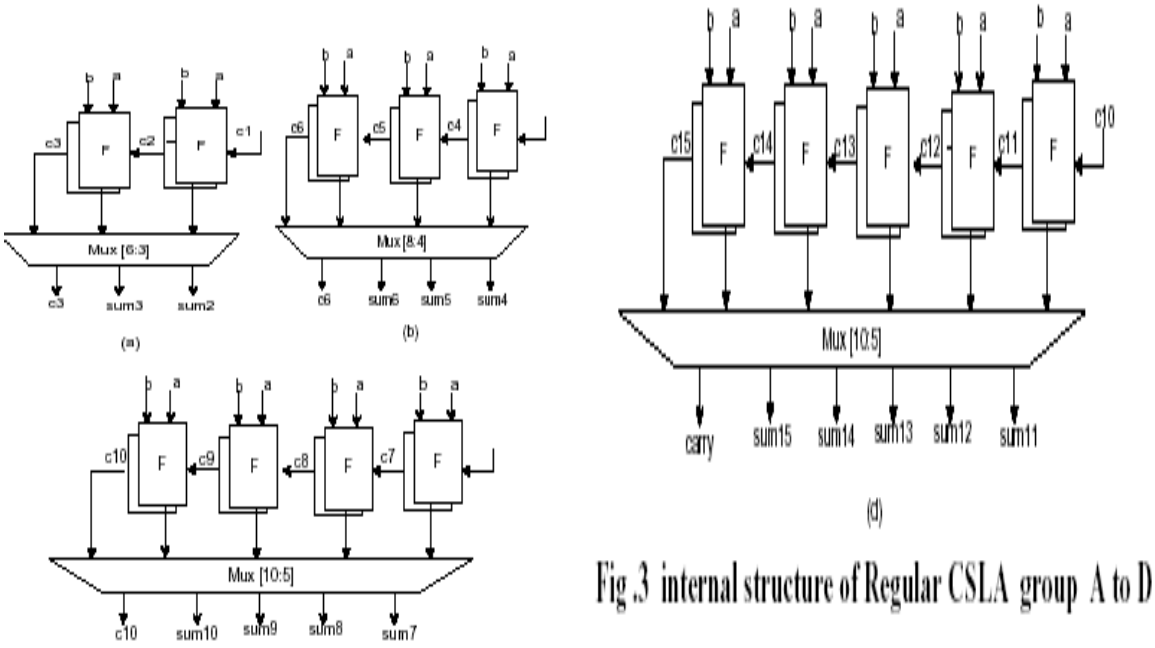
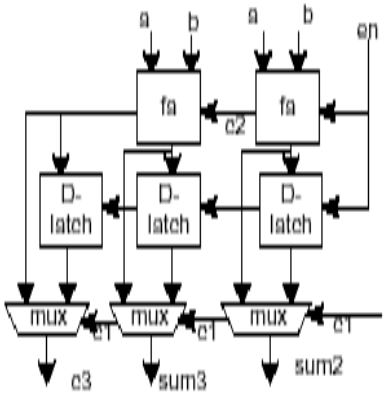
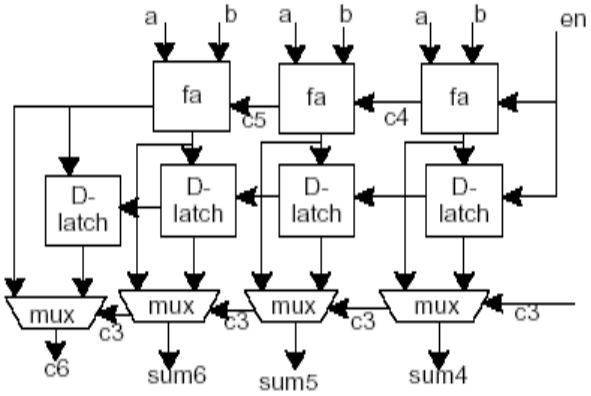


Fig .3 internal structure of Regular CSLA group A to D

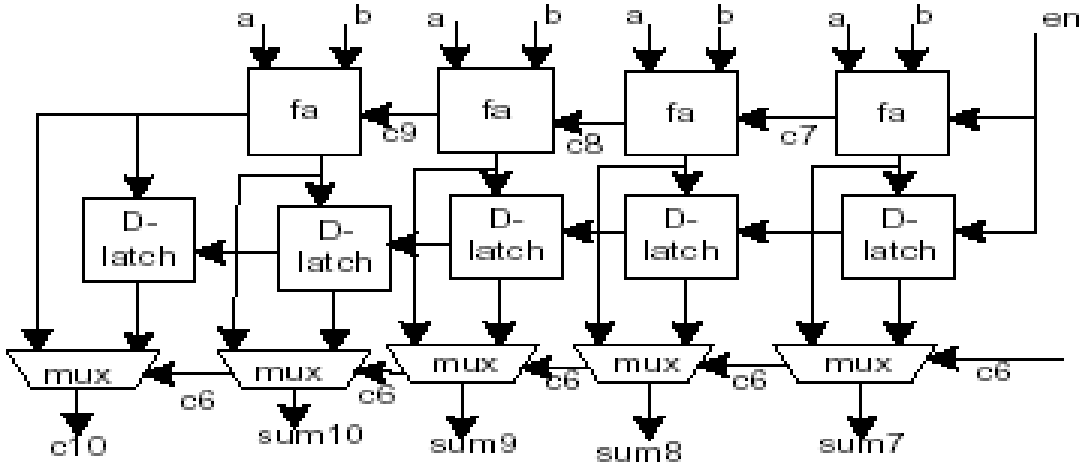


(a) Internal structure of 3 D-latchs in parallel block of Fig.10



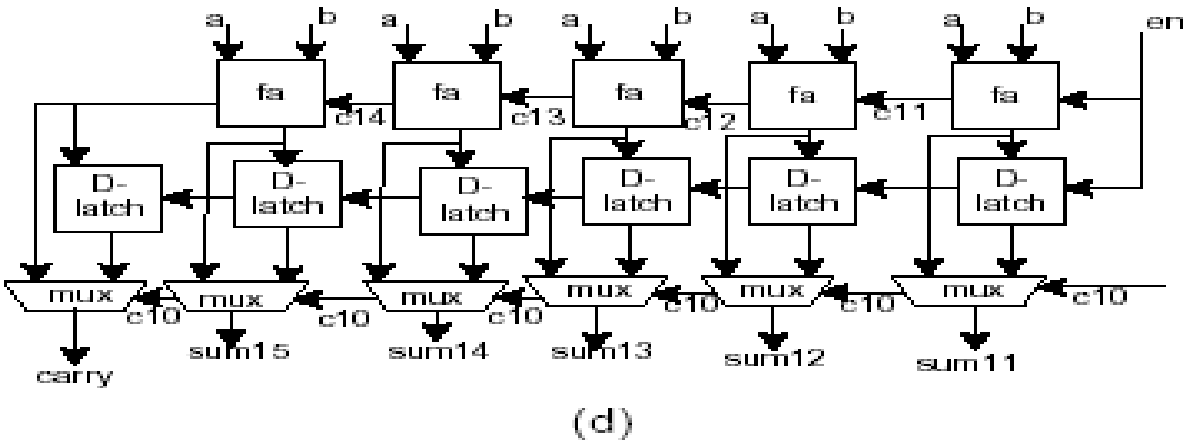
(b)

Internal structure of 4 D-latchs in parallel block of Fig.10



(c)

Internal structure of 5 D-latchs in parallel block of Fig.10



(d)

Internal structure of 6 D-latchs

internal structures of Proposed CSLA by using D-Latch

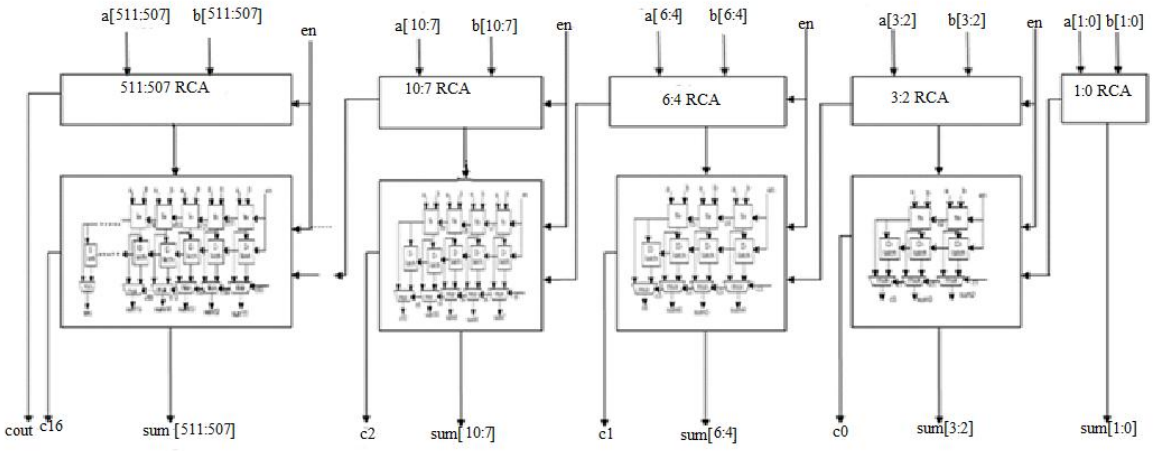


fig7. Proposed CSLA using D latch

Table 1:

TYPE OF ADDER	**DELAY(ns)**	**POWER(W)**
CSLA using RCA and D latch -512 bits	21.741	0.024
Csla using carry look ahead Adder- 64 bits	43.533	0.264

7. **SIMMULATION RESULTS:**

The design proposed in this paper has been developed using Verilog-HDL and synthesized the power and timing report. The comparison between carry select adder using RCA and Look ahead adder is made based on the power and delay obtained as in table 1.

8**. CONCLUSION:**

A unique approach is proposed in this paper to reduce the power and delay of SQRT CSLA architecture. This paper shows the design of carry select adder implemented by using D-Latch and compared with CSLA using carry look ahead adder.These two adders are implemented on Spartan XC3S500E FPGA device and the performance is compared. Power and Area is calculated by using synopsys RTL tool. This paper having better results when compared to CSA and modified techniques.

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