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An Individual-Driving Synchronous Rectifier for an LLC Resonant Converter With Voltage-Doubler Rectifier Structure

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***Abstract*—This paper proposes an Individual-driving scheme for a synchronous rectifier (SR) in an *LLC* resonant converter with a voltage-doubler rectifier. In the proposed scheme, only one secondary winding is used to drive two SRs in the voltage-doubler rectifier. Although the current rating of the SR in the voltage doubler rectifier is doubled, the voltage rating is well reduced and a lower voltage rating device with lower ON-state resistance can be used to compensate the increased current rating. Furthermore, the SR voltage stress is well clamped to the output voltage under any condition which improves the reliability of the circuit.**

***Index Terms*—Current driving, *LLC* resonant converter, synchronous rectifier (SR), voltage doubler.**

I. INTRODUCTION

The trend toward high power density and efficiency on power supplies has stimulated a lot of research effort over the past few decades. To achieve high power density, a high switching frequency operation with high efficiency is necessary. In recent years, the *LLC* resonant converter has been widely adopted in isolated dc/dc application due to its high efficiency and simple structure. Many research works have been published on the *LLC* resonant converter, such as those on optimal design methodology and protection.To further improve efficiency, the synchronous rectifier (SR) has been widely adopted in low output voltage applications to reduce the conduction loss of the output rectifier. Since the *LLC* resonant converter is a current-fed topology and has no output inductor, the voltage stress of the output rectifier is much lower than in conventional voltage-fed topologies. Low-voltage rating MOSFET can be used as an SR to achieve high efficiency.

However, the driving methods for SRs in an *LLC* resonant converter are much more complex than for the conventional voltage-fed topologies Generally, there are two ways to drive an SR, the self-driven and the external-driven methods. The external-driven method utilizes the primary-side gate drive signal to generate the SR gate drive signal, which is typically complex and costly. An extra isolation circuit is required to transfer the gate drive signal between the primary side and the secondary side. Also, with the external-driven method, the *LLC* converter can only be operated under the Continuous Current Mode (CCM) condition, which is not preferred for efficiency optimization

The self-driven method can be further categorized into the voltage- and current-driven methods. The voltage-driven method is attractive for its simplicity and low cost. The SR driving signal is derived from transformer secondary winding or inductor coupled winding with few extra components. However, they are topology dependent and usually only suitable for voltage-fed topologies with an inductive output filter. Since the *LLC* converter is a current-fed topology, the voltage on the transformer secondary winding can only be changed when SR is switched, which makes these voltage-driven methods not suitable for the *LLC* converter . In order to adopt the voltage driven methods in the *LLC* converter, a large leakage inductance needs to be presented in the transformer's secondary side, which results in high voltage spike across the SRs .The current-driven method senses the current flowing through the SR to turn ON or OFF the SR properly. Its main advantage is topology

independence. A current-driven SR (CDSR) can directly replace a diode in any topology. The most convenient way to sense the current is by using a current transformer (CT).

Numerous CDSR methods with CT have been proposed. Generally, each SR needs a CT to detect its current and generate the proper driving signals . In a high-current applications, the center-tapped structure is popular to reduce for reducing the conduction loss. Usually, two CTs are required to control two SRs in the center-tapped rectifier as shown , which will cause high current loss in traces and windings of CTs; also, the cost is high. In order to reduce the power loss and the cost, the required CT count need to be minimized. In the primary-side-current-sensing method is proposed. Thus, only one CT is required to drive two SRs in the secondary side. However, in the *LLC* resonant converter, the primary-side current differs from the secondary-side current due to the magnetizing current; a magnetizing current-compensation winding is required in to derive the actual secondary-side SR current. In the driving method with one CT in the secondary side for two SRs in the center-tapped rectifier is proposed.

The sensed energy from CT is used to drive the SRs; therefore, the turns ratio of CT is quite big in order to minimize the related power loss, which is not suitable for a high-frequency application. Also, the gate-driving voltage varies with the load current. An SR-driving method for a voltage-doubler rectifier was proposed in it], but the CT needs two secondary windings. Another current-detecting method is to utilize the drain-to-source voltage drop Vds when SR is ON. Several SR-driven methods based on Vds detection with an IC or discrete circuit have been proposed in it. Some commercial ICs are also available, such as IR1167/8, TEA1761, and MP6922. However, the accuracy and reliability of these driving methods are highly affected by the SR package, printed circuit board (PCB) layout, ON resistance R_{ON} of SR, and even by the temperature. The threshold for current detecting is usually around several milli volts, which makes the IC implementation difficult and costly Due to the inevitable package and circuit inductance, the sensed V_{ds} is the sum of the R_{ON} voltage drop and the inductive voltage drop, which leads to duty cycle loss in a high-frequency operation. A capacitive network to compensate the inductive voltage drop is proposed in it. the parameters design and turning are still complex. Furthermore, the variation of the parasitic parameters and R_{ON} will deteriorate the performance of the circuit. A digital implementation method is proposed in it, the SR turns ON based on the primary-side switch turn-ON signal and the SR turn-OFF point is smartly adjusted based on the sensed SR V_{ds} signal. An extra isolation circuit for the turn-ON signal is required, which complicates the whole circuit. Another issue related to the center-tapper rectifier in the *LLC* converter is the high voltage stress of SR due to the leakage inductance, which is always higher than 2 V_{out} An extra *RC* snubber circuit is usually required in practical applications to suppress this voltage spike and electromagnetic interference noise. Also, the transformer has two secondary windings, which decreases the utilization of transformer window area and makes transformer optimization difficult, especially for planar transformer.

II. PRINCIPLE OF OPERATION

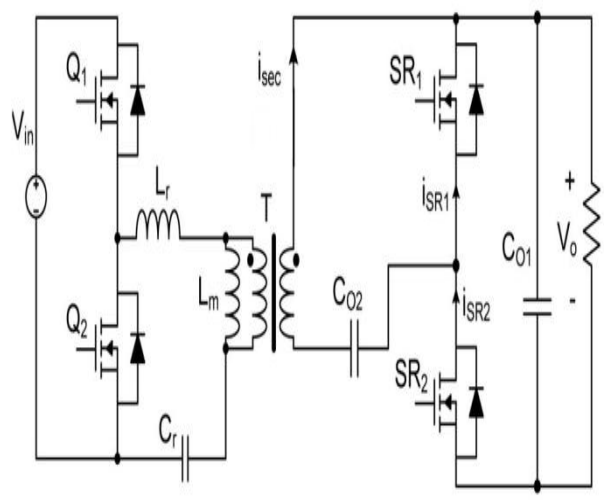

Fig. 1. Proposed SR-driving method for the trapezoid voltage-doubler rectifier.

As shown in Fig. 1, the trapezoid-type voltage-doubler rectifier is used. The gate drive voltage is clamped to the capacitor voltage VCO2 via D5 and D6 , which theoretically equals half of the output voltage. It is suitable for some applications with relative high output voltage such as laptop adapter and no extra voltage limit circuit is required. two clamp circuits that consist of *Ra* /*Da* /*Qa* and *Rb* /*Db* /*Qb* are used to clamp the gate voltage to zero under the

Discontinuous Current Mode (DCM) operation and provide a current freewheeling path for the magnetizing current of the CT. *Da* /*Db* is used to prevent *Qa* /*Qb* into deep saturation and fasten the ON/OFF speed. The capacitor *C*1 is used to prevent any potential dc bias of the CT. The PMOS *Q*7 is used as a level shifter and prevents the turning ON of SR2 when SR1 is ON since the undotted terminal of CT's secondary winding is clamped to *Vo* . Transistor pairs *Q*2 /*Q*3 and *Q*5 /*Q*6 are used as the push–pull stage to increase the driving capability. Transistor *Q*8 provides a freewheeling path for the magnetizing current of CT under DCM operation when both SRs are OFF. The detailed operation of the SR-driving circuit is presented later in the text. For simplicity, the output is simply modeled as a voltage source. Also, it is assumed that all of the switching devices and diodes are ideal, and theCT is modeled as a perfectly coupled transformer with magnetizing inductance *Lm* CT. The steady-state operation waveforms and related equivalent circuits are shown in Figs. 3 and 4, respectively. The voltage across *C*O2 is modeled as a voltage sources *V*CO2 in the equivalent circuit. Before *t*0 , both SR1 and SR2 are OFF.

At *t*0 , the transformer secondary side current *i*sec increases from zero, and the body diode of SR1 begins to conduct. The clamp transistor *Qa* turns OFF as soon as the body diode of SR1 turns ON. And the gate voltage of SR1 *V*gs SR1 is charged up by the reflected current *i*CTS1 through *N*CTS1 and the magnetizing current of CT *i*CT*m*. As mentioned earlier transistor *Q*2 is used to increase the driving capability with its current gain. The gate voltage *V*gs SR1 is given as where *C*gs is the gate capacitance of SR1 ; *N*CT is the turns ratio of the CT, i.e., *N*CT = *N*CTS/*N*CTp; and β is the current gain of transistor *Q*2 . In this mode, when the SR1 gate voltage *V*gs SR1 reaches the turn-ON threshold voltage, the current flows through SR1 instead of the body diode. When the *V*gs SR1 reaches the output voltage *Vo* , the clamp diodes *D*5 turns ON, *V*gs SR1 is clamped to *V*CO2, and this mode ends.

In this mode, SR1 is kept ON and the magnetizing current *i*CT*m* increases linearly. Since the clamp diodes *D*5 is ON, the sensed energy from the CT is fed to the capacitor *C*O2 and, then, fed to the output when SR2 is ON. Therefore, a small turns ratio of CT can be used to reduce the size and the turn-ON delay time as indicated in (1). The magnetizing current of CT can be expressed as where *Lm* CT is the magnetizing inductance of CT; *I*CT max is the peak magnetizing current of the CT; and *V*clamp is the clamp voltage for the gate drive signal, which is equal to *Vo* /2 here. *VD* is the forward-voltage drop of the clamp diode When the transformer's secondary-side current decreases to a certain level, the CT's secondary-side current *i*CTS1 is smaller than the magnetizing current *i*CT*m*, the current difference flows through *Q*8 to turn ON *Q*3 , and *V*gs SR1 is discharged to zero quickly. As soon as SR1 turns OFF and its drain–source voltage *V*ds SR1 increases from zero, the clamp transistor *Qa* turns ON and the gate voltage *V*gs SR1 is clamped to zero until next switch cycle. This mode only exists in the DCM mode and both SR1 and SR2 are OFF. For CCM and critical DCM operations, this mode no longer exists. The magnetizing current of CT *i*CT*m* freewheels through *Q*8 and *D*1 . It should be noted that the transistor *Q*8 can also handle the current from collector to emitter since the structure of the transistor is symmetrical, though the current gain is a little bit different. In this mode, the current flows through SR2 . Although the operation of this mode is similar to that of the turn ON of PMOS *Q*7 should be clarified here. As soon as the body diode of SR2 turns ON, the clamp transistor *Qb* and *Q*8 are OFF. The sensed current from CT charges up the gate–source capacitor of *Q*7 , and *Q*7 turns ON. Also, the sensed current from CT charges up the gate voltage of SR2. The gate–source voltage of *Q*7 is the same as *V*gs SR2 except the polarity since SR2 is ON. As soon as *V*gs SR2 reaches *V*CO2, the clamp diode *D*6 turns ON and this mode ends. The other operating modes during [*t*5–*t*8] are easy to understand since they are similar to Modes 2, 3, and 4, as described earlier, and they are thus not repeated here. The only difference is that the gate voltage of SR2 , i.e., *V*gs SR2, is clamped to *V*CO2 through *D*6 . In Mode 8, the magnetizing current of CT sfreewheels through *Qa* and *Q*8 /*D*2 when both SRs are OFF.

The detailed design of the *LLC* resonant converter is already well known and thus will not be elaborated upon here. Only the design considerations of the output capacitors will be briefly described. For simplicity, the transformer secondary winding current *i*sec can be simply treated as a sinusoidal waveform with amplitude being equal to *I*sec pk, which is given in it. In practical applications, the secondary-side current *i*sec is slightly different from the sinusoidal waveform and depends on the amplitude of the transformer magnetizing current.

The output capacitance of the voltage-doubler rectifier can be designed based on the maximum allowed

voltage ripple. Also, the capacitor C_{02} has high current stress due to the trapezoid voltage-doubler structure. The current through *C*O2 is the same as the transformer secondary side current *i*sec. The capacitor with very small equivalent series resistor (ESR), such as the ceramic capacitor, should be used to minimize the power loss. The proposed SR-driving circuits are quite simple. The key parameters for the proposed SR-driving method are the turns ratio *N*CT of the CT and its magnetizing inductance *Lm* CT. Basically, *N*CT is designed based on the required turn-ON delay time and related power loss.

Because the sensed current can be fed to the output, a small turns ratio is possible in the proposed SR-driving method. Although the sensed energy can be fed to the output, there is still conduction loss related to the diodes in the current path, such as D1 /D2 /D5 /D6. Assuming all the diodes have the same voltage drop V_D , the conduction loss can be estimated by it. Another important parameter for the CT is its magnetizing inductance.

The magnetizing current is given in it and the clamp voltage Vclamp is *Vo* /2 in the proposed SR-driving method. The amplitude of the magnetizing current of CT determines the turn-OFF point of the SR, which can be used to compensate the turn-OFF delay of the SR-driving circuit to prevent the reverse current flowing through the SRs.The other parameters in the circuit are quite simple to design. The maximum voltage across PMOS*Q*7 is the output voltage *Vo* .

A small signal PMOS can be used. Also, the bipolar transistors in the driving circuit should have the voltage rating slightly above *Vo* . Since the SR duty cycle is always 50% and the feedback loop response is usually slow in the *LLC* resonant converter, the voltage change in the *C*1 during transient is also slow and smooth, which means the potential parasitic ring caused by *C*1 can almost be eliminated. For the diodes in the proposed SR-driving circuit, the signal Schottky diode is preferred to reduce the forward-voltage drop and achieve good performance.

The voltage rating of the SRs is *Vo* , which is reduced by half in the center-tapped rectifier without considering the voltage spikes. And the current stress of transformer secondary winding and SRs is doubled compared to the center-tapped rectifier.

III. EXPERIMENTAL RESULTS

To verify the proposed SR-driving methods with voltagedoubler structure, a prototype for adapter application is built and tested. 230 V Input is given to it.Thus the output volage 24V is obtained and is shown in the figure 3 . Input is given it to the two switches and it provides reduce the voltage stress in it

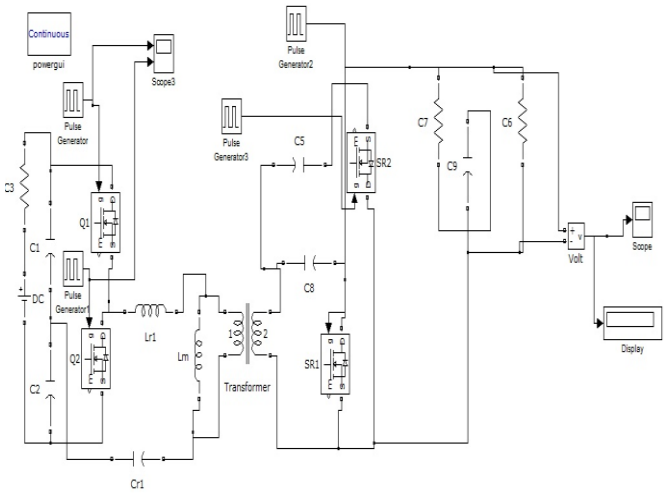

Fig 2 Simulation Diagram for Proposed Topology

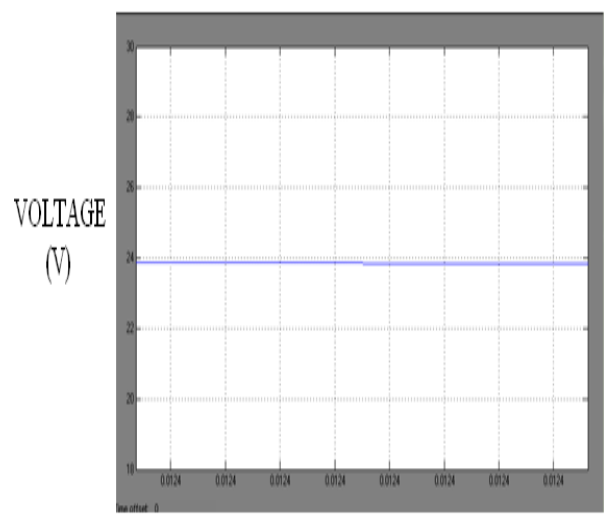

Fig 3 Output Voltage Waveform

IV.CONCLUSION

I presented a current-driving scheme for SR with trapezoid voltage-doubler rectifier structure for the LLC resonant converter. The voltage-doubler structure can reduce

the SR's voltage rating without the existence of parasitic ring in the conventional center-tapped rectifier though the current rating is increased. The SR voltage stress is well clamped to the output voltage under any condition, which improves the reliability of the circuit. The low voltage rating MOSFET with low ON resistance can be adopted as SRs to offset the increased current rating. Due to the inherent energy feedback mechanism, the proposed driving circuit also features low power loss and good performance. The experimental results are obtained from 24V output.

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