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A New Novel Charge Recycling Configuration Of Power Gated Technique For Mobile Application

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***Abstract*–Design of a suitable power gating (PG) in CMOS full adder structure is an important and challenging task in VLSI circuits where leakage current are significant.A new novel technique used to design the charge recycling circuit implemented in a 1.8 V 0.18-µm CMOS technology. In design where the mode transitions are frequent, a significant amount of energy is consumed to turn on or off the power gating structure. It is thus desirable to develop a power gating solution that minimizes the energy consumed during standby mode to active mode.This paper will focus on a solution by a new novel circuit technique for leakage current reduction in charge recycling (CR) between the virtual power and ground rails immediately after entering the sleep mode and just before wakeup. We will perform analysis and simulation of parameters such as leakage power, delay using Cadence Spectre180nm standard CMOS technology.**

***Index Terms* –Charge Recycling (CR),CMOS, Power Gating (PG).**

I. INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related toensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones suddenly powered for any periods (known as standby mode to active,during which the phone is able to receive an incomingcall), but are fully active for much shorter periods (known as talk to inactive mode, (i.e.) after disconnecting a call).Power gating is used to cut off the power to some functional blocks in a design. The power gating switch itself is typically realized as a single (footer) NMOS or (header) PMOS transistor, which disconnects logic cells from ground or VDD rails to reduce the leakage when the circuit is in the sleep mode.As a result, the leakage current has a disproportional effect on total battery life.

To summarize, some performance criteria are considered in the design and evaluation of adder cells, such as leakage power, ground bounce as well as varying process and compatibility with surrounding circuitries. None of these works attempt to minimize the power consumption during the sleep-to-active and active-to-sleep transitions or reduce wake up time and the noise generated by the power gating structure while maintaining the low standby leakage current. In this paper, we apply a new novel circuit for leakage current reduction in charge recycling technique to minimize the power consumption during the mode transition in a power gating structure while maintaining the wake up time. Through simulations, we show how the proposed technique also helps reduce the ground bounce in the sleep-to-active transition.

IICHARGE RECYCLING TECHNIQUE

There are two different blocks in the circuit; one is power-gated by an NMOS sleep transistor which connects the virtual ground (VGND), i.e., node G in the figure, to the ground, whereas the other is power-gated by a PMOS sleep transistor which connects the virtual VDD (VVDD), i.e., node P in the figure, to the supply.In the active mode, sleep transistors SN and SP are in the linear region and the voltage values of the virtual ground and virtual VDD are equal to 0 and VDD, respectively In the sleep mode, sleep transistors SN and SP are turned off; since they are high threshold voltage devices, very little sub threshold leakage current flows through them.All internal nodes of the gates in block C1 and the virtual ground node, G will be charged up to a voltage value very close to VDD. This happens because G is floating and leakage current causes its voltage level to rise toward VDD. Similarly, if the sleep period is long enough, all internal nodes of C2 and the virtual supply node, P, will be discharged to a voltage very close to 0.

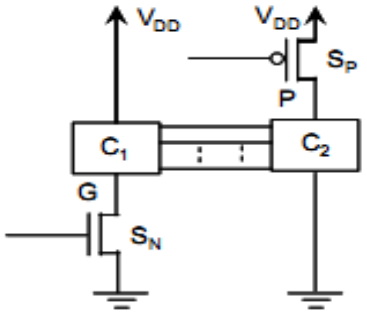

Fig 1 The Conventional Power Gating Structure

A.Charge recycling for Mode-Transition Energy

When the sleep-to-active transition edge arrives at the gates of the sleep transistors in an MTCMOS circuit, the voltage of VGND node, G, starts to fall toward zero, whereas the voltage of VVDD node, P, starts to rise toward VDD. If we denote the total effective capacitance in the VGND and VVDD nodes by CG and CP, respectively, we observe that during the active-to-sleep transition, CG is charged up from 0 to VDD, while CP is discharged from VDD to 0. The situation is reversed for the sleep-to-active transition, i.e., in this case CG is dischargedfrom VDD to 0, while CP is charged to VDD from its initial value of 0. These charge and discharge events on the VGND and VVDD nodes are wasteful from the energy dissipation. Our goal is to reduce the energy as we switch between active and sleep modes of the circuit. More precisely, we propose to use a charge-recycling technique to reduce the switching power consumption during the active-to-sleep and sleep-to-active transitions by adding a charge sharing switch between the VGND and VVDD nodes.The proposed charge-recycling strategy works as follows. We turn on the charge sharing switch Immediately before turning on the sleep transistors while going from the sleep to the active mode, and Just after turning off the sleep transistors while going from the active to the sleep mode. By turning on the switch at the end of the sleep mode as the circuit is about to go from sleep to active mode, we allow charge sharing between the completely charged up capacitance CG and the completely discharged capacitance CP. After the charge recycling is completed, the common voltage of the virtual ground and virtual supply is αVDD, where α is a positive real number less than 1. The value of α depends on the relative sizes of CG and CP. As a result of this step, the mode-transition energy is reduced. The reason is that in this case, the voltage of VGND changes from αVDD to 0 and the voltage of the VVDD changes from αVDD to VDD, whereas in the conventional MTCMOS circuit, the transitions are from VDD to 0 and from 0 to VDD at VGND and VVDD nodes, respectively.

III PERFORMANCE ANALYSIS AND SIMULATION RESULTS

We have performed simulation using cadence-spectre simulator and the technology used for simulation is 180nm CMOS technology

B.A New Novel Charge Recycling Technique

Power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Further, the peak of ground bounce noise is achieved with a proposed novel technique.

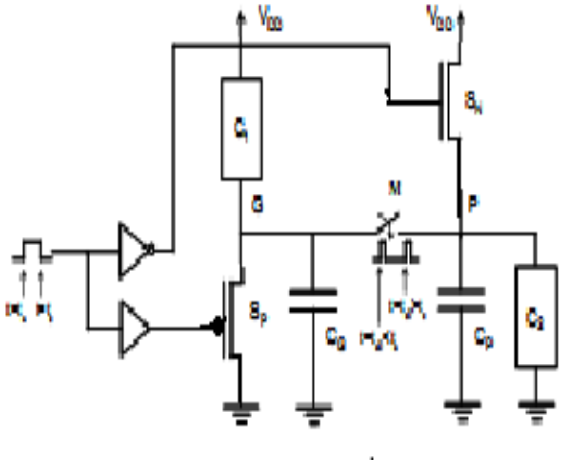

Fig 2. A new novel circuit technique for leakage current reduction in charge recycling

When a new novel circuit technique for leakage current reduction in charge recycling method is to same operation of early method but there is some difference between the processes. After the charge recycling is completed, As a result of this step, the mode-transition energy is reduced.

The reason is that, whereas in the conventional circuit, the transitions are from VDD to 0 and from 0 to VDD at VGND and VVDD nodes, respectively. This is the earliest method but the proposed a new novel circuit technique for leakage current reduction in charge recycling method is used to hold the virtual ground VGND node at high potential then the ground and NMOS pull up transistor maintains the virtual power VVDD node at lower potential. This cause the current flowing through the circuit to reduce and hence lower power dissipation during active mode.

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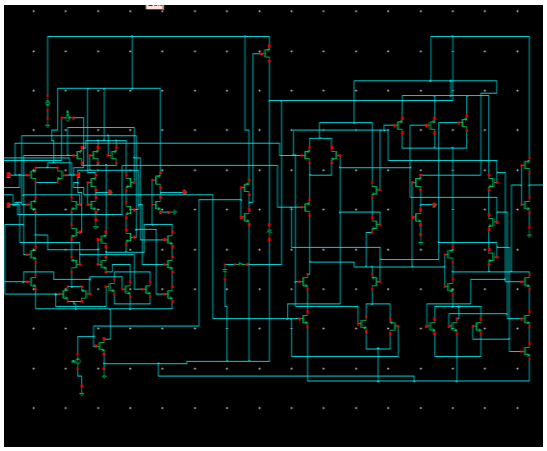

Fig 3 Schematic design of NMOS charge recycling

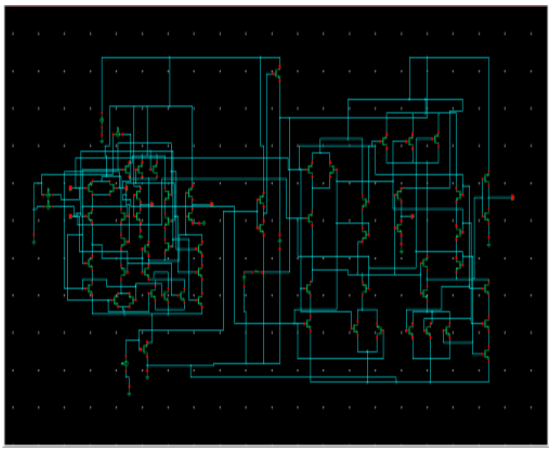

Fig 4. Schematic design of PMOS charge recycling

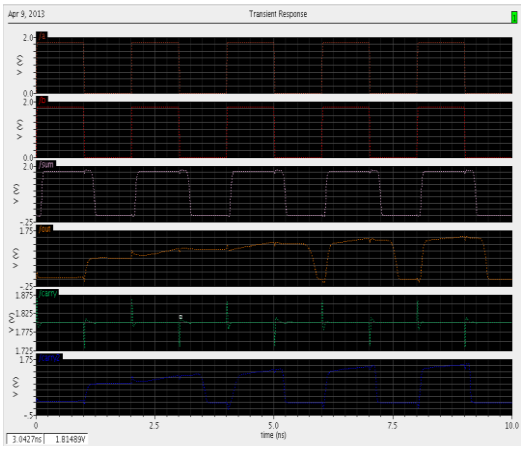

Fig5.Voltage and Time Response Curve in NMOS Charge recycling model

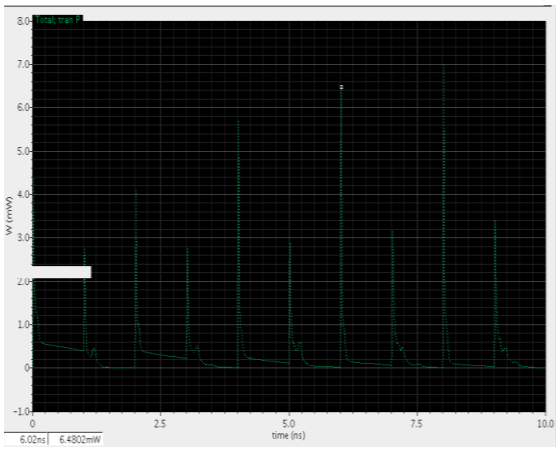

Fig 6 Power waveform of NMOS chargerecycling

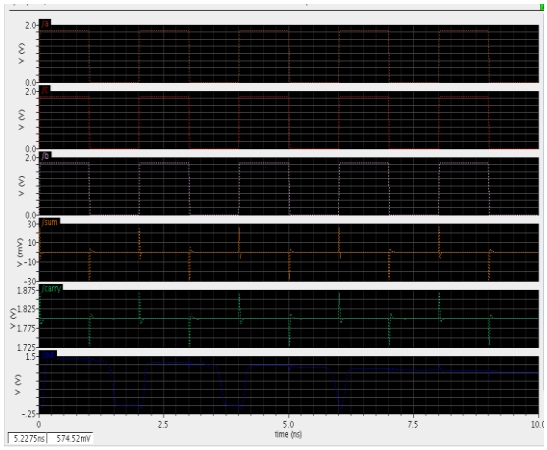

Fig 7. Voltage and Time PMOS charge recycling

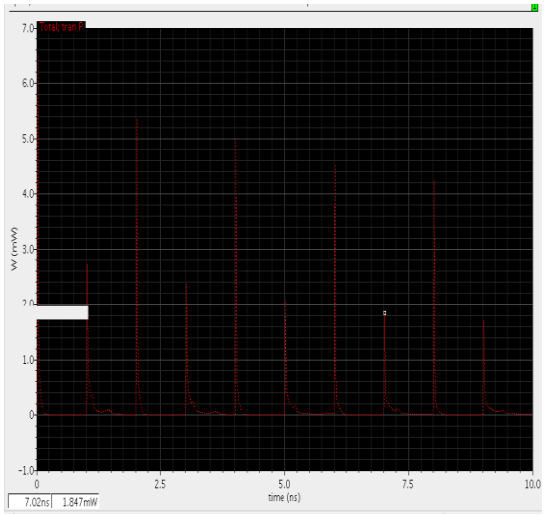

Fig 8 Power waveform of PMOS chargerecycling

IV RESULT OF MODE TRANSITION ENERGY

Table 1: Mode Transition Power Energy

Circuit	Total Delay	Resource Used(v)	Wake up time (ns)	Total Power	
				Time (ns)	Voltage (mw)
1Bit Full adder[NMOS Footer Power Gating]	1.211E-9	1.78	8.171	7.02	3.18
		1.46	7.052	5.02	2.89
		1.27	5.532	3.03	2.77
		1.20	2.021	1.02	2.76
1Bit Full adder[PMOS Footer Power Gating]	1.02E-9	1.08	8.171	7.02	1.84
		1.46	7.052	5.02	2.08
		1.15	5.532	3.03	2.38
		1.05	2.021	1.02	2.72

V.CONCLUSION

In this paper 1-bit full adder cell with power gating techniqueis implemented where a sleep transistor is added betweenactual ground rail and circuit ground the leakage power is reducedand in comparison to the conventional 1 bitfull adder cell. The delay is alsoreduced in the latter case. The implemented 1-bit full adders are designed using180nm technology and operated supply voltage of 1.8V.

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