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An On Chip Hindrance Computation Skill For Small Delay Deficiency Revealing Using Signature Registers

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Abstract: Efficient test and debug Techniques are indispensable for performance characterization of large complex integrated circuits. In this paper we present an on line scheme for latency fault revealing,where delay is quantized by a technique using signature registers which measures the delay of explicitly sensitized paths with the resolution of the on-chip variable clock generator. Small Delay Defects are recognized by means of a scan design which apprehend complete on-chip delay measurement in short time. The number of redundant latches is reduced exploiting the test bits of data for the impediment measurement.After that with the decrease of scan length,the number of the selectors of the scan design is reduced without decrease of number of extentable paths.By combining these techniques the area overhead will be reduced in this proposed system.

Index Terms - Small Delay Defects (SDD), Very Large Scale Integration (VLSI), sensitized paths, Scan Design.

1. INTRODUCTION

Frequent device scaling and large-scale integration of LSIs have resulted in an increase in small-delay defects (such as resistive-short or resistive-via) , which vary only small amount of path delay but makes outlier chips (chips with path delays which lie outside of the normal path-delay distribution).If small-delay defects cannot be detected in LSI screening, the outlier chips will cause improper operations under particular operation in certain applications and may cause improper operations after shipping due to effect of aging. Therefore, small-delay detection becomes a key to keep chip reliability [2]. Small-delay defects (SDD) are one type of timing defect, which introduces a small amount of extra delay to the design. Because of their small size relative to the timing margins allowed by the maximum operating frequency of a design, SDDs were not seriously considered in the testing of designs at higher technology nodes. Although the delay introduced by each SDD is small, the overall impact can be significant if the sensitized path is a long/critical path, especially when technology scales to 45 nm and below. As the shrinking of technology geometries and increasing of operating frequency of the design continues, the available timing slack becomes smaller.

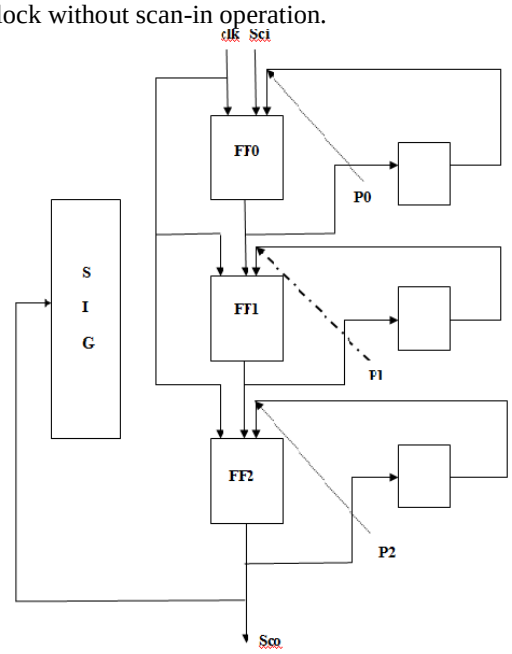
Therefore, SDDs have a good chance to add enough additional delay to a path to adversely impact the circuit timing and make that part deviate from its functional specifications [1]. A large portion of failures in delay-defective parts are due to SDDs in the latest technologies. Therefore, SDDs require serious consideration to help increase defect coverage and test quality, or decrease the number of test escapes (i.e., increase in-field reliability), denoted by DPM. Due to the small size of their delay, SDDs are commonly recommended to be detected via long paths running through the fault site. The delay measurement of paths inside the circuits is useful for detection and debugging of small-delay defects [2]. However, it is impossible to measure the small circuit path delays using an external tester, even if the resolution is high. The scan-based delay measurement technique with the variable clock generator is one of these on-chip delay measurement techniques [3]. In this technique, the delay of a path is measured by continuous sensitization of the path under measurement with the test clock width reduced gradually by the resolution. The main good point of the scan-based delay measurement technique is its high accuracy. The area overhead of these methods is still expensive compared with the conventional scan designs. The proposed method presents a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The measurement time of the proposed technique is smaller than conventional scan – based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

II.SYSTEM MODEL AND PERFORMANCE MEASURES

A. Whole System Model

The anticipated system is scan-based hindrance measurement. The discrepancy from the vital one is the usage of the signature registers and the additional latches for the hastening of the delay measurement. This system has three flip flops FF0, FF1, and FF2. Each flip flop has the input , the output, and the clock line clk. Each flip flop FFi is connected to an extra latch.

Initially ,we presume that each flip flop has its own extra latch. The value of each flip flop is stored in their respective latch, and the value of each latch can be loaded to the appropriate flip flops in arbitrary timing. In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation.



P1 is the path under measurement

Fig 1.Overall Delay Measurement System

It reduces the time for multiple sensitization of a path considerably. The horizontal line through these flip flops represents the scan path. The symbols SCi and SCo represent the scan input and output, respectively. The rectangle SIG represents the signature register using the linear feedback shift register as its basic component. The input of SIG is connected to the output of the last flip flop FF2.

We measure the delay of P1. In this we presuppose that the clock width of normal operation is 10 ns, and the resolution of the latency extent is 2 ns. First, SIG is initialized with reset operation. Second, the intented path is tested continuously 5 times with the test clock reduced progressively by the resolution. The multiple clock width testing is recognized by the variable clock generator. The test clock of the 1st testing (#1) is 10 ns. After the test, the test response is sent to SIG through the scan path with two clock shift out operation. The test clock of the second test (#2) is 8 ns. Similarly, the test clock width of the third, fourth, and fifth tests (#3, #4,#5) are the difference between 2 ns and the previous test clock Width.

Each test retort is sent to SIG with two clocks. After the above 5 times of delay fault testings, the signature value of SIG is repossessed. To approximate the delay, the retrieved signature value is compared with the expected signature values of the signature table.

B. Signature Table

The Signature Table has four columns. The first column is the cases of the measurement under test. The second column is the progressions of the test responses of #1–#5. The third column is the path latency value. The fourth column is the signature values of each case. Here, Sigr and Sigf are the signature values for rising and falling transition testings, respectively.

Table 1 Signature Table

Cases	#1	#2	#3	#4	#5	Delay (ns)	Sig. Sigr	Sigf
Case 0	F	F	F	F	F	10-	000	010
Case 1	P	F	F	F	F	8-10	011	001
Case 2	P	P	F	F	F	6-8	101	111
Case 3	P	P	P	F	F	4-6	100	110
Case 4	P	P	P	P	F	2-4	110	100
Case 5	P	P	P	P	P	0-2	010	000

The delay of every path is fixed as more than 10, 8–10, 6–8, 4–6, 2–4, or 0–2ns, with 2ns resolution. The series of the test responses for the 5 times measurement are shown in the table. The symbolscase0,case1,case2,case3,case4, case5 indicate the cases with path delays, more than 10, 8–10, 6–8, 4–6, 2–4, 0–2 ns, respectively. The symbols P and F represent the pass and fail of a testing. In case of rising transition testing, P=1 and F=0 , and in case of falling transition testing, P=0 and F=1.The obtained signature value is compared with the expected signature values on the table, and fixes the delay value.

C. Delay Measurement Sequence

When the number of flip flops used in testing is n ,T is the clock width , ΔT is the measurement resolution, and Nmeas is the continuous time of testing, the delay measurement sequence of a intented path is as follows. In this we assume that the test vector is already stored in the latches. The end point of the measured path is FFk ($0 \leq k \leq n-1$).

Step 1: Initializing SIG.
Step 2: Test vector is loaded from the latches.
Step 3: Test clock width T is set to normal clock width.
Step 4: Test clock is applied.
Step 5: The test response is sent to SIG which is connected to the output of FFn-1 with n-k clocks.
Step 6: If testing time is equal to Nmeas, go to Step 7 after the signature value of SIG is retrieved; otherwise go back to Step 2 after the test clock width T is updated to T-ΔT.

Step 7: The delay value is estimated by comparing the retrieved signature value and the signature table.

III. PROPOSED ARCHITECTURE IMPLEMENTATION

Small-delay defect detection methods using on-chip delay measurement techniques have been implemented. The direct measurement of the real delay of each path of each chip screens outlier chips robustly even in the presence of process variation or the gap between real and simulation environment. It realizes higher fault coverage of small-delay defects than the simulation-based ones.

A. Variable Clock Generator

In this system, the clock width should be reduced constantly by a regular interval. It is difficult for an exterior tester to control this clock operation. Therefore an on-chip variable clock generator is indispensable for the proposed method.

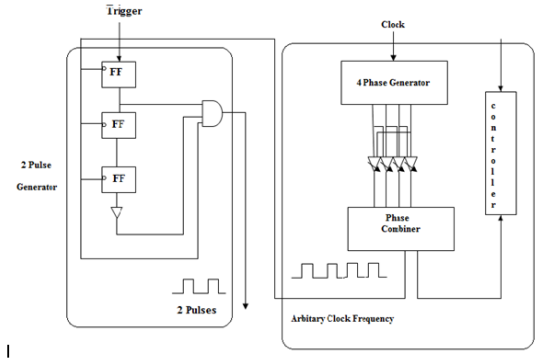


Fig 2.On-chip Variable Clock Generator

The circuit consists of the phase interpolator-based clock generator and the 2-pulse generator. The phase-interpolator-based clock generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal.

B. Scan Flip Flop For Measurement

The line D is the input, Q is the output, and clk are the clock lines, respectively. The test bit to the flip flop is provided by connecting the line latch to an extra latch. The lines si and so are the input and output for constructing the scan path. The input si is connected to so of an adjacent scan flip flop or the scan input. The output so is connected to si of an adjoining scan flip flop of the scan output. The flip flop has two multiplexers. The lines si and latch are the inputs of the first multiplexer which is controlled by se1. The output of the first multiplexer and D are the inputs of the second multiplexer which is controlled by se0 . When se0=0 , the flip flop is in normal operation mode. When se0 = 1 and se1 = 1 , the flip flop is in scan operation mode. When se0 = 1 , se1 = 0, the flip flop loads the value stored in the latch connected to the latch line.

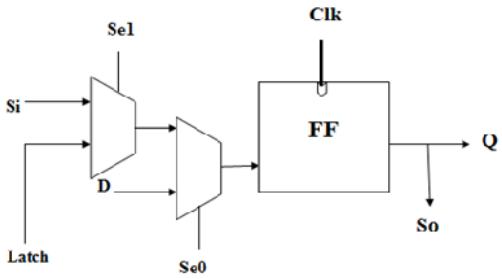


Fig 3.Scan Flip-Flop

C.Reconfigurable Signature Register

The signature register for the anticipated extent requires the following functions to meet the insist of the proposed measurement.

- Test response is captured in arbitrary timing.
- Shifting out the signature data in arbitrary interval.

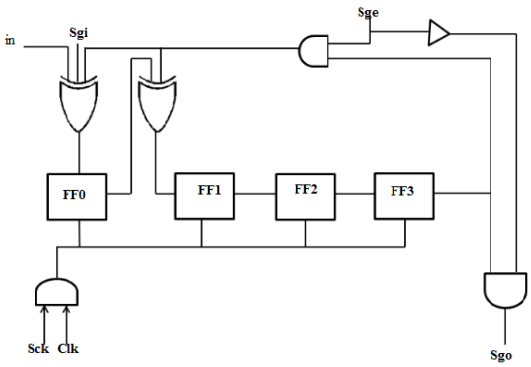


Fig 4. Reconfigurable Signature Register (Four Bit)

The span of the signature register is four bit. Therefore it has four flip flops FF0 ,FF1,FF2,FF3.

The signature register can be configured to a shift register. The line sge controls the configuration. When sge=1 , it exert as a signature register. When sge=0 , it exert as a shift register. The input of the signature register is line in. Test responses are sent to in during the measurement. The line clk is clock line. The clock line is controlled by sck . When sck=0 , the signature register does not capture the input value.

When sck=1, the signature register captures the input value synchronizing with the positive edge of clk. By controlling sck ,the signature registers capture only the target test response. When sge=0 , this circuit is configure to the shift register.The input is sgi .The output is sgo The measurement system needs multiple signature registers .The input and output are connected to the output and the input of adjacent signature registers to construct a long shift register for sending all the signature values to the external tester.

D.Area Reduced Scan Design Architecture

An area efficient scan design for the impediment measurement using the signature registers is introduced.

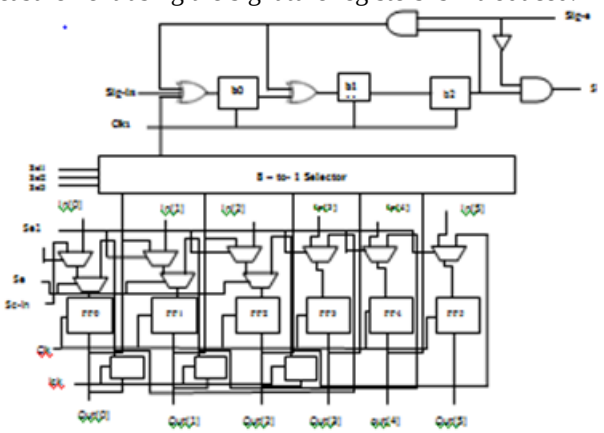


Fig 5.Area Reduced Scan Architecture

This scan design consists of three parts, namely a flip flop part, a selector part, and a signature register part. The latches are managed by the latch clock lck.The combination of the values of the lines se, and se 1 fixes the operation mode of the scan. When both se and se_ 1 are 1, a scan path is erected, which is scan-in operation mode. When se is 0, the flip flop is in normal operation mode. When se is 1 and se_ 1 is 0, each value of L; is loaded to every flip flops, which is the operation mode for loading the value from L the latches. The control lines of the selector se0-se2 select the flip flop capturing the test response of the path under measurement. The signature register has two modes , a measurement mode and a
Scan mode.In the measurement mode,a signature register is constructed. In the scan mode, it works as a scan path to retrieve the signature value from sig_ out.

IV.RESULTS AND DISCUSSIONS

The performance of the blocks in the overall system architecture is obtained as;

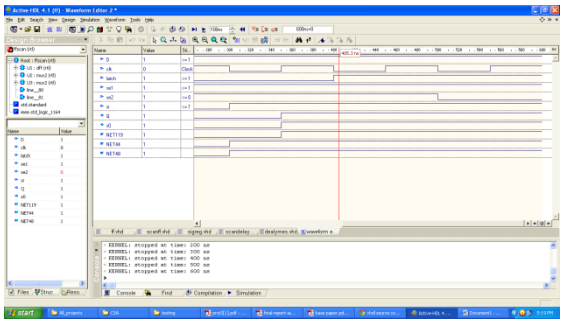


Fig 6.Output Of The scan Flip-Flop

Si,So are the input and output for constructing the scanpath.
The conditions in which the scan fliopflop works are :
*Se0=0,the FF is in normal operation mode.

*Se0=1,Se1=1,the FF is in scan operation mode.

*Se0=1,Se1=0,the FF loads the value stored in the latch connected to the latch line.

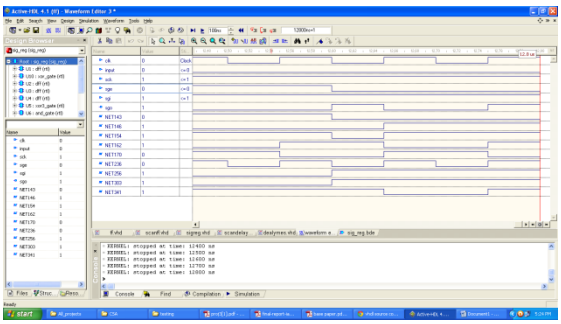


Fig 7.Output Of The Reconfigurable Signature Register

Fig 7 explains that this signature register can be configured to shift register which is controlled by sge,under the conditions.

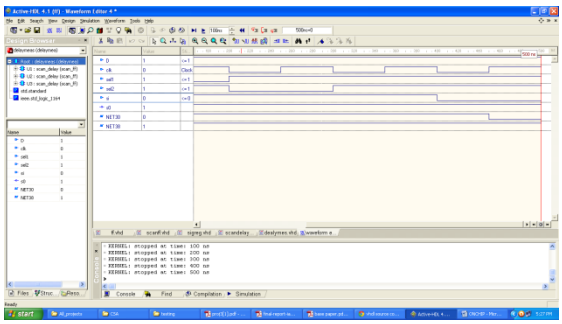


Fig 8. Output of The Delay Measurement Architecture

This fig. Explains about the path which is considered for delay measurement P1.

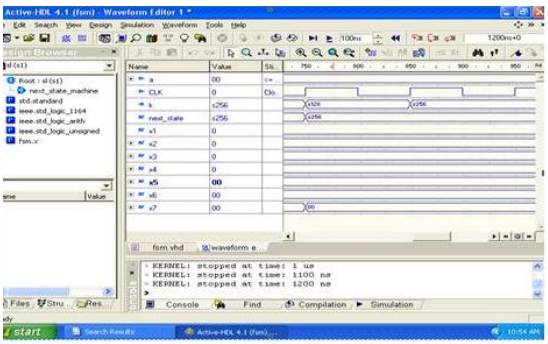


Fig 9. Output Of Test Responses

The description was made by VHDL and the functionality was verified by Active HDL simulator edition 8.3.

V.CONCLUSION

Based on the embedded measurement technique, new efficient on-chip delay measurement technique using signature registers with the reduction of area overhead was

put forward. The architectural structure of measurement system consists of scan flipflop and on chip variable clock generator.Since Signature Register is a main component in the implementation of this system, it find extensive applications as it can be reused for testing, debugging and diagnosis. Further, the proposed architecture of a scan design measures the delay in the internal paths of SOC. Future work is the reduction of scan chains.

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