

A High speed Low Power Adder in Dynamic logic base on Transmission Gate

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Abstract— Speed operation is depends on the longest critical paths in the multi-bit adders and also the MOSFET transistor gain which in turn depends on transistor size. The power consumption in MOSFET is depends on the switching frequency, sub threshold leakage and switching time. In this paper author proposed the speed and area efficient transistor base adder using static CMOS pass transistor logic. In this method we shortened the longest critical path to decrease the total critical path delay. The design simulation on microwind layout tool calculates the worst-case delay in nanosecond and total power consumption in microwatt range.

Index Terms— Adder, delay, multi output domino logic, Transmission gate (TG).

INTRODUCTION

Adder is the essential module of arithmetic unit in microprocessor, microcontroller, and a complex digital signal processing system etc. The speed, performance, and power are the major constraints are in the VLSI. A parallel adder uses a simple design but delay due to carry propagation will reduce its performance. The largely accepted high speed adder is look ahead adder, skip adder, conditional sum adder, carry skip adder etc. The high speed adder with CLA (Carry Look Ahead) are extremely used but it has the limitation of large number of transistors requires for its design [1-2].

I. TRANSMISSION GATE

Transmission Gate has the capability of a high-quality switch with small resistance and capacitance [3]. Transmission gate is the part of the design module of this paper. The delay of the transmission gate can be modeled by linearized RC network. The on-resistance and diffusion capacitance of transmission gate is represented by a resistor.

$$t_p = 0.69 \sum_{i=1}^N \sum_{j=1}^n C_i R_j$$

Transmission Gate is generally used to implement of XORs and MUXs with the minimum number of transistors.

II. ARCHITECTURE DESIGN

The architecture designs of our adder logic consist of transmission gate (TG) base multiplexer logic. Here the full adder is design by using transmission gate base OR, AND, XOR logic gates. Fig 1 shows the transmission gate base OR gate. When input enable is equal to logic '0' then it will transmit input B towards V_{out} by upper TG otherwise it will transmit input logic '1' towards V_{out} by lower TG.

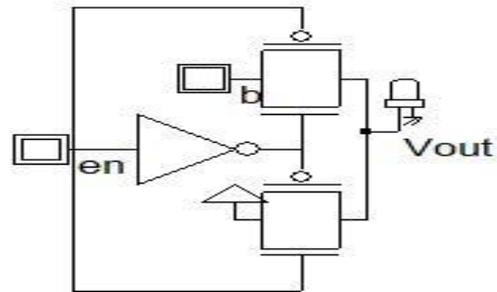


Fig.1. Transmission Gate base OR gate

In Fig.2 the Transmission gate AND based , when input enable is equal to logic '0' then it will transmit grounded input towards V_{out} by upper TG otherwise it will transmit input B towards V_{out} by lower TG.

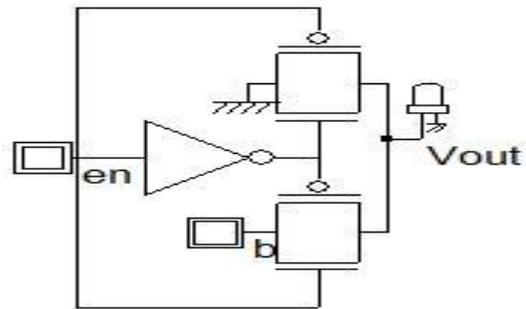


Fig.2. Transmission Gate base AND gate

Fig 3 shows the XOR logic operation, where input A is equal to logic '0' then it will turn on upper transmission gate and turn off lower transmission gate. Thus the input B is transmitted towards output V_{out} .

On the other hand when input A is at logic '0' then it will turn on lower transmission gate and turn off upper transmission gate. This transmits complimented binary of input B towards V_{out}.

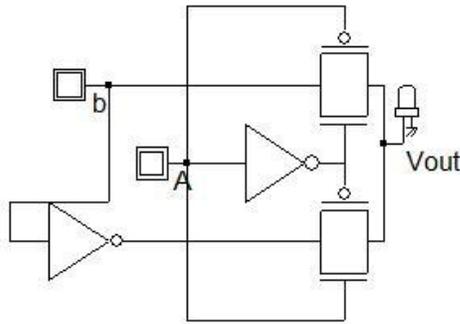


Fig.3. Transmission gate base XOR logic

Fig 4 shows the transmission gate base full adder logic using transmission gate base OR, AND, XOR logic gate. This can be design by two transmission gate base half adder circuit.

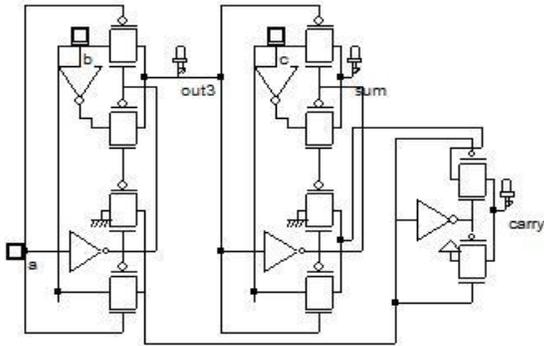


Fig. 4. Transmission Gate base full adder logic

The conventional adder is design using 42 MOSFETs. In proposed adder, total number of transistors require to design are 30.

III. POWER REDUCTION

The power dissipation in MOSFET is

$$P_{avg} = P_d + P_{sc} + P_{leak} + P_{static}$$

Where, P_d is the capacitive switching power dissipation, P_{sc} is the short-circuit power dissipation, P_{leak} is the power dissipation due to leakage currents and P_{static} is the static power dissipation due to non-leakage static currents [2]. Short-circuit power and capacitive switching powers are components of dynamic power dissipation. Leakage power is a major component of static power dissipation in CMOS circuits. dynamic power dissipation of a digital CMOS circuit depends on the supply voltage V_{dd}, the clock frequency f_{clk}, the node switching time, the node capacitances, the node short circuit current and the number of nodes. A reduction of each of these parameters results in a reduction of dissipated power. The

dynamic power can be reduce by reducing capacitive load which is generated from gate, diffusion and interconnect wiring. This can be done by using pass transistor transmission gate logic which reduces number of transistors and interconnect nodes as possible.

IV. CARRY LOOK AHEAD ADDER

The carry look-ahead adders enhance the speed by calculating the carry signals in advance, depends on the input signals. This reduces the propagation time for carry in series connected adders. The logic equation for sum bit of a binary adder can be written as S_i = X_i xor Y_i xor C_i. For a combination of inputs X_i and Y_i, adder stage I is said to be generate a carry if it produces a carry out of 1 independent of the input on X₀-X_{i-1}, Y₀-Y_{i-1} and C₀. For the combination of input X_i and Y_i adder stage I is said to propagate carries if it produces a carry out of 1 in presence of the input combination of X₀-X_{i-1}, Y₀-Y_{i-1} and C₀ that cause a carry in of 1 [3-5].Corresponding to this definition the logic equations for a carry generate signal G_i and a carry propagate signal P_i for each stage of carry look ahead adder.

$$G_i = X_i \cdot Y_i$$

$$P_i = X_i + Y_i$$

$$C_{i+1} = G_i + P_i \cdot C_i$$

To eliminate carry ripple we recursively expand the C_i in term of each stage. Thus:

$$C_1 = G_0 + P_0 \cdot C_0 \tag{1}$$

$$C_2 = G_1 + P_1 \cdot C_1$$

$$= G_1 + P_1 \cdot (G_0 + P_0 \cdot C_0)$$

$$= G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0 \tag{2}$$

$$C_3 = G_2 + P_2 \cdot C_2$$

$$= G_2 + P_2 \cdot (G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0)$$

$$= G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0 \tag{3}$$

$$C_4 = G_3 + P_3 \cdot C_3$$

$$= G_3 + P_3 \cdot (G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0)$$

$$= G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0 \tag{4}$$

These above equations by using transmission gate logic will minimize number of transistors, Minimize all internal capacitances, by minimizing the active area of the transistors, and thus minimizing power [3,6-7]. The P_i and G_i generator is design by using the transmission gate base AND gate logic and XOR gate logic. A P_i and G_i generator is a combinational circuit that performs the arithmetic sum of two input bits. It consists of two inputs and two outputs P_i and G_i. Two of the input variables can be defined as A_i and B_i and the two output variables can be defined as P_i for sum and G_i for carry.

V. PROPOSED ADDER

The layout design of the basic building blocks of OR gate, AND gate and XOR gate is design by using transmission gate shown in fig 5, fig. 6 and fig. 7. And the basic building blocks of full adder

is design by using transmission gate is shown in fig 8. When the gate is at zero, no channel exists so the node V_{source} is disconnected from the drain. When the gate is on, the source copies the drain. It can be observed that the n-channel MOS device drives well at zero but poorly at the high voltage. The highest value of V_{source} is around 0.85V, which is V_{DD} minus the threshold voltage. This means that the n-channel MOS device do not drives well logic signal 1. Whereas it can be observed that the PMOS device drives well at one but poorly at the low voltage. The highest value of V_{source} is around 0.41V, which is V_{SS} plus the threshold voltage. This means that the p-channel MOS device do not drives well logic signal 0. Thus in transmission gate both the NMOS and PMOS is turn on and turn of at the same time. This gives both strong '1' and strong '0' output.

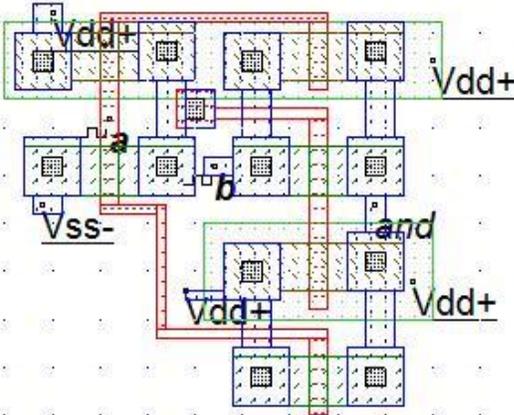


Fig.5. Layout design of transmission gate base OR gate

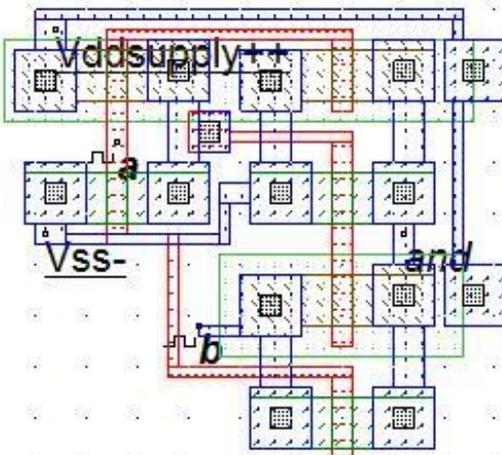


Fig.6. Layout design of transmission gate base AND gate

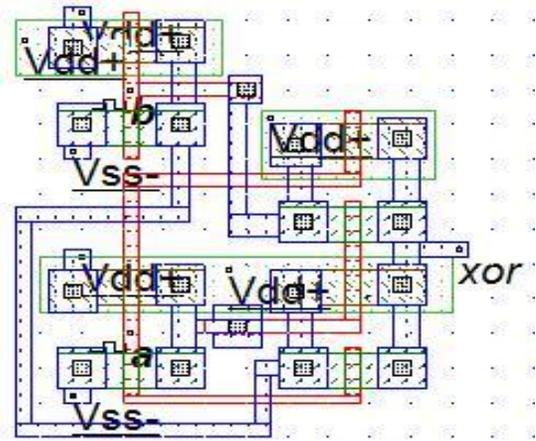


Fig.7. Layout design of transmission gate base XOR gate

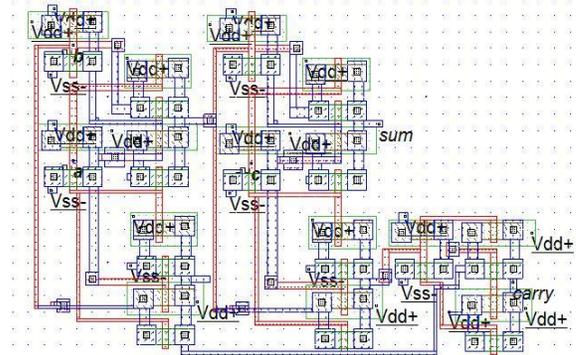


Fig.8. Layout design of transmission gate base full adder logic

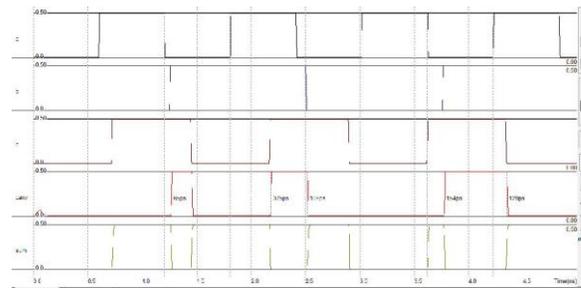


Fig.9. Timing simulation of TG base full adder logic

Fig. 8 shows the layout design of two half adder base full Adder using transmission gate and fig.11 shows 4 bit adder circuit. Fig. 9 shows the timing simulation of full adder logic using transmission gate. The circuit receives two inputs of n bit operands generates half sum words S_0 and half carry words C of width n bits. The successive half adder logic receives these half sum and carry bits and generates full sum output.

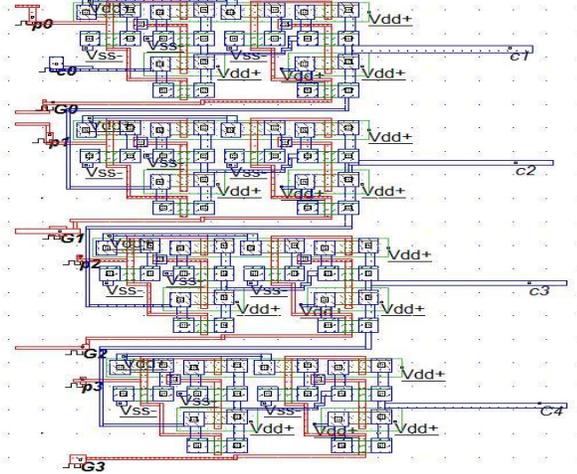


Fig.10. Four bit adder logic consist of 4 parallel full adder logic

The layout design of fig 10 is based on the logic formulation given in above equations (1), (2), (3) and (4) of the carry look ahead adder. It consist of transmission gate base AND, OR logic gates.

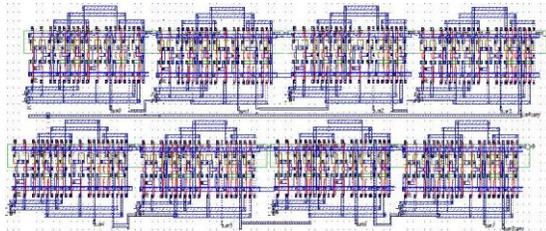


Fig.11. Layout design of cascade n bit full adder logic

Fig 11 shows the Cascade n bit full adder stage each of which handles one bit. and fig 12 shows the timing simulation of n bit full adder logic [8].

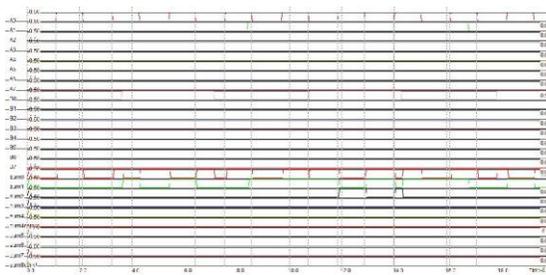


Fig.12. Timing simulation of n bit full adder logic

The carry input to the least significant bit is normally set to zero and the carry output of each adder is connected to the carry input of next most significant bit adder. This kind of operation is slow because the carry require propagating from least significant bit to most significant bit. The worst case delay is calculates as

$$t_{ADD} = t_{COUT} + 9(n-2)t_{CINCOUT} + t_{CINS}$$

In above equation where t_{COUT} is delay in lest significant bit stage, $t_{CINCOUT}$ is the delay from cin to cout in the middle stage, and t_{CINS} delay from cin to s in most significant stage.

Thus a high speed adder can be designed by considering each sum output S_i with just two level of logics. This can be accomplish by writing an equation for S_i in terms of inputs and C_0 , multiply and add logic.

Table.1. Parametric analysis of design logic.

Basic cell	Number of transistor	Dynamic power (μ W)	Delay (ps)
Design Parallel Adder	240	2.3	2 to 3 ns
Conventional adder	336	12	2 ns
Propose Adder	256	12.5	2 ns

Table.2. Parametric analysis of basic cell design.

Basic cell	No. of transistor	Static power (μ W)				Dynamic power	Delay (ps)
		0	1	10	11		
Input	-	0	0.215	74.7	74.77	-	-
AND	8	0.21	0.215	74.7	74.77	0.2	2 to 4
OR	6	0.047	0.042	0.046	0.005	0.338	2 to 4
XOR	6	0.086	0.051	0.088	0.015	0.1	2 to 4
Half Adder	12	0.086	0.056	0.088	0.056	0.09	2 to 4

The Table.1 and Table.2 are the parametric analysis for propagation delay, static power, and dynamic power dissipation. The static power is calculated by applying the static input of all possible combination. The static power of the design is varies from 4μ W to 74μ W range. The number of transistor for conventional adder is calculated by the number of transistor requires in conventional full adder. One conventional full adder requires two XOR gate, two AND gate and one OR gate which have 24, 12, 6 transistor each i.e. one full adder requires 42 transistor. Thus the 8 bit conventional adder requires 336 numbers of transistors.

VI. CONCLUSION

The above circuits are simulate in microwind 3.1 using 50nm CMOS technology The delay measured in the range of ns, power consumed in the range of microwatt and area acquired reduced number of transistor. A transmission gate base design is an analog switch controlled by logic signals. It uses N and P type MOS transistor. We design the basic building blocks of carry look ahead

adder by using transmission gate. Transmission Gate has is a high-quality switch with low resistance and capacitance. Sizing is also not necessary in general, as the resistance and capacitance decrease and increase respectively as the gate $W=L$ ratio is increased. TG is commonly used to implement designs with the minimum number of transistors.

VII. REFERENCES

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