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ACTIVE MODE POWER REDUCTION USING SUBCLOCK POWER GATING TECHNIQUE

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Abstract: This paper presents a technique, called sub clock power gating, for reducing leakage power during the active mode in low performance, energy-constrained applications. For dynamic sleep transistors and body bias are used in conjunction with clock gating to control active leakage in CMOS technology. The SCPG technique achieves through two mechanisms, the first technique is power gating the combinational logic within the clock period and the second technique is reducing the virtual supply to less than threshold voltage. A power gating structure that supports both a cut off mode, intermediate power saving and data retaining mode. By using of Tanner EDA tool, we can achieve power reduction.

Keywords: Active mode, low power, power gating, sub threshold, Tanner EDA

I.INTRODUCTION

The power reduction is done by using sub clock power gating technique. a pair of nmos and pmos transistors are used in the head and foot of the power gated logic. for dynamic sleep transistors and body bias are used in the conjunction with clock gating to control active leakage in CMOS technology. the SCPG technique achieve through two mechanisms, the first technique is power gating the combinational logic within the clock period and the second technique is reducing the virtual supply to less than threshold voltage. In multiple sleep mode power gating technique it represents a different point in the wakeup overhead versus leakage saving design space.

In this paper aim to reducing the active leakage power using some logic gates. The logic gate plays that the important role for all digital components. These include dual sub threshold logic. This uses high threshold voltage logic gates on non-critical timing paths and adaptive body biasing. This raises or lowers the threshold voltage of transistor for active power management. The effectiveness of power gating to Reduce leakage power has been demonstrated during active mode.We used a technique, called sub clock power gating(SCPG), targeted reach applications that demand low power performance is not a primary concern.

This results from low performance operation at a fixed bed. Power reduction is achieved by power gating within the clock period to reduce leakage power during active mode. To generate this voltage, Dynamic power gating of both the power (Vdd) and ground (Vss) supplies is proposed and can be achieved through the use of both an **nMOS** and **pMOS** transistor at the head and foot of the power

A. Related work

To use a dual threshold technique to reduce the power dissipation in Active mode power gating. This technique is only used for the CMOS Inverter. To connect the head and foot of the transistor to reduce the power[1]-[4]. A finer granularity power gating has been proposed in disabling executional units during active mode. A method of power gating part of multiplier depending on the data width during run time was proposed in. a guanularity akin to clock gating use the clock enable signal to power gate an integer execution core, in other hand to use the fan in logic. Rather than power gating the proposed technique provides a less than Vth voltage across the combinational logic to minimize power mode transition energy overheads.[5-9]. Therefore, development of power and efficient dual sub clock approaches which can work under such relaxed power constraints is highly desirable.

B .Proposed work

To achieve leakage power dissipation, there are two main tasks to be followed: our first technique is a static power gating and second technique is dynamic power gating using logic gates. In static method, the pair of nMOS and pMOS transistors is connected at the head of the circuit.This process is also called as reverse body bias. Body biasing has been londed considered as an effect and relatively easy way to compensate for some the process variations.

Not only does it leads to a tighter performance distribution and better yield, but also mitigating the guard band

requirements for process corners and temperature variation, it leads to better performance and faster design cycle.In the dynamic power gating method, a pair of nMOS and pMOS transistors are connected at the footer of the circuit. This process is known as a negative feedback method. Negative feedback occurs when some function of the output of a system, process, or mechanism is fed back in a manner that tends to reduce the fluctuations in the output, whether caused by changes in the input or by other disturbances.

C.Process

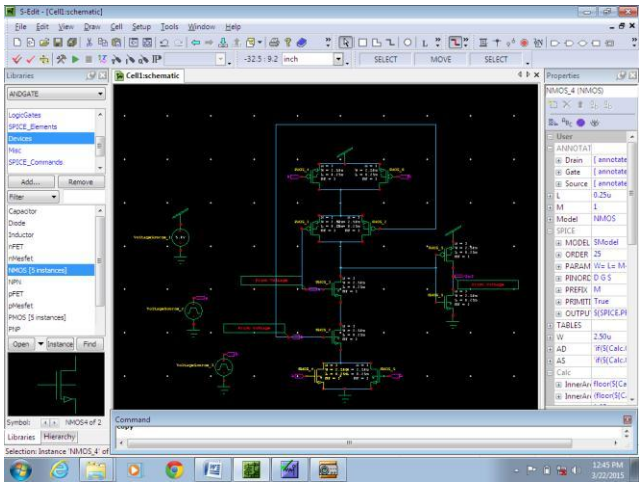


Fig. 1 CMOS AND gate using static and dynamic logic

The CMOS Inverter circuit is designed by using of static and dynamic power gating .In this circuit,When it is in *Sleep* and *Ret* are logic 1 (and thus *n Sleep* and *n Ret* are logic0) the *VV*dd is clamped to *V* dd −*V*thn and the *VV*ss is clamped to *V*ss + *V* thp. The result is a much more aggressive reduction in voltage across the power gated logic,but also has three advantages over single rail clamping.

When the clock is logic 1, ISOLATE is driven to logic 1, thereby isolating the combinational outputs. When the clock is logic 0, ISOLATE is held at logic 1 while the *VV*dd input remains at logic 0 (clamped) . This ensures the combinational outputs remain isolated until the supply rail is charged to an equivalent logic 1, eliminating short-circuit currents during wake-up. The use of a *VV*ss is unnecessary as the pairs of nMOS and pMOS transistors are assumed to be balanced to ensure equal voltage drop and charge/discharge times. The n-Override signal ensures that if the SCPG technique is disabled, additional dynamic power is not consumed by the isolation being activated in every clock cycle.

II.SCPG TECHNIQUE USING UNIVERSAL GATES

A NOR gate circuit is designed by using Tanner EDA tool. In S-edit, the schematic for nand is to be drawn. This circuit is designed using a pair of nMOS transistor connected at the header.

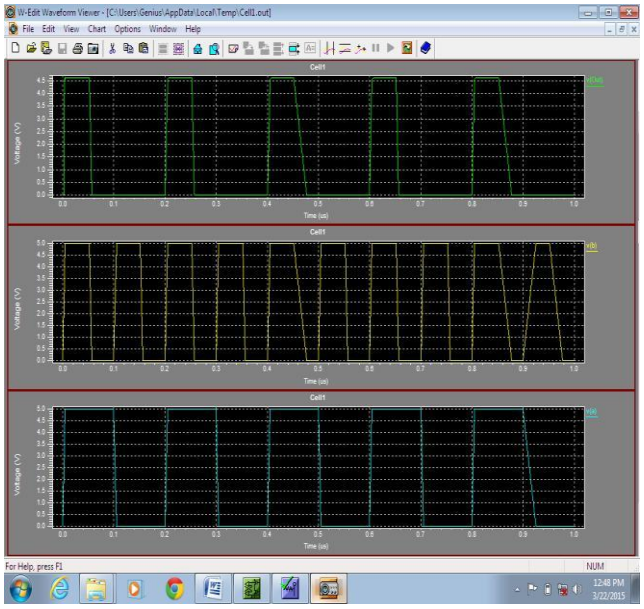


Fig. 2 AND using static and dynamic logic waveform

It will act as a reverse body biasing and to eliminate the leakage power. And a pair of pMOS connects at the footer to avoid negative feedback, these negative feedback current no sent the power in main circuit. So the unwanted leakage problem can be reduced. This process is fabricated in 65nm technology so area is not exceed.

The waveforms for Multiplexer is found in W-edit and the power results are found in the T-spice, it displays the output measures of power.

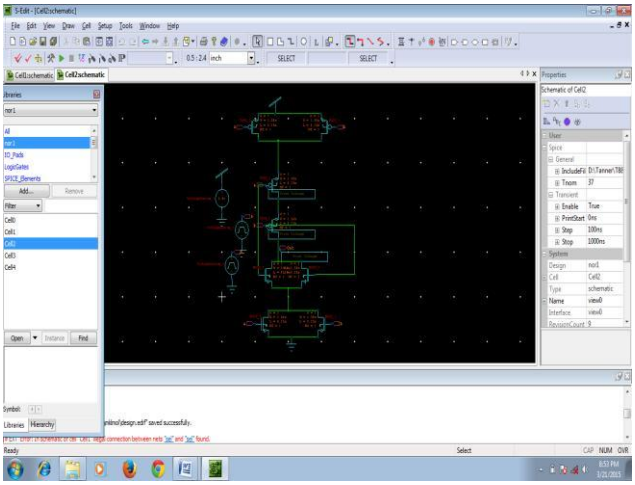


Fig. 3 NOR gate using static and dynamic logic

We saw the output as leakage power reduction in high percentage. Therefore, we use the technique static and dynamic power gating to reduce the power and to increase the efficiency of the circuit.

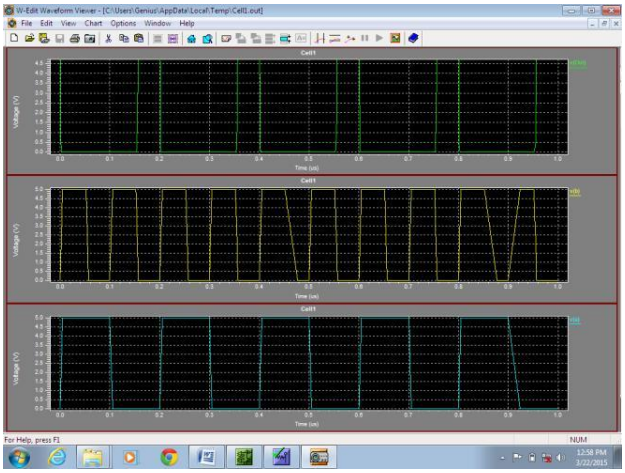


Fig.4.NOR gate using static and dynamic logic waveform

IV. IMPLEMENTATION

The proposed dual SCPG technique has been proven by implementing the full adder circuit within a chip. Mostly used in universal gates and multiplexer circuit to achieve through power reduction using sub clock power gating technique.

In normal circuit, it consumes 5v-10v, but using of these techniques our required voltage is reduced to 2v-5v. so, we can achieve minimum leakage power and less power consumption and it also produces the output as more efficient manner.The 2:1 multiplexer circuit output will be select line is 0,the output is B it depends on the input B.The select line is 1,the putput will be A it depends on the input A.

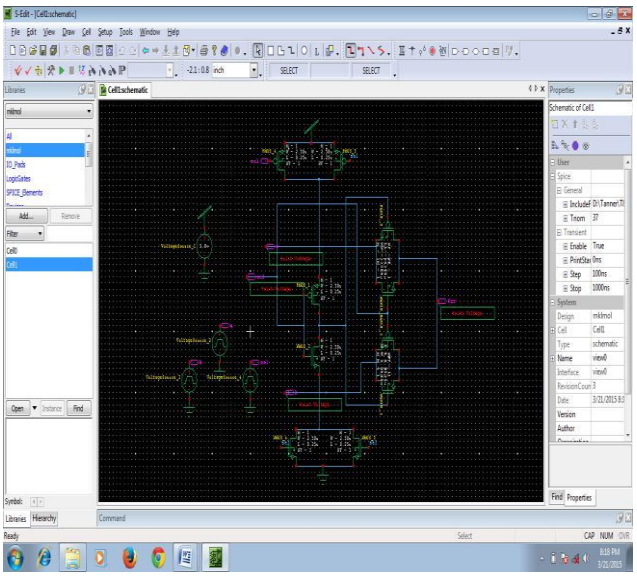


Fig. 6 Multiplexer using static and dynamic logic circuit

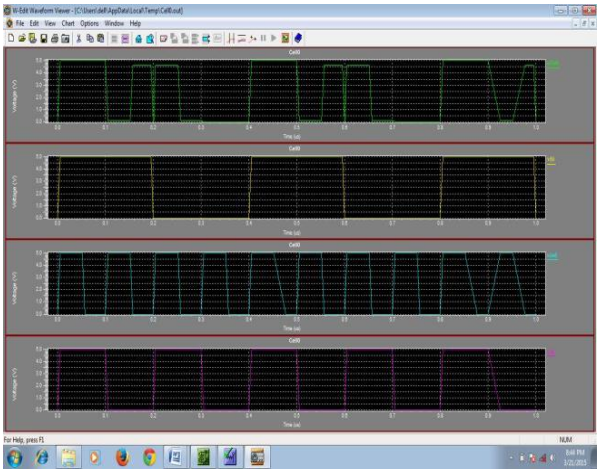


Fig.7 MUX using static and dynamic logic waveform

III. COMPARISON TABLE FOR INVERTER and UNIVERSAL GATE POWER OUTPUT

Fig.8.static power consumption

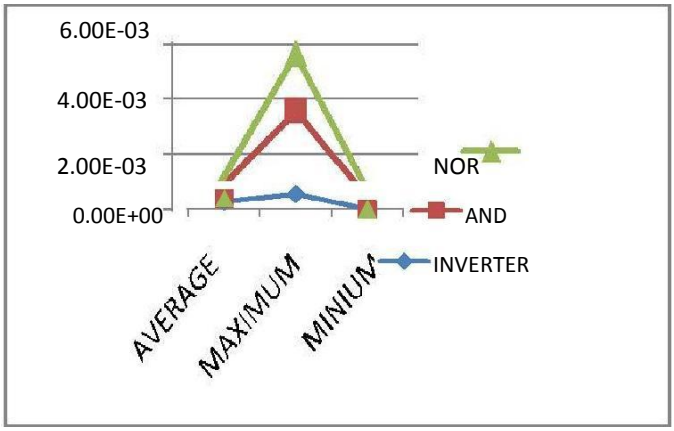
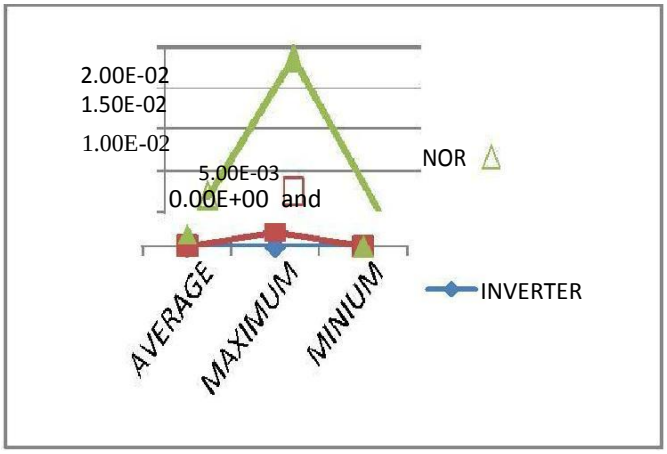


Fig.9. dynamic power consumption



V. CONCLUSION

This paper has proposed a power gating technique that reduces leakage power during the active mode for low performance, energy-constrained applications with power gating combinational logic within the clock period. Rather than shutting down completely, symmetric virtual rail clamping was proposed to reduce wake-up power mode transition energy cost. The proposed SCPG with symmetric virtual rail clamping technique has been implemented full adder circuits, fabricated in 65-nm technology. To reduce the average power by up to 67% during the active mode, SCPG can achieve a 47% reduction in power and improvements in energy efficiency. It avoids increased design complexity, making it fully compatible with standard EDA tool.

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