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Design of Carry Select Adder with Reduced Area and Power

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***Abstract*— Adders are the most fundamental importance in a wide variety of digital systems. Among the fast adders exist, but fast adding using low area and power is still challenging. Several new adders based on the new carry select adder structure are proposed. Comparison with well-known conventional adders demonstrates that the usage of carry-strength signals allows high-speed adders to be realised at significantly lower cost and also consuming lower power. Data-dependency and redundant logic operations are identified and which cannot be eliminated, in binary to excess-1 converter (BEC) based conventional carry select adder (CSLA). By using the BEC based on CSLA architecture, the area delay product (ADP) is high. The proposed CSLA is being designed by Pass transistor logic (PTL) technique for further reduction of area and power. By using Pass transistor logic the number of transistor used for each logical circuit is reduced so that the area and power consumption has been reduced for the carry select adder.The simulation is carried out using Tanner EDA tool.**

***Index terms* - Carry select adder, Area delay product, Pass transistor logic.**

I. INTRODUCTION

The adders play an important role in a digital system for its fast and low cost binary properties. They are necessary for computing the physical address in virtually every memory fetch operation in CPUs and also used in every arithmetic operation. Adders are also used in other digital systems like telecommunications systems, where a full-fledged CPU performs unnecessarily.

Adders play a role of heart for computational circuits and other complex arithmetic circuits, based on its addition. Its arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. These adder cells mainly designed to increase speed and also to reduce more power consumption. Various approaches realizing adders CMOS technologies also investigated by these studies. It is necessary for designers to work within a very tight leakage power specification in order to meet product battery life and package cost objectives for mobile applications.

Adder is still plays an important role though many people focus on more complex computation such as multiplier, divider, cordic circuits in arithmetic computatios. There is no general architecture for measuring performance equally, so several algorithms and architectures are implemented in literature to overcome issues after under different conditions which possibly result in variant performance even implemented with the same algorithm.

II. CARRY SELECT ADDER

Low-power, area-efficient and high-performance VLSI systems are increasingly used in portable and mobile devices, multi-standard wireless receivers, and bio-medical Instrumentation due to its Low-power, area-efficient and high-performance. The main component of arithmetic unit is Adder. Some digital signal processing (DSP) system involved in several adders. An efficient adder design practically improves the performance of complex DSP system.

The most substantial areas of research in VLSI system design are Design of area- and power-efficient high-speed data path logic systems. The speed of addition is limited by the time required to propagate a carry through the adder ,in digital adders. After the previous bit position has been summed and a carry propagated into the next position, the sum for each bit position in an elementary adder is sequently generated. In computational systems, CSLA is used to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

It uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin and Cout then the final sum and carry are selected by the multiplexers (mux) because, the CSLA is not area efficient. Depends upon the great extent on the type of design style used for implementation as well as the logic function realized using the particular design style, full adder performs their function. To achieve a reasonable power delay product with high noise margins, regular layout and relatively higher tolerance to process variations, CMOS implementation allows circuits.

Yielding extremely fast design and paying higher costs in the overall power consumption, in Dynamic implementations. The two design styles which allow high performance dynamic circuit design without the additional power consumption in the clock distribution network are Data driven dynamic logic and Split pre-charge data driven dynamic logic and also they form interesting implementation strategies for realizing high performance, power-efficient full adders. One of the most critical design factors in modern VLSI design is Power consumption.

The two input bits A and B and creates a true and partial sum from them takes place in carry-select adder and these goes into a multiplexer which chooses the correct output based on the actual carry in. Fig 1 shows 4-bit Carry-select adders are made by linking 2 adders together, one being fed a constant 0-carry, the other a constant 1-carry. It calculate the power delay product means measures the energy consumed per switching event.

The advantages of carry select adder is simple but rather fast, it performs fast arithmetic functions, low power. It reduces the propagation delay.

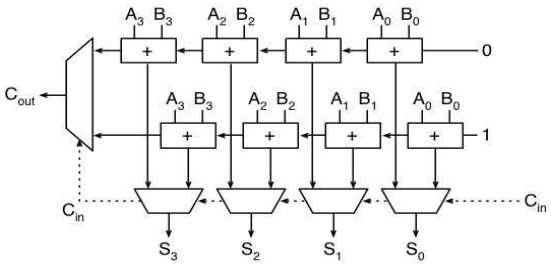

Fig 1: 4-bit carry select adder

One of the fastest adders used in many data-processing processors is Carry Select Adder (CSLA) and these are designed to perform fast arithmetic functions. The scope for reducing the area and power consumption in the CSLA is explained from the structure of the CSLA. Simple and efficient gate-level modification is used in this work to significantly reduce the area and power of the CSLA. CLA shows the good performance while using in high speed adder have been proved. This architecture are used commonly in many papers.

III. PASS TRANSISTOR LOGIC

Several logic families used in the design of integrated circuits is described by **pass transistor logic** (PTL) in electronics. The count of transistors is reduced to make different logic gates, by eliminating redundant transistors. Transistors serves as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages.

Designers must take care to assess the effects of unintentional paths within the circuit, due to there is less isolation between input signals and outputs. Design rules restrict the arrangement of circuits for proper operation, for avoiding sneak paths, charge sharing, and slow switching. Simulation of circuits may be required to ensure adequate performance.

I nput is applied to gate terminal of transistor in conventional logic families. Input is also applied to source /drain terminal, in PTL. These circuits serves as a switches use either NMOS transistors or parallel pair of NMOS and PMOS transistor called Transmission gate. Here the width of PMOS is taken equal to NMOS so that it makes both transistors can pass the signal simultaneously in parallel.

Using both the source (or drain) and the gate, its high functionality, PTL can propagate signals, so that it can reduce the number of transistors in the critical path. Only one type of MOS transistor (generally an nmos transistor) ,is contained in PTL-based circuit, because it has a low node capacitance. As a result, PTL enables high-speed and low-power digital circuits.

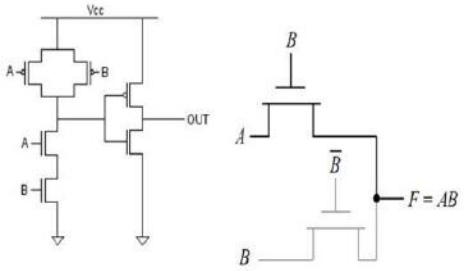

Fig 2: AND gate and AND gate using PTL

IV. OPERATION

The particular way to implement an adder is carry select adder, which is a logic element that computes the (n+1) bit sum of n-bit numbers. In order to perform the calculation time, one time with the assumption of carry being zero, and other assume one, it has simple and adding n-bit numbers with a carry select adder is done with two adders. After two results calculated, the correct sum and carry is selected with the multiplexer one the correct carry is known.

The carry select adder consists of two ripple carry adders and one multiplexer. The ripple carry adder includes series of full adders. The full adder consist of AND, OR, XOR gates. For example the fig 2, shows normal AND gate includes six transistors. It occupies large area and more power. But the pass transistor logic using AND gate includes two transistors for the same operation. So it reduces the transistor count when automatically reduce the area and power.

The proposed pass transistor logic requires less power than the same function implemented with the same transistors in fully complementary CMOS logic. It can be also reduced the propagation delay. Propagation delay means when an input to the circuit changes until that change propagates though the circuit and changes the output. It is also called gate delay.

V. PERFORMANCE EVALUATION

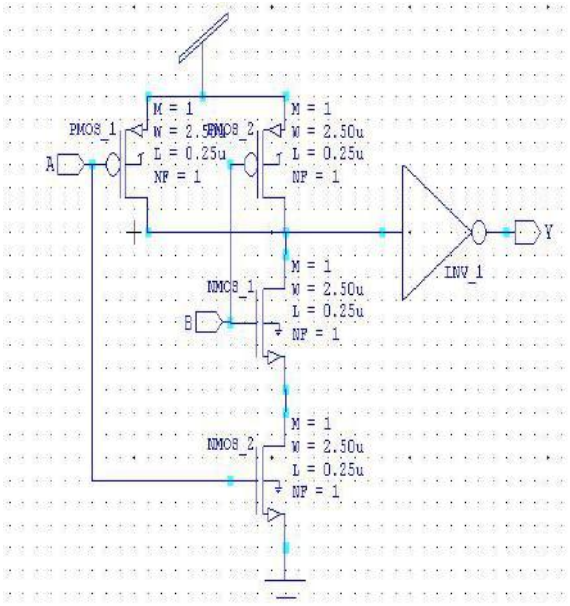

Fig 3:AND gate

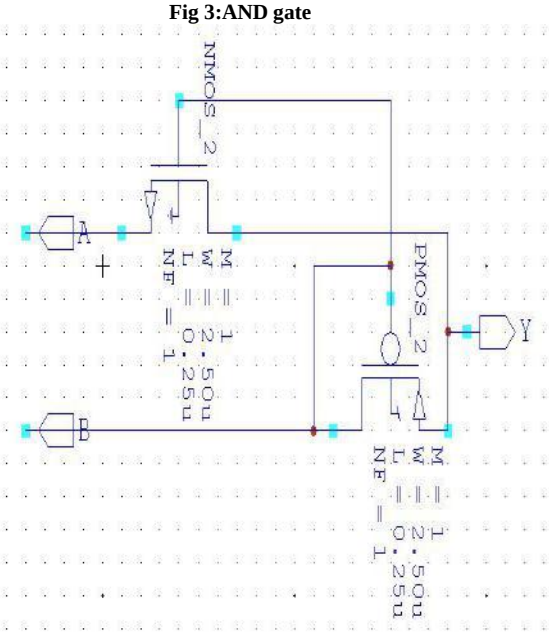

Fig 4: AND gate using PTL

The above fig shows normal AND gate consist of six transistor and the proposed pass transistor logic reducing the transistor count in two for same operation. So the area also get minimized and power value also reduced.

A. *Circuit Diagram Of CSA*

Fig 5 shows circuit diagram of carry select adder by using full adder and ripple carry adder and analyzed the output.

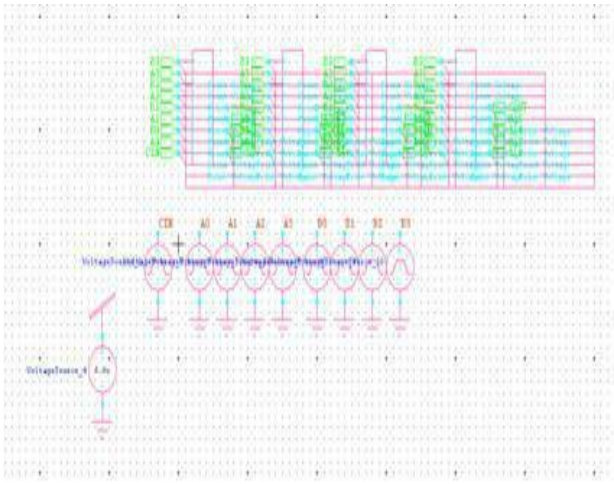

Fig 5: Circuit diagram of CSA

B. *Simulation Output*

Fig 6 shows output waveform of carry select adder inputs are Cin,A0,A1…and B0,B1…then the output is Cout,S0….to analyze sum and carry output.

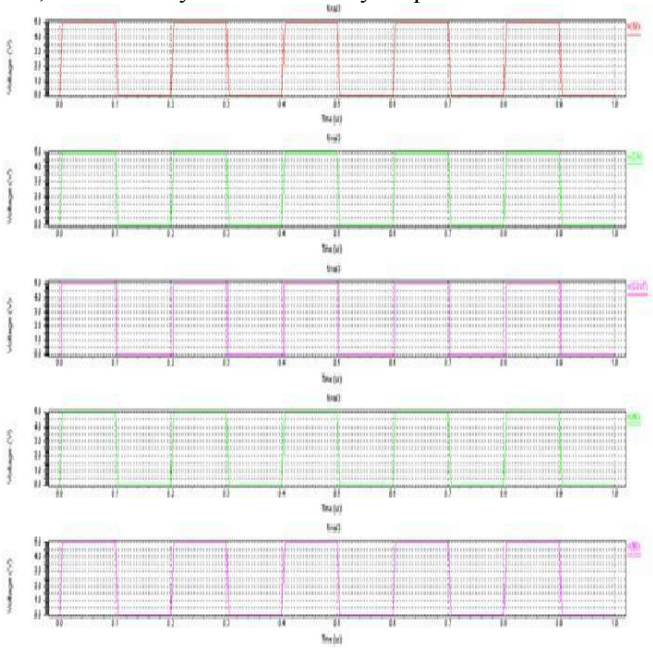

Fig 6: Output waveform of CSA

C. *Proposed PTL Circuit*

Fig 7 shows circuit diagram of carry select adder using PTL, it can be included in the PTL logic to analyzed output.

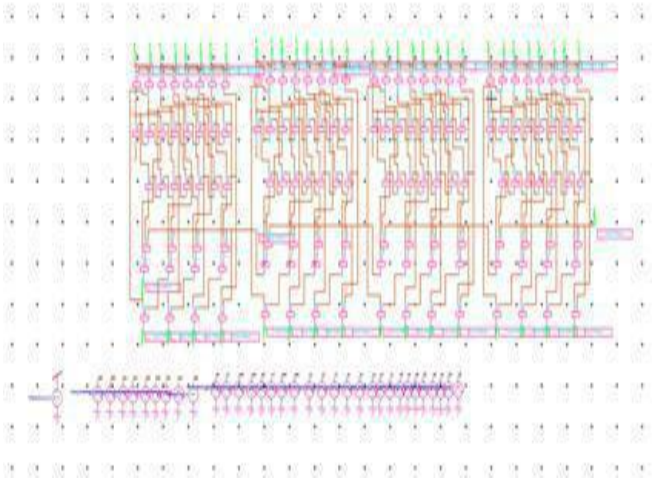

Fig 7: Circuit diagram of CSA using PTL

D. Simulation Output

Fig 8 shows output waveform of carry select adder using PTL inputs are Cin,A0,A1…B0,B1… then the outputs are Cout,S0…. and to analyze sum and carry output.

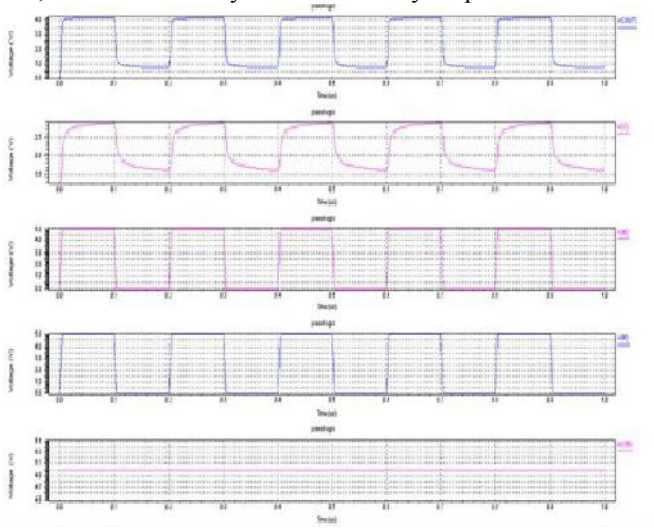

Fig 8: Output waveform of CSA using PTL

VI. Results And Discussion

From the results the proposed carry select adder using pass transistor logic technique reducing the transistor count, area and power. The adder output is produced. The carry select adder inputs are A,B,Cin and the output is Cout. The power value obtained 8.299242e-002 w. the proposed CSA using PTL logic inputs are A,B,Cin and the output is Cout, the power value obtained 3.228994e-002 w.

PARAMETER	NORMAL CSA	CSA using PTL
POWER CONSUMPTION (Watts)	8.299242e-002 w	3.228994e-002 w

Fig 9: Tabulation of power consumption

A. Power Consumption

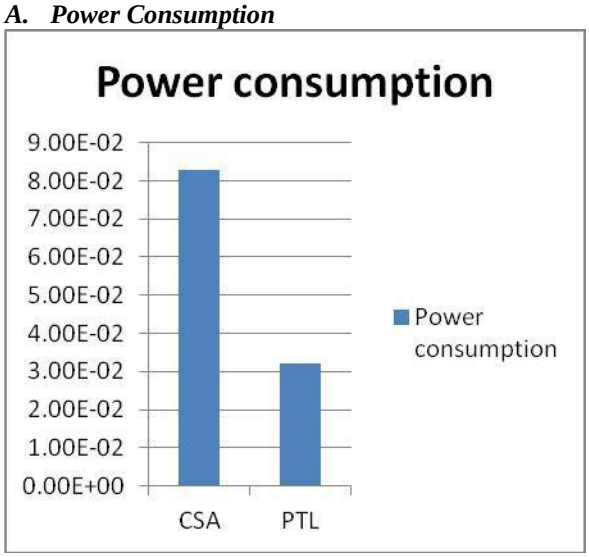

Fig 10. Graph for CSA and PTL

From the above fig, it shows power comparison results. The relation between carry select adder and carry select adder using PTL. The carry select adder using PTL is reduced the power value when compared to the normal carry select adder. The output waveform can be simulated with the help of Tanner EDA tool.

VII. Conclusion

A carry select adder is designed and the power consumption is reduced using the proposed PTL technique which is the best one to decreases the number of transistors. The number of transistor for each logical circuits was reduced using the proposed pass transistor logic. It can be also reduced the propagation delay and redundant transistors .The PTL technique is used to reduce the complexity in transistor level so as to achieve the less area and power.

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