International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:2682
Vol.4, No.10, October 2015 DOI:10.15693/ijaist/2015.v4i2.242-247

Design of High Speed Low Power Binary Content Addressable Memory for Packet Classification

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***Abstract*—Packet classification is the core mechanism that enables many networking devices. Also using Ternary Content Addressable Memories (TCAMs) to perform high speed packet classification has become the widely adopted solutions. TCAMs are very expensive, have limited capacity, consume large amount of power , and generate tremendous amount of heat because of their extremely dense and parallel circuitry. In this paper, we propose the first packet classification scheme that uses Binary Content Addressable Memories (BCAMs). BCAMs are similar to TCAMs except that in BCAMs, every bit has only two possible states: 0 or 1; in contrast, in TCAMs, every bit has three possible states: 0, 1, or * (don't care). Because of the high complexity in implementing the extra "don't care" state, TCAMs have much higher circuit density than BCAMs. As the power consumption, heat generation, and price grow non-linearly with circuit density, BCAMs consume much less power, generate much less heat, and cost much less money than TCAMs. The main objective of this project is to design a BCAM based packet router for packet classification with packet switching network on a single chip. Also optimization ofarea and performance. The path for a data packet between a source and a destination through the routers is denied by the routing algorithm. We evaluated our BCAM scheme on 17 real-life packet classifiers. On these classifiers, our BCAM scheme requires roughly 5 times fewer CAM bits than the traditional TCAM based scheme. The penalty is a throughput that is roughly 4 times less.**

Index terms -CMOS, content addressable memory (CAM), Ternary Content Addressable Memory (TCAM), Binary Content Addressable Memory (BCAM).

I. INTRODUCTION

Content addressable memory (CAM) is a type of solidstate memory. In general, a CAM has three operationsModes: READ, WRITE, and COMPARE [4].The comparison operation is performing to n-input search word into the search Data register CAM [1]. Due to its parallel match-line comparison, CAM is power-hungry. The recent developments in the design of large-capacity content-addressable memory (CAM). A CAM is a memory that implements the lookuptable function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in networkrouters for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high-speed table lookup. However,the speed of a CAM comes at the cost of increased silicon area and powerconsumption, two design parameters that designers strive toreduce. As CAM applications grow, demanding larger CAM. A size, the power problem is further exacerbated. Reducingpower consumption, without sacrificing speed or area, is the main thread of recent research in large-capacity CAMs.

The developments in the CAM area at two levels: circuits and architectures. First briefly introduce the operation of CAM and also describe the CAM application of packet forwarding. The input to the system is the search word that is broadcast onto the search lines to the table of stored data. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits [1]. A typicalCAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits. Each stored word has amatchline that indicates whether the search word and stored word are identical (the match case) or are different (a mismatch case, or miss).

The match lines are fed to an encoder that generates abinary match location corresponding to the matchline that is inthe match state. An encoder is used in systems where only asingle match is expected. The operation of a CAM is like thatof the tag portion of a fully associative cache. Many circuitsare common to both CAMs and caches; however, we focus onlarge capacity CAMs rather than on fully associative caches,which target smaller capacity and higher speed.

Today's largest commercially available single-chip CAMsare 18 Mbit implementations, although the largest CAMsreported in the literature are 9 Mbit in size [1]. As a rule ofthumb, the largest available CAM chip is usually about half the size of the largest available SRAM chip. This rule of thumb comes from the fact that a typical CAM

cell consists of two SRAM cells, as we will see shortly. Chips versus timefrom 1985 to 2004, revealing an exponential growth rate.

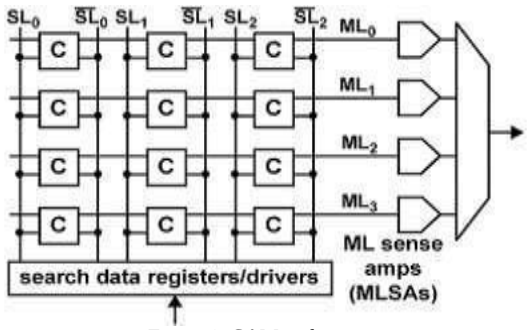

Figure 1. CAM architecture

It consists of core cells. Search line, match line, MLSA and an encoder. Search data register is used to get the input from user, and will be compared with the memory bank through search line. Matchlinesensing amplifiers are used to sense the voltage variationsfrom the matchline. Encoder is used to identify the location of the output [1]. CAM search operation begins with pre-charging all match lines high, putting them all temporarily in the match state. The match lines are inputs to an encoder that generates the address corresponding to the match location. The content addressable memory is the modification of random access memory. Random Access Memory consist of read, write operation, Content Addressable Memory consist of read, write, and comparison operation.

II. Related Work

Each CAM cell is powered by two power rails VDDML for the compare transistors, VDD for the SRAM transistors. The rail VDDML of a row is connected to the power network VDDC via a p-MOS device Px which is used to limit the transient current. All the cells of a row will share the limited current offered by the transistor Px, despite whatever number of mismatches.

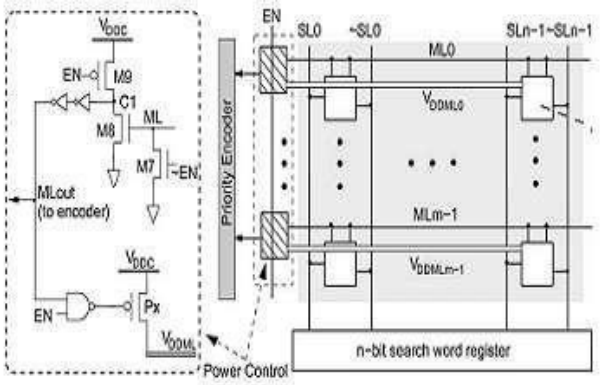

Figure2. Previously proposed structure

At the beginning of each cycle, the ML is first initialized by a global control signal EN. At this time signal EN is set to low and the power transistor Pxis turned OFF. CAM can be used to accelerate any applications ranging from local-area networks, database management, file-storage management, pattern recognition, artificial intelligence, fully associative and processor-specific cache memories, and disk cache memories. This will make the signal ML a C1 initialized to ground and VDD, respectively. After that, signal EN turns HIGH and initiates the COMPARE phase. If one or more mismatches happened the CAM cells, the ML will be charged up. After a certain but very minor delay, the NAND2 gate will be toggled and thus the power transistor (PX) is turned off again. As a result, the ML is not fully charged to VDD but limited to some voltage slightly above the threshold voltage of M8.

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III. Proposed Binary Content Addressable Memory For Packet Classification

A. Objectives

The main objective of this project is to design a BCAM based packet router for packet classification with packet switching network on a single chip. Also Optimization of Area and Performance. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm.A CAM has three major operations:

- Write into the next free location
- Search for a word match.
- Read matching entries.

Data may be transferred to or from an CAM withoutknowing the memory address2 of the word. Binary datais automatically written to the next free word. T o read aword the user must first do a search operation. Then, ifthere are multiple matches, the CAM decides (based onsome internal state) which matched word to read next.Reading is useful because a CAM word has two parts. Themost important part is the search-field, which is the part ofthe word that is matched with the search pattern. Thistypically contains the addresses of the known destinations.The CAM word also contains a return-field, which is theinformation returned during a read. This contains either therelated information or an index.All the CAM lookup algorithms are similar to theparallel search used in a RAM; however, the size of a CAMneeded for direct access is determined primarily by thenumber of words that require storage. The size of the searchfield only affects the number of bits a word requires. Forexample, with a 10-bit search field, 10 bits per word arerequired. Thus, if there were only 256 possible inputs, eachwith a 16-bit search field, the CAM must have 256 words -with each word being at least 16 bits. The size and cost ofa CAM grows linearly with the size of the search field andthe number of entries.

In Binary-CLASS, the first packet classification scheme that uses Binary Content Addressable Memory (BCAM). BCAM works similar to TCAM except that in

BCAM, every bit has only two possible states: 0 or 1; in contrast, in TCAM, every bit has three possible states: 0,1,or*. A BCAM core cell is simpler than a TCAM core cell because it only has a binary state because there is no need for the third ―don't care‖ state. Specifically, there are two types of BCAM core cells: a NORtype BCAM cell and a NAND-type BCAM cell. A NOR-type BCAM cell consists of four comparison transistors and an SRAM cell that has six transistors. A NAND-type BCAM cell consists of three comparison transistors and an SRAM cell that has six transistors. This means TCAM circuitry is about two times denser than BCAM circuitry. T his implies a TCAM chip consumes roughly twice as much power and roughly twice as much board space as an equivalent BCAM chip. Considering the number of transistors and the associated circuits, the circuitry of a TCAM is about two times denser than that of a BCAM.Packet classification is an enabling function for a variety of Internet applications including quality of service, security, monitoring, and multimedia communications. In order to classify a packet as belonging to a particular flow or set of flows, network nodes must perform a search over a set of filters using multiple fields of the packet as the search key.

In general, there have been two major threads of research addressing packet classification, algorithmic and architectural. A few pioneering groups of researchers posed the problem, provided complexity bounds, and offered a collection of algorithmic solutions. Subsequently, the design space has been vigorously explored by many offering new algorithms and improvements on existing algorithms [12].Given the inability of early algorithms to meet performance constraints imposed by high speed links, researchers in industry and academia devised architectural solutions to the problem. This thread of research produced the most widely-used packet classification device technology, Ternary Content Addressable Memory(TCAM). New architectural research combines intelligent algorithms and novel architectures to eliminate many of the unfavorable characteristics of current TCAMs. We observethat the community appears to be converging on a combined algorithmic and architectural approach to the problem. Using a taxonomy based on the high-level approach to the problem and a minimal set of running examples, we provide a survey of the seminal and recent solutions to the problem. It is our hope to foster a deeper understanding of the various packet classification techniques while providing a useful framework for discerning relationships and distinctions.

B. Routing Algorithm

TheInternet is comprised of a mesh of routers interconnected by links. Communication among nodes on the Internet (routers and end-hosts) takes place using the Internet Protocol, commonly known as IP. IP data grams (packets) travel over links from one router to the next on their way towards their final destination. Each router performs aforwarding decision on incoming packets to determine the packet's next-hop router. The capability to forward packets isa requirement for every IP router. Additionally, an IP router may also choose to perform special processing on incoming packets. Examples of special processing include filtering packets for security reasons, delivering packets according to a pre-agreed delay guarantee, treating high priority packets preferentially, and maintaining statistics on the number of packets sent by different networks. Such special processing requires that the router classify incoming packets into one of several f lows— all packets of a flow obey a pre-defined rule and are processed in a similar manner by the router. For example, all packets with the same source IP address may be defined to form a flow. A f low could also be defined by specific values of the destination IP address and by specific protocol values. Throughout thisthesis, we will refer to routers that classify packets into f lows as f low-aware routers.

On the other hand, of low-unaware routers treat each incoming packet individually and we will refer to them as packet-by packet routers. This thesis is about two types of algorithms: (1) algorithms that an IP router uses to decide where to forward packets next, and, (2) algorithms that a flow-aware router uses to classify packets into f lows. In particular, this thesis is about fast and efficient algorithms that enable routers to process many packets per second, and hence increase the capacity of the Internet. This introductory chapter first describes the packet-by-packet router and the method it uses to make the forwarding decision, and then moves on to describe the flow-aware router and the method it uses to classify incoming packets into f lows.

C. Router data packet format

Address Based Routing Algorithm based on advanced XYRouting Algorithm. It by pass an unavailable component in the Network on Chip. It achieves routing error detection. It can differentiate the permanent and transient error.

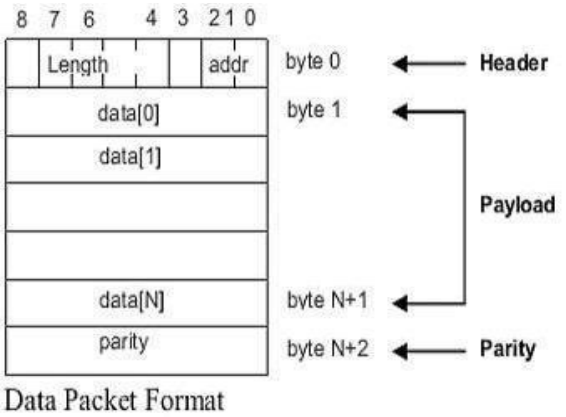

Figure 3. Router data packet format

D. Structure of packet router

The routing algorithm, which defines the path taken by a packet between the source and the destination, is

a main task in network layer design of Network on a Chip. According to where routing decisions are taken, it is possible to classify the routing as source and distributed routing. he XY routing algorithm is one kind of distributed deterministic routing algorithm. XY routing never runs into deadlock or live lock. The XY routing algorithm compares the current router address(Cx, Cy) to the destination router address (Dx,Dy) of the packet, stored in the header flit. There are a couple of

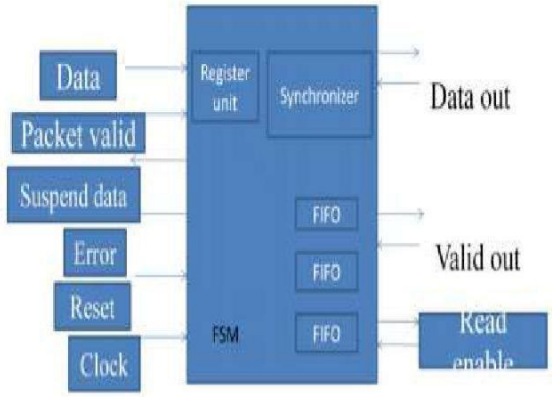

Figure 4. Structure of packet router

The network traffic in Network on Chip network is classified into two types as: Guaranteed Throughput (GT) Traffic Best Performance requirements that every Network on Chip implementation must satisfy: Small latency, guaranteed throughput, Path diversity, Sufficient transfer capacity, Lowpower consumption, Fault and distraction tolerance, Architectural requirements of scalability and programmability Effort (BE) Traffic.

In the proposed system packet switching network is used. The PEs and IPs can be connected directly to any side of a router. Therefore, there is no specific connection port for a PE or IP. Three port networks are used as a router.This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock.Synchronizer is mainly used to perform the synchronization between FSM and FIFO unit. Finite State Machine is used to control all the blocks Finite state machine is the difference between Mealy machine and Moore machine.

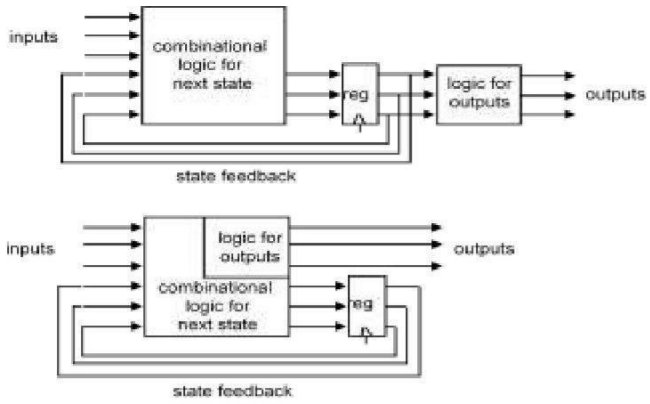

Figure 5. Mealy and Moore machine functional description

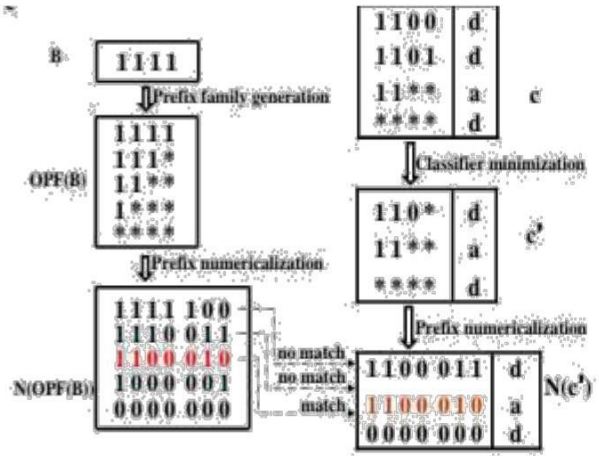

Figure 6. Binary classification on a packet

Our 1-dimensional scheme B-CLASS is composed of two algorithms. The first algorithm describes how to preprocess a classifier so that it can be stored in BCAM. The second algorithm classifies a packet. We first describe the classifier preprocessing. Given a 1-dimensional classifier C, we first convert it to an equivalent minimum prefix classifier C using algorithms in [9], [11]. By minimum, we mean that n equivalent prefix classifier has strictly fewer rules than a minimum prefix classifier. Second, for each prefix P in C′, we convert P to a binary number using the prefix numericalization described above. The preprocessing result N(C′) is stored in a BCAM. We then classify packets using the following algorithm.

Given a packet represented as a w-bit binary number B =b1,b2 · · · bw, we first generate its prefix family PF(B). In particular, we generate the prefixes in PF(B) in the deceasing order of prefix length. We use OPF(B) to denote this ordered prefix family; that is, OPF(B) = hb1,b2 · · · bw, b1,b2 · · ·

bw−1∗, · · ·, b1∗ · · · ∗, ∗∗ ...∗i. Second, we numericalize every prefix in OPF(B) and get N(OPF(B)). The search process starts by testing whether the first element of N(OPF(B))

(i.e.(b1,b2 · · · bw)) is in the BCAM. If yes, then return the corresponding decision; otherwise, continue to test whether the second element of N(OPF(B)) is in the BCAM. This process proceeds until the BCAM returns a match.

IV. Performance Evaluation

We now report our simulation results on the effectiveness and efficiency of B-CLASS-d for a number of real-world packet classifiers as well as large synthetic packet classifiers. As a reminder, we use BCAM lookup time to refer to the number of BCAM lookups performed. For all classifiers, we apply the optimization techniques of minimizing maximum lookup time and minimizing average lookup time in isolation for a better evaluation on the effectiveness of each technique, although minimizing maximum lookup time will reduce the average lookup time and minimizing average lookup time may reduce the maximum lookup time.

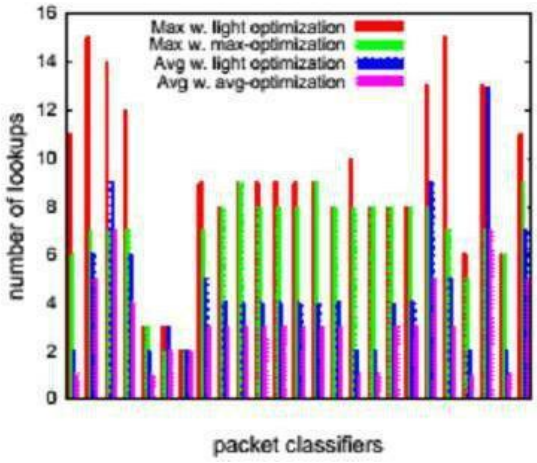

Figure 7. Packet classifier

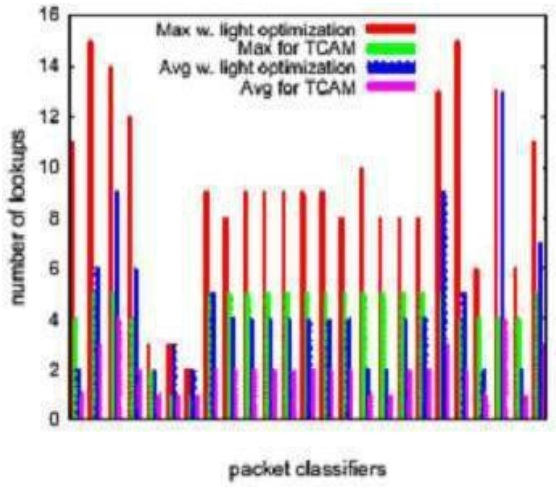

Figure 8. Packet classifier with TCAM

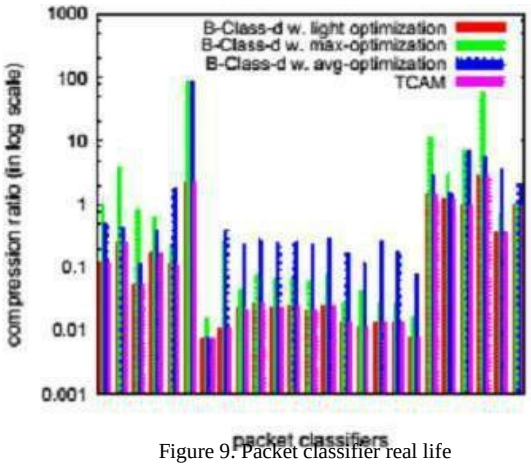

Figure 9. Packet classifier real life

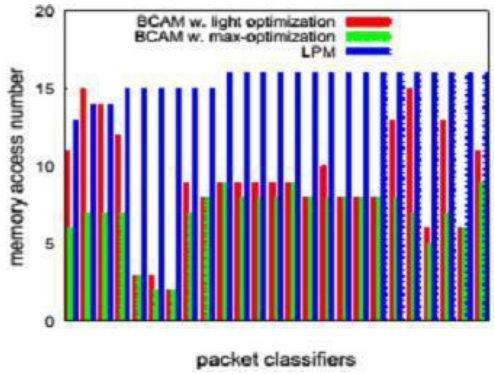

Figure 10. Packet Classifier for maximum lookup time

Because packet classifier rules are considered confidentialDue to security concerns, it is difficult to get many real-livesPacket classifiers for experiments. To address this issue andFurther evaluate the efficiency of our approaches; we generated a set of synthetic packet classifiers of 9 sizes, where each size has 100 independently generated classifiers. Every predicate of a rule in our synthetic packet classifiers has five fields: source IP address, destination IP address, source portnumber, destination port number, and protocol type. We firstrandomly generated a list of values for each field. For IPaddresses, we generated several random class C addresses andthen generated single IP addresses within the class Caddresses; for ports we generated a random range; forprotocols, we chose TCP, UDP, or ICMP. Every field also hasthe —*‖ value included in the list. We then generated a list ofpredicates by taking the cross product of these five lists andrandomly selected from the cross product until we reached ourdesired classifier size by including a final default predicate.Finally, we randomly assigned one of two decisions, accept ordiscard, to each predicate to make a complete rule. The timingresults on the synthetic rules for our BCAM classificationscheme with light optimization.

The maximum (worst case) memory access number for BCLASS-d with only light optimization, B-CLASS-d withmax-optimization and sequential decomposition based longestprefix matching scheme. For B-CLASS-d one BCAM

lookup is counted as one memory access. The maximum lookup timefor B-CLASS-d with light optimization is 15 or lower with an average of 10.4, and it drops to 12 or lower with an average of8.9 if we apply max-optimization. The maximum lookup timefor sequential decomposition based longest prefix matching is16 with an average of 15.48. Note that we count one Bloomfilter query or one hash table lookup as one memory accessfor the sequential decomposition based longest prefixmatching scheme.

VI. CONCLUSION

The significance of this paper lies in Binary-CLASS-d, the first proposed BCAM packet classification scheme, as well as the several optimization techniques such as skip lists, free expansion, an algorithm for minimizing maximum lookup time, an algorithm for minimizing average lookup time, and lookup short circuiting. We implemented B-CLASS-d and conducted experiments on a number of real-life classifiers. Our experimental results validate the practicality of building high performance BCAM based packet classification systems. Furthermore, as this paper opens a new packet classification paradigm, there are many possible future research directions such as developing more efficient and effective algorithms for minimizing the maximum or average lookup time.

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