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A Low Power And Delay Efficient Fixed Point Lms Adaptive Filter With Low Adaptation Delay

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Abstract:

In this architecture, for achieving lower adaptation-delay and area-delay-power efficient implementation, use a novel partial product generator (PPG) and to modify the efficient architecture for the implementation of a delayed least mean square adaptive filter using fixed point LMS algorithm. In the existing system using this filter collateral a desired output is generated, it can be used as a part for mass updating to be observe using conventional adaptive algorithm. It is suitable in many real time DSP processing such as adaptive filters. The conventional adaptive algorithm is used for real-time operation and the same algorithm is used to the conventional existing systems. The output obtained from pipelined FFT is treated as a covet output part in weight updating system of existing conventional adaptive algorithm. This paper presents a precise analysis of the critical path of the least-mean-square (LMS) adaptive filter for deriving the architectures for high-speed and low-complexity implementation.

Key words:Optimized critical path, Least Mean Square algorithm(LMS), Least Mean Square Adaptive Filter, Shift add-tree.

I.Introduction:

THE LEAST MEAN SQUARE (LMS) adaptive filter is the most popular and most widely used adaptive filter, due to its simplicity and its convergence performance[1].Adaptive digital filters find wide application in digital signal processing (DSP) system.

This paper proposes three various structures of the LMS adaptive filter. The first design does not having any adaptation delay, the second design have only one adaptation delay and the third design having two adaptation delay[3].The FIR filter block is designed to reduce the area in an architecture. An architectures that uses several blocks and sub-blocks. All the weights are updated in every cycle to compute the output according to direct-form realization of the FIR filter. The FIR filter block consist of two things. These are sample delay and coefficients.The direct-form LMS adaptive filter is often to have a long critical path due to an inner product computation to obtain the FIR filter output[6]. The critical path of the multiply operation and add operation becomes , where and are the time required for a multiplication operation and an addition operation respectively[5]. The existing system has the three main disadvantages. These are 1)The existing system has more add and multiply operators. And it consumes more power.2)Its accuracy to be low and the path delay also increased.3)The system performance is too low. The shift-add tree that performs the binary addition and multiplication process. Using the shift-add tree the binary bits are spitted into two 8 bits. Each bits perform its binary operation and it performs the power simulation.

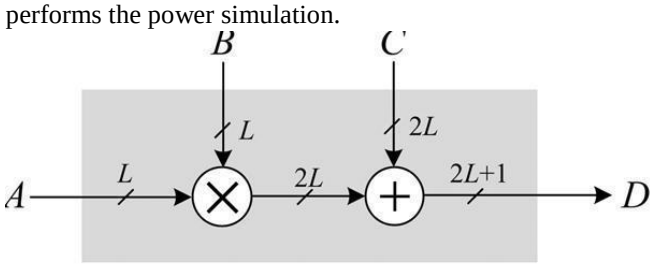

Fig1.Example for multiply-add operation.

The architectures supports the high sampling frequency,but it involves large pipeline depth. It has two adverse of effects, these effects are includes in the register complexity and power dissipation. The second effect is an adaptation delay increases and convergence performance degrades[7] [8].The convergence performance and the power dissipation is varied to each bit cycles. The multiply-add performs the addition of two bits and the multiplication of two bits in the spitted binary values. The transpose-form realization uses the three pipelined stages and the direct-form realization does not use any pipelined stages. So the direct-form realization is more perfect than the transpose-form realization. From the direct-form realization the power and the energy is consumed with its length and it‘s MUF.

Component	0.13-μm		90-nm	
	$L=8$	$L=16$	$L=8$	$L=16$
T_{FAC}	0.21~ 0.23		0.10	
T_{FAS}	0.14~ 0.18		0.1~ 0.16	
T_{ADD}	1.08	2.03	0.74	1.42
T_{MULT}	2.43	4.51	1.54	3.00
T_{MA}	2.79	4.90	1.83	3.29

Table1.for computation delay

The error-computation path is implemented in thepipelined stages [13], and it is used with the input samples that are delayed by the cycles. A generalized block diagram of weight updating in the DLMS adaptive filter is shown in Fig. 3. It consists of an error-computation block and a weight-update. The error update block is used to analyze the error bit in the architectures. Then the error bits are modified and it sends to the circuit block. Each block having the several sub -blocks.

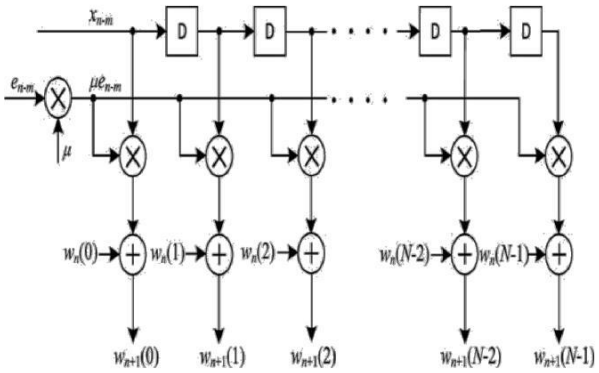

Fig. 3 General Weight Update Diagram

II. Learning of DELAYED LMS ALGORITHM AND ITS IMPLEMENTATION

In this section,the implementation and convergence performance of direct-form and transpose-form. DLMS adaptive filters [11] are discussed. In the delayed LMS algorithm involved in the three types of pipelined concepts in the transpose-form LMS adaptive filter

A. Implementation of a Direct-Form Delayed LMS Algorithm

Computation of the filter output and weight updation could be multiplexed to share the system hardware resources in an adaptive filter structure for reducing with their convergence behavior. In the existing system the work is to modify the filter architecture using fixed point LMS Adaptive algorithm and to reduce the delay unit in filter architecture.the area consumption. It present asystematic then it will result in lower area complexity and less power[6] consumption.Direct-form and transpose-form implementations in the DLMS algorithm.So it consumes low power[3][9].This algorithm used to reduce the path delay and improve the speed compare to proposed algorithm.

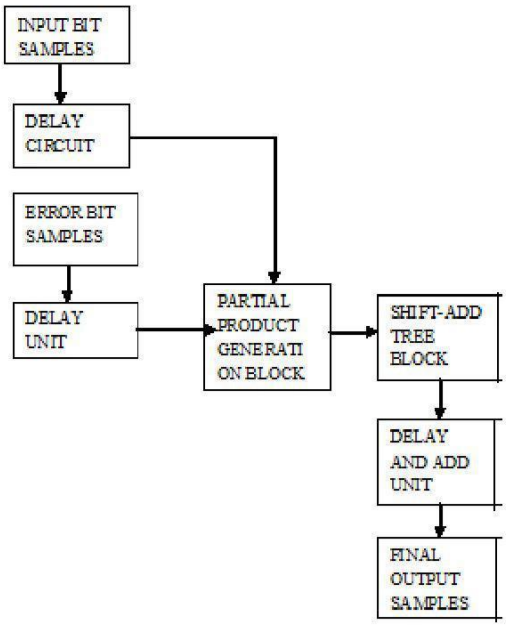

Fig.4 General flow diagram

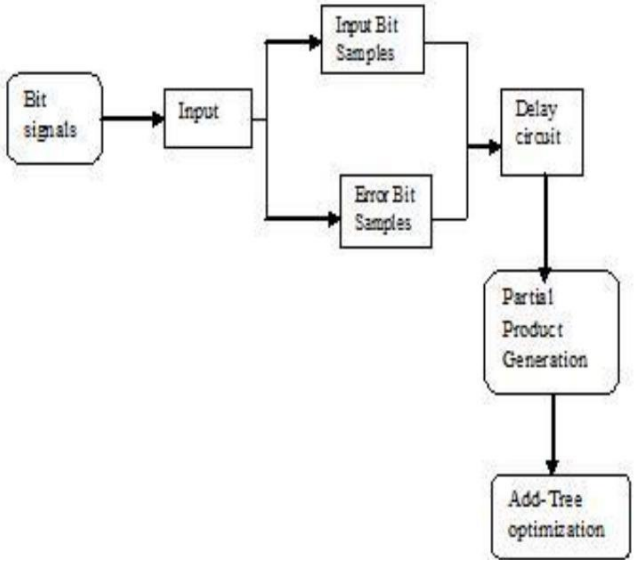

Fig.5 System Architecture

B. Implementation of Transpose-Form Delayed LMS Algorithm:

The transpose-form LMS is a delayed LMS and it provides slower convergence performance. To compare the convergence performance of LMS adaptive filters , we have to simulate the direct-form LMS[13][12], direct-form DLMS, and transpose-form LMS for the same system has an identification problem. The direct-formDLMS adaptive filter with delay 3 also provides faster convergence compared to the transpose-form LMS adaptive filter without any delay.

C.System Architecture:

Bit signals are sent as input signal. It has two blocks like input bit samples and error bit samples.The error bit samples are used to identify the error bits.as shown in fig 5. Then the bit samples are send to the delay circuit, the partial product generation are created and then generate the output bits.

III. ANALYSIS OF LMS ADAPTIVE FILTER AND IMPLEMENTATION:

To find the critical path of the direct-form LMS adaptive filter, an inner product of length 8, and an additions of product words start as soon as the LSBs of products are available[5]. Computations of the first-level adders (ADD-1 and ADD-2) are completed in time.

A.Modules used in the LMS adaptive filter:

There are four modules are used for the LMS adaptive filter. These are i)pre- processing,ii)partial product generation,iii)shift-add architecture,iv)delay-adder unit

i)Pre-processing:

In this pre processing module The input bit to be applying the delay circuit,At the same time the error bit apply the delay unit section.Then the input is sequentially apply to the modified partial protect generation circuit. ii)Partial product generation:

The modified partial protect generation to be apply the input signal and the error signal. The modified PPG circuit used to modify the fixed point LMS adaptive algorithm. The proposed fixed point LMS algorithm to apply the modified PPG architecture. It is used to reduce the pattern count for PPG circuit.

iii)Shift-add architecture:

The modified PPG circuit output to be given to the multiplier architecture.The reduced multiply operator using shift-add tree method.This method used to optimize the multiplier gate count. So reduce the power consumption level.To perform the entire operations for getting the final product, the conventional architecture for shift and add multipliers require many switching activities iv)Delay-adder unit:

The reduced delay-adder unit to be apply the input for shift-add architecture. The delay unit to apply the sequentially in this operation.So the final output to be produced and we using the fixed point LMS adaptive algorithm to reduce the delay circuit and to improve the efficiency of proposed system.

B.Proposed System:

In this paper, we present an efficient architecture for the implementation of a delayed least mean square adaptive filter. Lower adaptation delay and area delay power efficient implementation, that uses the novel partial product generator and propose a strategy for optimized balanced pipelining across the time consuming combinational blocks of the structure. The proposed structure for the weight-update block. It performs N multiply-accumulate operations of the form $(\mu \times e) \times xi + wi$ to update N filter weights.

To present here the optimization of our previously reported design to reduce the number of pipeline delays that are area, energy sample, and power consumption. The proposed design is more efficient in terms of the power-delay product (PDP) and energy-delay product (EDP) compared to the existing structures.

Advantages are,the design approach of the proposed framework to minimize the adaptation delay in the error-calculation block. The proposed scheme could achieve less area and more power reduction correlated with by removing redundant pipeline latches. This paper presents a precise analysis of the critical path of the least-mean-square (LMS) adaptive filter for deriving its architectures for high-speed and low-complexity implementation.The finite impulse responce filter block is designed with the least-mean-square adaptive filter.

The proposed design offers nearly 17% less area-delay product (ADP) and nearly 14% less energy-delay product (EDP) than the best of the existing systolic structures, on average, for filter lengths N = 8, 16, and 32. We propose an efficient fixed-point implementationscheme of the proposed architecture.Here we have proposed a bit-level pruning of the proposed architecture, which provides nearly 20% saving in ADP and 9% saving in EDP over the proposed structure before pruning without noticeable degradation of steady-state-error performance.

IV.Result and Discussion:

Register-transfer level (RTL) is a design abstraction which models a in terms of the flow of digital signals (datathe hardware and logigal operations are performed by the signal register. The FIR filter block created and the signal energy will be reduced. In the hardware description languages the register transfer level is used. The EPS value reduced and the architecture level reduced for area consumption. The energy of the signal and the power and the length of the signals are represented in the simulation diagram. In the simulation the bit signals are spitted into two bit signals. Using the shift-add tree operation the addition and the multiplication operations are performed.

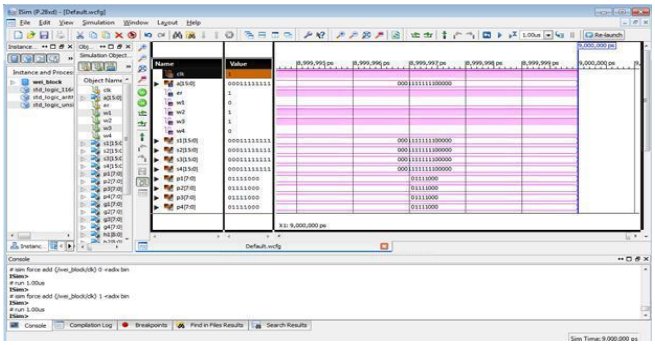

Fig. 6 Simulation result

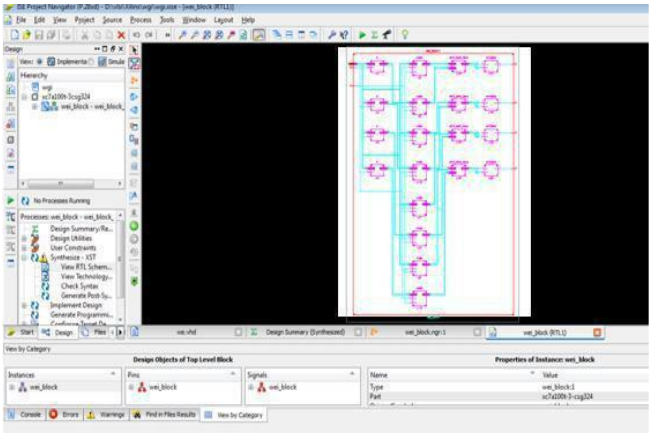

Fig.7 RTL Schematic

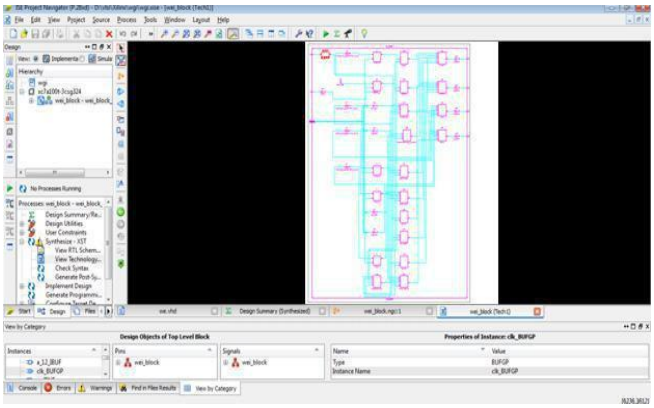

Fig. 8 Technology Schematic

Design	Filter length,N	Area (sq.um)	PCMUF (mW)	EPS (mW x ns)
Two Adaptation delay	8	42729	5.02	16.42
	16	85664	9.92	32.39
	32	171979	19.93	65.10

Table 2 Performance Evaluation

V.Conclusion:

FIR Filter block designed to optimize the PPG unit and it reduces the area and delay power. It reduces the energy per sample(EPS) value upto 85% compared to the existing system. An area and the power are reduced with the FIR filter block. Using the FIR filter block architecture size will be reduced. The direct-form LMS adaptive filter is more efficient than the transpose-form LMS adaptive filter. In tne direct-form LMS structure there is no need of pipelined concept. So it consumes more power than the existing system.Fromthis method,morethan 92% power consumption is possible while using the direct-form structure.

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