International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:2682
Vol.4, No.11, November 2015 DOI:10.15693/ijaist/2015.v4i2.481-486

Design Of Stbc Ofdm Downlink Baseband Receiver For Low Power Applications Using Vlsi Technology

R.Sundarabharathi
PG Scholar
M.E.VLSI DESIGN
Sethu Institute of Technology

R.Naveenkumar
PG Scholar
M.E.VLSI DESIGN
Sethu Institute of Technology

Dr R. Ganesan
PG Program Head
M.E.VLSI DESIGN
Sethu Institute of Technology

Abstract-This paper proposes a space time block code-orthogonal frequency division multiplexing downlink baseband receiver for mobile wireless metropolitan area network. The proposed baseband receiver applied in the system with two transmit antennas and one receive antenna aims to provide high performance in outdoor mobile environments. It provides a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of multipath fading channels. The coded bit error rate performance for 16quadrature amplitude modulation can achieve less than under the vehicle speed of 120 km/hr. The proposed 10-6 receiver designed in 90-nm CMOS technology can support up to 27.32 Mb/s uncoded data transmission under 10MHz channel bandwidth. It requires a core area of 2.41× 2.41 mm and dissipates 34.48 mW at 78.4 MHz with 1 V power supply.

Index Terms : base band receiver,wman , adaptive modulation

I. INTRODUCTION

Next generation portable Internet services require high data rate and mobile capability to provide various multimedia transmissions. IEEE 802.16e standard which usually refers to mobile worldwide interoperability for microwave access (WIMAX) is an extension of IEEE 802.16–2004 for providing mobility of wireless metropolitan area network (WMAN). It is based on an orthogonal frequency division multiple access (OFDMA) technique to support multiple access scheme and multiple-input multiple-output (MIMO) systems over multipath fading channels. Space time block code-orthogonal frequency division multiplexing (STBC-OFDM) systems with multiple antennas can provide diversity gains to improve transmission efficiency and quality of mobile wireless systems but accurate channel state information (CSI) is required for diversity combining, coherent detection, and decoding. Moreover, the system performance is also sensitive to the synchronization error. Therefore, high quality synchronization and channel estimation are two crucial challenges for realizing a successful STBC-OFDM system in outdoor mobile channels. In this paper, an STBC-OFDM downlink baseband receiver for mobile WMAN is proposed and implemented. First, a novel match filter is proposed to precisely detect symbol boundary. Moreover, a ping-pong algorithm is presented to improve the performance of carrier frequency synchronization . Then, we propose a two-stage channel estimator to accurately estimate CSI over fast fading channel.

II.COMMUNICATION

Communication is the process of establishing connection or link between two points for information exchange. For any communication to take place, three things are essential. They are Transmitter, Receiver, Channel or transmission medium. The source generates the message to be transmitted.The transmitter sends the message over the transmission channel. The transmission link can be the medium such as electric conductors, air or light. The receiver receives the message from transmission channel. It is then given to the destination by the receiver. During the transmission over the channel, the message is distorted and it becomes noisy.

A.Wireless Communication

Wireless communication is the transfer of information over a distance without the use of electrical conductors or ―wires‖. The distances involved may be short (a few meters as in television remote control) or long (thousands or millions of kilometers for radio communications). When the context is clear, the term is often shortened to "wireless". Wireless communication is generally considered to be a branch of telecommunications.It encompasses various types of fixed, mobile, and portable two-way radios, cellular telephones, personal digital assistants (PDAs), and wireless networking. Other examples of wireless technology include GPS units, garage door openers and or garage doors, wireless computer mice, keyboards and headsets, satellite television and cordless telephones.

B.Adaptive Modulation

Adaptive modulation is a transmission scheme in digital communications where the transmitter adapts its transmission mode in accordance with the channel. Depending on the condition of the channel, the transmitter could be adapting one or more of the following: constellation size, code rate, and power. Adaptive modulation systems invariably require some channel information at the transmitter. This could be acquired in time division duplex systems by assuming the channel from the transmitter to the receiver is approximately the same as the channel from the receiver to the transmitter.

Adaptive modulation systems improve rate of transmission, and/or bit error rates, by exploiting the channel information that is present at the transmitter. Especially over fading channels which model wireless propagation environments, adaptive modulation systems exhibit great performance enhancements compared to systems that do not exploit channel knowledge at the transmitter. Different order modulations allow you to send more bits per symbol and thus achieve higher throughputs or better spectral efficiencies. However, it must also be noted that when using a modulation technique such as 64-QAM, better signal-to-noise ratios (SNRs) are needed to overcome any interference and maintain a certain bit error ratio (BER). The use of adaptive modulation allows a wireless system to choose the highest order modulation depending on the channel conditions. As you increase your range, you step down to lower modulations (in other words, BPSK), but as you can utilize higher order modulations like QAM for increased throughput. In addition, adaptive modulation allows the system to overcome fading and other interference.Most OFDM systems use a fixed modulation scheme over all carriers for simplicity. However each carrier in a multiuser OFDM system can potentially have a different modulation scheme depending on the channel conditions. Any coherent or differential, phase or amplitude modulation scheme can be used including BPSK, QPSK, 8PSK, 16QAM, 64QAM, etc. Each modulation scheme provides a tradeoff between spectral efficiency and the bit error rate. The spectral efficiency can be maximized by choosing the highest modulation scheme that will give an acceptable Bit Error Rate (BER).

C.STBC OFDM

Space-time block code (STBC)-orthogonal frequency division multiplexing (OFDM) techniques (STBC-OFDM) have been shown to be very promising . With multiple transmit antennas, STBC can provide transmit diversity gain to improve system performance in wireless communications, especially when receive diversity is too expensive to deploy. STBC-OFDM systems have been adopted in IEEE 802.16e which is an extension of IEEE 802.16-2004 for supporting the mobility of wireless metropolitan area network (WMAN). However, for STBC decoding, STBC-OFDM systems require accurate channel state information (CSI), which is particularly difficult to obtain in mobile wireless channels. Therefore, high quality channel estimation with acceptable hardware complexity is a crucial challenge for realizing a successful STBC-OFDM system.

Various channel estimation methods have been proposed for OFDM systems. Among these methods, discrete Fourier transform (DFT)-based channel estimation methods using either minimum mean square error (MMSE) criterion or maximum likelihood (ML) criterion have been studied for OFDM systems with preamble symbols. Since no information on channel statistics or operating signal-to-noise ratio (SNR) is required in the ML scheme, the ML scheme is simpler to implement than the MMSE scheme . Furthermore, when the number of pilots is sufficient, the two schemes have comparable performances. For this reason, the decision-feedback (DF) DFT-based channel estimation method is adopted to use the decided data as pilots to track channel variations for providing sufficient tracking information. Recently, Ku and Huang presented a DF DFT-based method derived from ML criterion and

Newton's method. Moreover, they concluded that a refined two-stage channel estimation method is more robust than the classical DF DFT-based method to apply in fast time-varying channels. Thus, the two-stage channel estimation method with an initialization stage and a tracking stage is adopted in this paper. Nevertheless, the two-stage channel estimation method has high computational complexity and is difficult to realize in hardware directly; hence, a novel architecture and an implementation method shall be proposed to reduce the hardware complexity.

III. DOWNLINK BASEBAND RECEIVER

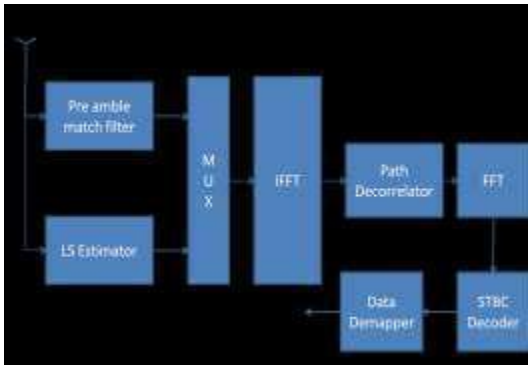

Figure1.Architecture of Downlink baseband receiver

The MPIC-based decorrelation estimates CIR path-by-path and cancels out the known multipath interference. The channel estimation for each transceiver antenna pair can be independently performed because the preambles transmitted from different antennas do not interfere with each other. First, two parameters and are defined as a presumptive path number of a channel and an observation window set, respectively. Second, the cyclic cross-correlation between the received and transmitted preambles as well as the normalized cyclic auto-correlation of the transmitted preamble are calculated. The indexes and which stand for a pathcounting variable and the number of the legal paths found by the MPIC-based decorrelation are initialized to zero. Third, the process is started by picking only one path whose time delay yields the largest value in, for it.

If the path delay is larger than the length of CP, this path is treated as an illegal path and discarded by setting . Otherwise, this path is recorded as the legal path with a time delay and a complex path gain . Then, the interference associated with this legal path is canceled from to obtain a refined cross-correlation function

Meanwhile, is increased by one. The value of is also increased by one at the end of each iteration, and the iterative process is continued until reaches the presumed value.

A.Tracking Stage

After the initialization stage, we can obtain the information of the path numbers, the multipath delays, the multipath complex gains, and the corresponding channel frequency responses, where is corresponding to the transmit antenna. Under the assumption that the multipath delays do not change over the duration of a frame, the DF DFT-based channel estimation method can be equivalently expressed in Newton's method as According to, the vector calculates the difference between the previous estimated channel frequency response vector and the least-square (LS) estimation vector in, where is the iteration index. The matrix is the re-encoded STBC matrix with decided symbols, and, as its entries. The decided symbols are obtained by applying the previous estimated channel frequency responses to decode the received signal vector, where is the symbol index within a time slot. The value is the energy normalization factor.

The inverse DFT (IDFT) matrix multiplying by the vector in is to form the gradient vector in Newton's method, where is a subset of. In addition, the weighting matrix is infact the inverse of the Hessian matrix in Newton's method. The entry of is given by in the previous It is demonstrated that the two-stage channel estimation method has better performance than the classical DF DFT-based method, the STBC-based MMSE method, and the Kalman filtering method for estimating channels in high mobility, and its computational complexity is quite the same with these methods. However, the high complexity problem still needs to be solved for hardware implementation. Hence, we propose a modified two-stage channel estimation method and its architecture for hardware design.

B. FFT/IFFT

The FFT and IFFT are required by the proposed two-stage channel estimator and can be shared by the initialization stage and the tracking stage. A parallel memory-based FFT/IFFT architecture with multiple inputs and outputs in normal order is used to have a lower cost and reduce the latency which is targeted to be less than 1/4 of an OFDM symbol time. The 1024-point

FFT/IFFT module that is composed of eight independent memory modules, four radix-8 processing elements (PEs), two radix-2 butterfly elements, and two commutators. The memory modules are implemented with single-port SRAM modules which consume less area and power than dual-port SRAM modules. The PE adopts the pipelined single-path delay feedback (SDF) FFT architecture with a reorder buffer, a complex multiplier and the associated twiddle factor table.

By the symmetry property of sine/cosine functions, the lookup table just requires to store the sine/cosine values from 0 to 1. For radix-8 FFT operation, the read-out data index of the memory access is the 3-bit reversal of the write-in data index. In order to achieve the parallel inputs and outputs in normal order, the memory access addressing for eight memory modules must avoid the memory conflict occurring. Assume that the binary index of the write-in data is, and the binary index of the read-out data. 3-bit reversalwrite-in index. The parallel write-in data assigned to the eight independent memory modules are based on the addressing scheme. The data located in the different memory modules can be parallel outputted in normal order.

C.STBC Decoder And Demapper

This technique used in wireless communications to transmit multiple copies of data stream a cross a number of antenna and to exploit the various received versions of the data to improve the reliability of data transfer. The fact that the transmitted signal must traverse a potentially difficult environment with scattering,reflection,refraction and so on and may then be future correpted by thermal noise in the receiver means that some of the receiver copies of the data will be better choose In the tracking stage, from , the LS estimator is used to calculate the LS estimations followed by calculating the vector that can be expressed. Before the LS estimation calculation, the decided symbols and must be determined first. Based on the latest estimated channel frequency responses, the STBC decoder the symbol demapper are used to decode these two received symbols and can be formulated as where is the demapper process. The hardware design of a divider is very costly; therefore, a demapping dichotomy method with two stages is adopted to avoid the divider implementation.

.

IV. VLSI DESIGN HIERARCHY

The hierarchical design approach reduces the design complexity by dividing the large system into several sub-modules. Usually, other design concepts and design approaches also needed to simplify the process. Regularity means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much possible.

A. Verilog HDL

The Verilog hardware description language-**[1]**, usually just called Verilog was designed and first implemented by philmoorby at gateway Design automation in 1984 and 1985. It was first used in 1985 and was extended substantially through 1987. The implementation was the verilog simulator sold by gateway. The first major extension was Verilog-XL, which added a few features and implemented the infamous algorithm, which was a very efficient method for doing gate level simulation. This occurred in 1986 and marked the beginning of verilog's growth period. In 1988 synopsis delivered the first logic synthesizer, which used verilog as an input language. This was a major recent as now the top down design methodology could actually be used effectively. The design could be done at the ―register transfer level‖ and then Synopsis design compiler could translate that into gates. With this event, the use of verilog increased dramatically.

B. Field-programmable gate array

A field programmable gate array (FPGA)-**[1]** is a semiconductor device containing programmable logic components and programmable interconnects. The programmable logic components can be programmed to duplicate the functionality of basic logic gates such as AND, OR, XOR, NOT or more complex combinational functions such as decoders or simple math functions. In most FPGA, these programmable logic components (or logic blocks, in FPGA parlance) also include memory elements, which may be simple flip-flops or more complete blocks of memories. A hierarchy of programmable interconnects allows the logic blocks of an FPGA to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard.

so that the FPGA can perform whatever logical function is needed.FPGA are generally slower than their application-specific integrated circuit (ASIC) counterparts, can't handle as complex a design, and draw more power. However, they have several advantages such as a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs.

C. HDL Simulator

The benefits of a full HDL design flow that includes HDL simulation follow: We can quickly generate highly verified designs, simplifying the test and integration task. We can discover problems earlier in the design process .Our productivity is improved .Designs are consistently more robust and more competitive. Design flows are more effective.

HDL simulation allows you to debug your design at the source code level, pinpointing design problems directly to the line of code responsible for the failure. For example, you can stop the simulation whenever a variable changes, or step through a piece of code line by line, or trace a signal flow through a design. HDL simulation supports reusable HDL test benches throughout the verification process. It is easier to let the test bench inspect the design for failures as a way to improve design quality. You can write tests in VHDL or Verilog which apply stimulus to your design and check for the correct response. The same ―self-checking test benches‖ can be used before synthesis, after synthesis, and after place-and-route.

V.SIMULATION RESULTS

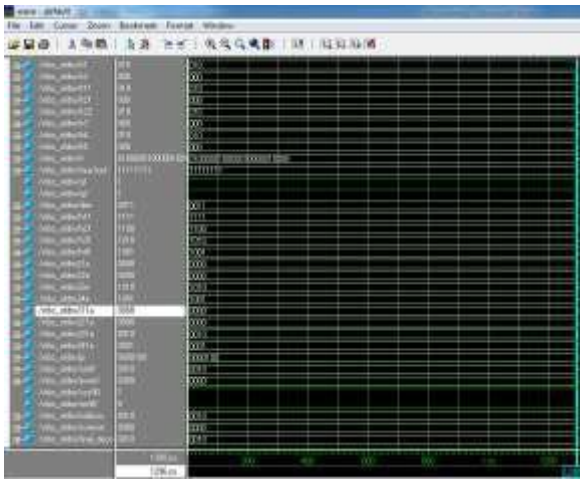

Figure 2. Final output

V.CONCLUSION FUTURE WORK

In this paper, we propose a downlink baseband receiver for mobile WMAN that is applied in the STBC-OFDM system with two transmit antennas and one receive antenna. A simple symbol boundary detector, a carrier frequency recovery loop modified by the ping-pong algorithm, and an accurate two-stage channel estimator are effectively implemented. Although the two-stage channel estimator requires higher hardware cost as compared with the interpolation-based channel estimators,it has significant performance improvement for successfully realizing the STBC-OFDM system in outdoor mobile environments.From the simulation results, we have shown that the proposed receiver improves about 8.5 dB of the normalized MSE for 16QAM modulation as compared with that adopting the 2-D interpolation methods in multipath fading channels.Moreover, under the vehicle speed of 120 km/hr, the convolutional coded BER for 16QAM modulation can achieve less than with coded rate of 1/2. The proposed receiver designed in 90-nm CMOS technology can support up to 27.32 Mbps (uncoded) downlink throughput under 10 MHz channel bandwidth. This design has a core area of mm and dissipates 34.48 mW at 78.4 MHz operating frequency. With verifications through all of the simulations and design results, the proposed baseband receiver can provide a solid foundation for WMAN in fixed and mobile wireless communication.

REFERENCES

[1] S. M. Alamouti, ―A simple transmit diversity technique for wireless communications,‖ *IEEE J. Sel. Areas Commun.*, vol. 16, no. 8, pp. 1451–1458, Oct. 1998.

[2] Y. H. Zeng, W. H. Lam, and T. S. Ng, ―Semiblind channel estimation and equalization for MIMO space-time coded OFDM,‖ *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 463–474, Feb. 2006.

[3] Y. H. Chung and S. M. Phoong, ―Unitary precoders for ST-OFDM systems using alamouti STBC,‖ *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2860–2869, Oct. 2008.

[4] *Local and Metropolitan Area Networks Part 16: Air Interface for Fixed Broadband Wireless Access Systems*, IEEE Std 802.16-2004, Oct. 2004.

[5] *Local and Metropolitan Area Networks Part 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems*, IEEE Std 802.16e- 2005, Feb. 2006.

[6] J. H. Park, M. K. Oh, and D. J. Park, ―New channel estimation exploiting reliable decision-feedback symbols for OFDM systems,‖ in *Proc. Int. Conf. Commun.*, Jun. 2006, pp. 3046–3051.

[7] L. Deneire, P. Vandenameele, L. Van Der Perre, B. Gyselinckx, and M. Engels, ―A low-complexity ML channel

estimator for OFDM,‖ *IEEE Trans. Commun.*, vol. 51, no. 2, pp. 135–140, Feb. 2003.
[8] M. Morelli and U. Mengali, ―A comparison of pilot-aided channel estimation methods for OFDM systems,‖ *IEEE Trans. Signal Process.*, vol. 49, no. 12, pp. 3065–3073, Dec. 2001.
[9] M. L. Ku and C. C. Huang, ―A derivation on the equivalence between Newton's method and DF DFT-based method for channel estimation in OFDM systems,‖ *IEEE Trans. Wireless Commun.*, vol. 7, no. 10, pp. 3982–3987, Oct. 2008.
[10] M. L. Ku and C. C. Huang, ―A refined channel estimation method for STBC/OFDM systems in high-mobility wireless channels,‖ *IEEE Trans. Wireless Commun.*, vol. 7, no. 11, pp. 4312–4320, Nov. 2008.
[11] M. Speth, S. Fechtel, G. Fock, and H. Meyr, ―Optimum receiver design for OFDM-based broadband transmission part II: A case study,‖ *IEEE Trans. Commun.*, vol. 49, no. 4, pp. 571–578, Apr. 2001.
[12] T. A. Lin and C. Y. Lee, ―Predictive equalizer design for DVB-T system,‖ in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, vol. 2, pp. 940–943.

AUTHORS PROFILE

R.Sundara bharathi received her **B.E.** degree in Electronics and communication Engineering from SACS m.a.v.m.m engineering college,alagarkovil,Madurai,Anna University, Chennai, India, in 2011. Pursuing **M.E.** degree in VLSI Design from Sethu Institute of Technology, Anna University, Chennai, India. Her research interest includes digital image processing and Low power VLSI design.

R.Naveen kumar received her **B.E.** degree in Electronics and instrumentation Engineering from sethu institute of tecnology ,kariapatti, Anna University, Chennai, India, in 2014. Pursuing **M.E**. degree in VLSI Design from Sethu Institute of Technology, Anna University, Chennai, India. Her research interest includes digital signal processing and vlsi design.

V. Karthick received his **B.E**. Electronics and Communication Engineering from National Engineering College in the year 2009 and **M.Tech** VLSI DESIGN from Sathyabama University in the year 2011. He is presently working as an Assistant Professor in the department of ECE at Sethu Institute of Technology, India. His research interests include Low Power VLSI and Analog VLSI.