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SRAM Stability Measuremnt In CMOS Technology

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ABSTRACT−SRAM occupies two-third area of VLSI chips. To enhance the performance of these chips, SRAM cell should meet the requirement of lesser power consumption. This paper proposes a technique to accurately estimate the stability of SRAM cell without changing the cell structure. Static noise margin is one of the key metrics to estimate the failure of static random-access memory (SRAM) cell. The main principle is to measure the specific cell's currents with variant supply levels . The measured currents are used to estimate the read stability and the write ability through a nonlinear regression. In the conventional 6T SRAM cell, stability problems also arise during a write operation. But in the 4T-SRAM cell, stability metrics for read and write are surveyed and modified to improve the correlation with the conventional stability definition. TANNER EDA simulation tool has been used for simulation of various parameters like power and delay of SRAM Cells.

Keywords − Static Random Access Memory (SRAM), Static Noise Margin (SNM), read retention voltage(RRV), read-static-noise-margin, read stability and write ability.

I. INTRODUCTION

Technology scaling has led to increasing challenges in designing higher density static random-access memory (SRAM).Conventionally, SRAM yield is predicted either by a static-read margin or a write-noise margin (WNM)[7],[8].The SRAM yield based on these metrics can be rapidly estimated through stochastic simulation techniques such as response surface model or importance sampling . SRAM cells consisting of different number of transistors used to store single bit. It is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit [1].The word static here points that it needs not to be refreshed periodically unlike dynamic random access memory. Sram exhibits data-remanence but still it can be called volatile memory as it eventually loses the data when memory is not powered. This paper suggests a technique to estimate the read stability and the write ability of 4T cells from peripheral measurements of the physical SRAM cells without changing the array structure. The idea is to measure the cell currents from the bitline access with varying supply levels and to use this information to estimate the failure conditions (or stability).

Previouswork in this area has not clearly demonstrated how to use the cell currents to estimate the cell stability.They tried to directly correlate the read/write delay at a single supply to the measured stability, but their correlation (*R2)* is at best 0.6 (0.84 in simulation) for the read stability and 0.65 (0.92 in simulation) for the write ability. Although many papers are published for estimating the noise margins during design stage, most of these estimation techniques cannot be directly applied to the measurements of active SRAM cells.

The driving force for SRAM technology is low power applications.It is a type of memory that uses bi-stable latching circuitry to store each bit. As the conventional techniques cannot be measured without change of the cell structure, their correlations with the conventional stability are discussed. Analysis on the dynamic stability also reveals that the alternative metric, despite measured statically, is a good indicator of the dynamic failure for relatively unstable cells. The estimation technique described in this paper uses a modified in situ current measurement technique. Based on an accurate device model of the fabrication technology, this relationship can be directly used with on-chip measurements to determine a cell's stability. Instead of using a simulation model, the relationship can be derived directly from the onchip measurements to apply to a single SRAM IC or wafer.

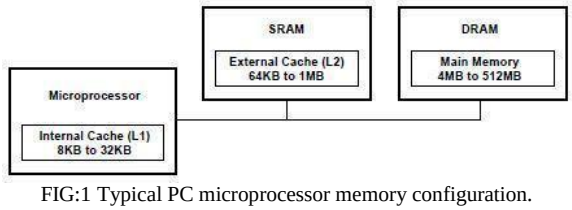

FIG:1 Typical PC microprocessor memory configuration.

Read SNM and Write SNM :

Stability measured in terms of Static Noise Margin(SNM) is defined as the maximum value of DC voltage tolerated by the SRAM cell without changing the stored data [4].Write SNM and Read SNM are the two parameters that defines the stability of cell in write and read mode respectively . To have more stable and much reliable SRAM cell, many different configuration and well optimized cells are proposed in literature but the design of efficient SRAM cell is still a challenging issue.. Despite the simple interpretation, the actual measurement of the RSNM and the WNM requires an internal node access of every single cell and graphical analysis on the measured data[3].

As an alternative way of characterizing the SRAM cell's read stability and write ability, supply read retention voltage (SRRV), and bit-line WTV (BWTV) [3] are chosen that can be characterized by tracking the bit-line current with supply variation without the need to access the internal nodes.

In the conventional techniques they cannot be measured without change of the cell structure and their correlations with the conventional stability are discussed. Analysis on the dynamic stability also reveals that the alternative metric, despite measured statically, is a good indicator of the dynamic failure for relatively unstable cells. The estimation technique described in this paper uses a modified current measurement technique[4]. In this project we explores a method to extract a relationship between the read stability and the cell currents with varying supply levels. Based on an accurate device model of the fabrication technology, this relationship can be directly used with on-chip measurements to determine a cell's stability. Instead of using a simulation model, the relationship can be derived directly from the on-chip measurements to apply to a single SRAM IC or wafer. In the excisiting model we are having the three different modes as given below:

- Standby mode
- Read mode
- Write mode

A. STANDBY MODE

If the word line is not asserted, the access (Pass) transistors will be disconnect . The two cross coupled inverters formed the two inverter connected back to back reinforce each other as long as they are disconnected. And they will retain the data which they have already stored in the memory cell [11].

B. READ MODE

Assume that the content of the memory is a 1,. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line signal with the high voltage pulse. The second step occurs when the values stored in a and b are transferred to the bit lines one of the bit line will discharge through the driver transistor and the other bit lines will be pull up through the Load transistors toward VDD,. If the content of the memory was a 0, the opposite would happen if the memory cell was stored the logic 1 [14].

C. WRITE MODE

The start of a write cycle begins by applying the value to be written to the bit lines. Careful sizing of the transistors in a SRAM cell is needed to ensure proper operation [17].

In the proposed technique ,we are having the three different technique during the 6T SRAM test is given below,

- Read failure test
- Write failure test
- SRRV measurement

RRV is a measurable quantity for an cell by changing the cell supply or word-line driver supply [9]. This discussion focuses on the SRRV as these two metrics are highly correlated. This technique can be used to extract the cell's read stability without changing the cell layout.

II.CIRCUIT DESCRIPTION

A.6T SRAM READ FAILURE TEST

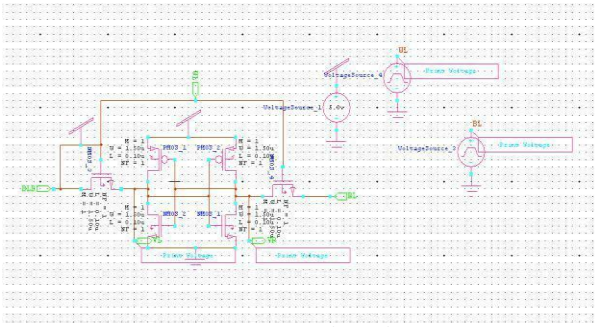

FIG:2 Schematic diagram of read failure test.

The schematic diagram shows the 6T SRAM memory cell consists of two cross coupled CMOS invertors connected back to back with two

pass transistors connected to a complimentary bit lines BL ,word line WL and BLB . Here we are using the 6 transistors as four NMOS transistors and two PMOS transistors,then 2 NMOS transistors are act pass transistors. If we give the input V_L as 1 and read the output in V_R as 0.The cell ratio for this circuit is 1.5.

B.6T SRAM WRITE FAILURE TEST

The schematic diagram shows the 6T SRAM during write failure test . If we give the write V_L as 1 and get the output in V_R as 0.The cell ratio for this circuit is 1.5.Here two cross coupled CMOS invertors connected back to back with two pass transistors connected to a complimentary bit lines BL ,word line WL and BLB .Then the pull –up ratio for the SRAM during write failure test is 0.8.

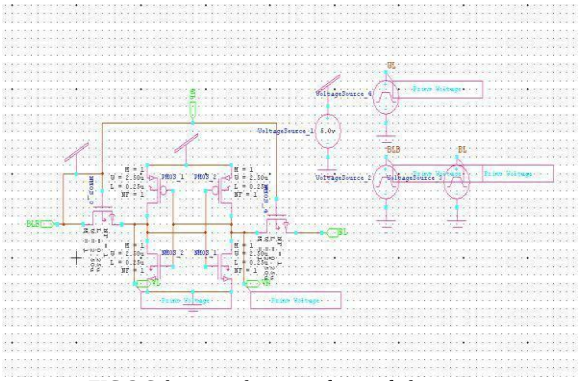

FIG:3 Schematic diagram of write failure test.

C.6T SRAM DYNAMIC SRRV MEASUREMENT

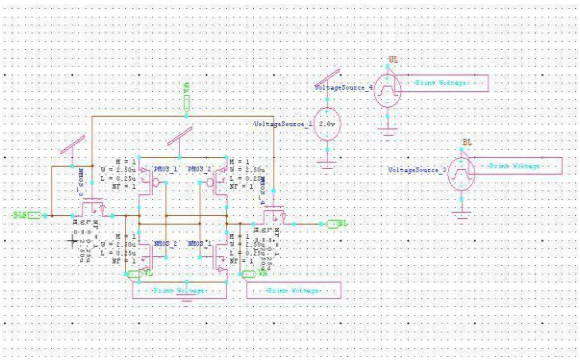

FIG:4 Schematic diagram of Dynamic SRRV measurement.

The schematic diagram shows the 6T SRAM dynamic SRRV measurement ,here the word –line is driven by a pulse with duration T_W. The cell supply voltage is gradually scaled down per every access.

One of the bit lines storing "0" is tied to *V*DD, and other bit line storing "1" is swept from high to low. RRV is a measurable quantity for an cell by changing the cell supply or word-line driver supply . The approach measures the lowest cell supply voltage before disturbing the stored bit. From Fig., all bit lines are tied to the supply line with the access transistors on, and the cell supply voltage (*V*CELL*)* is swept from high to low. At the beginning of the test, "0" is written into the target cell and hence *V*R stores a low state. Next, *V*CELL scales down by a predefined step , and then the bit-line current (*I*BL*)* is measured. If the data are not changed, the nonzero amount of current can be measured. At this cell supply level, *I*BL suddenly drops to zero. The amount of the supply voltage scaling is recorded as the SRRV. Depending on the direction of the flipping, the SRRV can be divided into SRRVL and SRRVR. The read stability of the SRAM cell is critically affected by the cell supply level. Other stability enhancing techniques such as reverse body bias or adjustment of the word-line driver supply level have relatively small impact on the read stability. Therefore, a proper cell supply level should be chosen on the basis of the SRRV distribution to minimize the read disturbance .

D.POWER ANALYSIS OF 6T SRAM

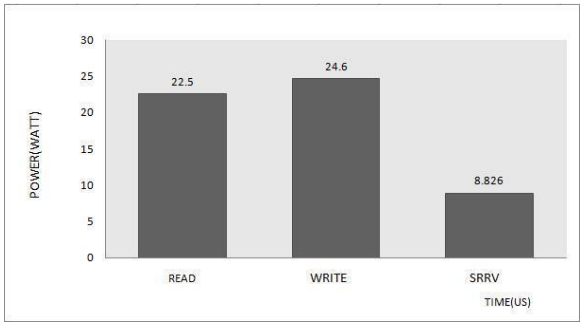

FIG:5 Power consumption in 6T SRAM

By comparing the read failure test , write failure test and dynamic SRRV measurement, we are obtaining the low power in dynamic SRRV measurement. The comparison chart for these three techniques are shown below.

D.PROPOSED 4T SRAM CIRCUIT

A 4T SRAM contains 4 transistors, a pair of pmos and nmos make twisted inverter and two nmos as access transistor. There is feedback between two nodes, WL line is used for transferring new data into the cell. Reading and writing operation of 4T SRAM cell is similar to 6T SRAM cell except data

has been written[7]. During write operation BL and BLB line is prechaged to supply voltage.

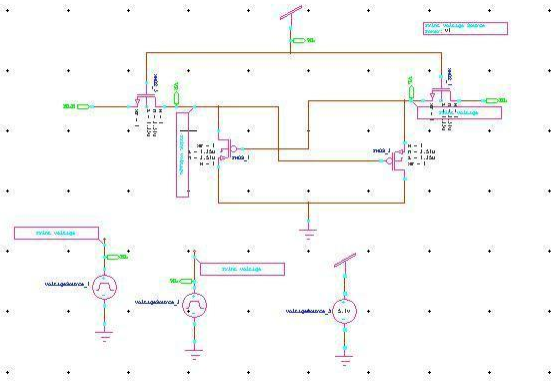

FIG:6 Schematic diagram of proposed 4T SRAM

III. CONCLUSION

The stability of a 6T-SRAM cell was estimated using a nonlinear regression from cell currents under variant supply levels. To apply this technique, the modified measurable failure conditions (SRRV and BWTV) were considered. The static measurements shows the better read stability and the write-ability estimation. This technique can be implemented in a modern CMOS SRAM chip with small extra cost for the area of the measurement circuitry without the change of the SRAM array structure. SRAM cell consume approximately 16.72% more silicon area as compared to the existing basic SRAM cell .But it provides better voltage and comparition in SRRV measurement compared with the read and write circuits in 250nm CMOS technology.

Fewer transistors play an important role in designing high density SRAM where large. 6T SRAM cell contains two nodes,data and their compliment have been holding on each node. While in 4T,it also having two nodes for reading and writing performance. Area of cell reduced by more than 65%. Read and write delay into 4T cell is comparable to other configuration. Power consumption in 4T cell is higher but it can be reduce if after read 0 there is an extra cycle either read1 or write.

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