International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:2682
Vol.4, No.6, June 2015 DOI:10.15693/ijaist/2015.v4i6.9-15

Data Encoding Techniques For Low Power Address And Data Buses

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***Abstract* — As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs).In this project we present a set of data encoding schemes aimed at reducing the power dissipated by the links of an NoC. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture).The proposed encoder will be coded in HDL and simulated using Xilinx 12.1.**

Index Terms - Coupling Switching Activity, Data Encoding, Network Interface (NI), Network-on-Chip (NoC), System on-Chip (SoC).

I. INTRODUCTION

Shifting from a silicon technology node to the next one results in faster and more power efficient gates but slower and more power hungry wires [1]. In fact, more than 50% of the total dynamic power is dissipated in interconnects in current processors, and this is expected to rise to 65%–80% over the next several years [2]. Global interconnect length does not scale with smaller transistors and local wires. Chip size remains relatively constant because the chip function continues to increase and RC delay increases exponentially. At 32/28 nm, for instance, the RC delay in a 1-mm global wire at the minimum pitch is 25× higher than the intrinsic delay of a two-input NAND fanout of 5 [1].If the raw computation horsepower seems to be unlimited, thanks to the ability of instancing more and more cores in a single silicon die, scalability issues, due to the need of making efficient and reliable communication between the increasing number of cores, become the real problem [3]. The network on-chip (NoC) design paradigm [4] is recognized as the most viable way to tackle with scalability and variability issues that characterize the ultra deep submicron meter era. Now-a-days, the on-chip communication issues are as relevant as, and in some cases more relevant than, the computation related issues [4]. In fact, the communication subsystem increasingly impacts the traditional design objectives, including cost (i.e., silicon area), performance, power dissipation, energy consumption [7], reliability etc. As technology shrinks, an ever more significant fraction of the total power budget of a complex many-core system on-chip (SoC) is due to the communication subsystem.

II. EXISTING WORK

The existing data encoding techniques reduces power consumption at a smaller level and encoding architectures are very complicated to design. As technology shrinks an ever more significant fraction of the overall system power/energy budget is due to the on-chip interconnect. It is therefore essential the definition of new methodologies and techniques aimed at optimizing the on-chip communication system not only in terms of performance but also in terms of power. The encoding scheme exploits the wormhole switching techniques and works on an end-to-end basis. That is, flits are encoded by the network interface (NI) before they are injected in the network and are decoded by the destination NI [5]. This makes the scheme transparent to the underlying network since the encoder and decoder logic is integrated in the NI and no modification of the routers architecture is required. We assess the proposed encoding scheme on a set of representative data streams (both synthetic and extracted from real applications) showing that it is possible to reduce the power contribution of both the self-switching activity and the coupling switching activity [15], [16] – [20] in inter-routers links. As results, we obtain a reduction in total power dissipation and energy consumption up to 37% and 18%, respectively, without any significant degradation in terms of both performance and silicon area.

III. PROPOSED MODEL

The previous Data Encoding Technique perform with more number of clocks and area stages. The main objective of our work is to reduce time, switching and coupling activity of network. The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity [18] – [20] and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling

switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique [4]. Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision taken at the NI may provide the same power saving for all the links. For the proposed scheme, an encoder and a decoder block are added to the NI. Except for the header flit, the encoder encodes the outgoing flits of the packet such that the power dissipated by the inter-router point-to-point link is minimized.

A. ENCODING SCHEMES

In this section, we present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. Let us first describe the power model that contains different components of power dissipation of a link. The dynamic power dissipated by the interconnects and drivers is

$$P = [T_0\rightarrow 1\ (Cs + Cl\ ) + TcCc]\ V^2ddFck \quad (1)$$

Where $T_0\rightarrow 1$ is the number of $0 \rightarrow 1$ transitions in the bus in two consecutive transmissions, Tc is the number of correlated switching between physically adjacent lines, Cs is the line to substrate capacitance, Cl is the load capacitance, Cc is the coupling capacitance, Vdd is the supply voltage, and Fck is the clock frequency. One can classify four types of coupling transitions as described in. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high while the other makes transition from high to low. A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type, and hence, the coupling transition activity, Tc, is a weighted sum of different types of coupling transition contributions. Therefore

$$Tc = K_1T_1 + K_2T_2 + K_3T_3 + K_4T_4 \quad (2)$$

Where T_i is the average number of Type i transition and $_{Ki}$ is its corresponding weight. According to [26], we use $K_1 = 1$, $K_2 = 2$, and $K_3 = K_4 = 0$. The occurrence probability of Types I and II for a random set of data is 1/2 and 1/8, respectively. This leads to a higher value for K_1T_1 compared with K_2T_2suggesting that minimizing the number of Type I transition may lead to a considerable power reduction. Using (2), one may express (1) as

$$P = [T0\rightarrow 1\ (Cs + C_l\ ) + (T_1 + 2T_2)\ Cc]\ V\ ^2ddFck \quad (3)$$

According to [3], C_l can be neglected

$$P\ \alpha\ T_0\rightarrow 1Cs + (T_1 + 2T_2)\ Cc \quad (4)$$

B. SCHEME I

In scheme I, we focus on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction.

1) POWER MODEL

If the flit is odd inverted before being transmitted, the dynamic power on the link is

$$P'\ \alpha\ T'_{0\rightarrow 1} + (K_1T'_1 + K_2T'_2 + K_3T'_3 + K_4T'_4)Cc \quad (5)$$

Where $T_{0\_\rightarrow 1}$, T_1', T_2', T_3', and T_4', are the self-transition activity, and the coupling transition activity of Types I, II, III, and IV, respectively.

TABLE I – Effect of odd inversion on change of transition types

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10 10, 01			01, 10 11, 00		
$t-1$	Type III			Type I		
t	00, 11 11, 00			00, 11 10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10 00, 11, 01, 10			00, 11, 01, 10 01, 10, 00, 11		

Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted as is and when its bits are odd inverted. Data are organized as follows. The first bit is the value of the generic ith line of the link, whereas the second bit represents the value of its (i + 1)th line. For each partition, the first (second) line represents the values at time t − 1 (t). As Table I shows, if the flit is odd inverted, Types II, III, and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions indicated as T1*, T1**, and T1*** in the table convert to Types II, III, and IV transitions, respectively.

Also, we have $T'_{0\rightarrow 1} = T_{0\rightarrow 0}$(odd) + $T_{0\rightarrow 1}$(even) where odd/even refers to odd/even lines. Therefore, (5) can be expressed as

$$P \alpha (T_{0\to0}(odd) + T_{0\to1}(even))\, Cs + [\, K_1(T_2+T_3+T_4) + K_2T_1{***} + K_3T_1{*} + K_4T_1{**}]\, Cc \quad (6)$$

Thus, if P > P_, it is convenient to odd invert the flit before transmission to reduce the link power dissipation. Using (4) and (6) and noting that Cc/Cs = 4 , we obtain the following odd invert condition

$$¼\ T_{0\to1} + T_1 + 2T_2 > 1/4(T_{0\to0}(odd) + T_{0\to1}(even)) + T_2 + T_3 + T_4 + 2T_1{***}.$$

Also, since $T_{0\to1} = T_{0\to1}(odd) + T_{0\to1}(even)$,one may write

$$¼\ T_{0\to1}(odd) + T_1 + 2T_2 > 1/4\ T_{0\to0}(odd) + T_2 + T_3 + T_4 + 2T_1{***} \quad (7)$$

It is the exact condition to be used to decide whether the odd invert has to be performed. Since the terms $T_{0\to1}(odd)$ and $T_{0\to0}(odd)$ are weighted with a factor of 1/4, for link widths greater than 16 bits, the misprediction of the invert condition will not exceed 1.2% on average. Thus, we can approximate the exact condition as

$$T_1 + 2T_2 > T_2 + T_3 + T_4 + 2T_1{***} \quad (8)$$

Of course, the use of the approximated odd invert condition reduces the effectiveness of the encoding scheme due to the error induced by the approximation but it simplifies the hardware implementation of encoder. Now, defining

$$T_x = T_3 + T_4 + T_1{***}$$
and
$$T_y = T_2 + T_1 – T_1{***} \quad (9)$$

one can rewrite (8) as

$$T_y > T_x \quad (10)$$

Assuming the link width of w bits, the total transition between adjacent lines is w − 1, and hence

$$T_y + T_x = w - 1 \quad (11)$$

Thus, we can write (10) as

$$T_y > (w - 1)/2 \quad (12)$$

This presents the condition used to determine whether the odd inversion has to be performed or not.

2) ENCODING ARCHITECTURE

The proposed encoding architecture, which is based on the odd invert condition defined by, is shown in Fig. 1. We consider a link width of w bits. If no encoding is used, the body flits are grouped in w bits by the NI and are transmitted via the link. In our approach, one bit of the link is used for the inversion bit, which indicates if the flit traversing the link has been inverted or not. More specifically, the NI packs the body flits in w − 1 bits [Fig. 1(a)]. The encoding logic E, which is integrated into the NI, is responsible for deciding if the inversion should take place and performing the inversion if needed. The generic block diagram shown in Fig. 1(a) is the same for all three encoding schemes proposed in this paper and only the block E is different for the schemes. To make the decision, the previously encoded flit is compared with the current flit being transmitted. This latter, whose w bits are the concatenation of w−1 payload bits and a "0" bit, represents the first input of the encoder, while the previous encoded flit represents the second input of the encoder [Fig. 1(b)]. The w − 1 bits of the incoming (previous encoded) body flit are indicated by X_i (Y_i), i = 0, 1, . . . , w − 2. The w^{th} bit of the previously encoded body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0).

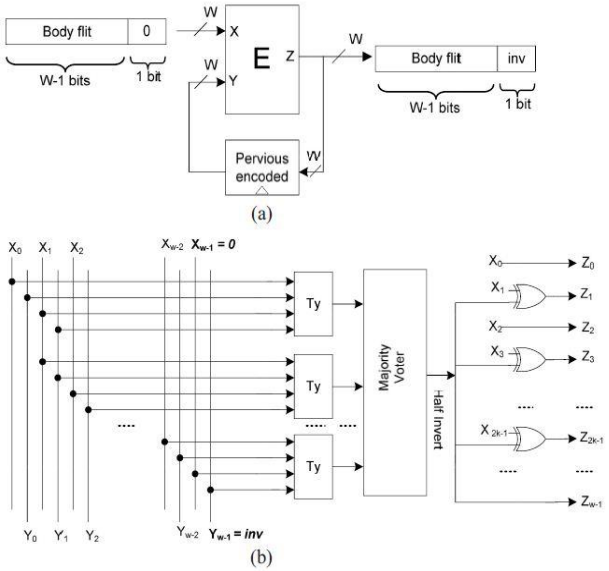

Fig. 1 Encoder architecture scheme I. (a) Circuit diagram. (b) Internal view of the encoder block (E).

In the encoding logic, each Ty block takes the two adjacent bits of the input flits (e.g., $X_1X_2Y_1Y_2$, $X_2X_3Y_2Y_3$, $X_3X_4Y_3Y_4$, etc.) and sets its output to "1" if any of the transition types of T_y is detected. This means that the odd inverting for this pair of bits leads to the reduction of the link power dissipation (Table I). The T_y block may be implemented using a simple circuit. The second stage of the encoder, which is a majority voter block, determines if the condition given in is satisfied (a higher number of 1s in the input of the block compared to 0s). If this condition is satisfied, in the last stage, the inversion is performed on odd bits. The decoder circuit simply inverts the received flit when the inversion bit is high.

C. SCHEME II

In the proposed encoding scheme II, we make use of both odd (as discussed previously) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction.

1) POWER MODEL

Let us indicate with P', P'', and P''' the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when P' < P'' and P'< P. The power P'' is given by [23]

$$P'' \alpha T_1 + 2T_4^{**} \quad (13)$$

Neglecting the self-switching activity, we obtain the condition P' < P'' as [see (7) and (13)]

$$T_2 + T_3 + T_4 + 2T_1^{***} < T_1 + 2T_4^{**} \quad (14)$$

Therefore, using (9) and (11), we can write

$$2 (T_2 – T_4^{**}) < 2T_y – w + 1 \quad (15)$$

Based on (12) and (15), the odd inversion condition is obtained as

$$2 (T_2 – T_4^{**}) < 2T_y – w + 1\ T_y > (w – 1)/2 \quad (16)$$

Similarly, the condition for the full inversion is obtained from P'' < P and P''< P'. The inequality P''< P is satisfied

$$T_2 > T_4^{**} \quad (17)$$

Therefore, using (15) and (17), the full inversion condition is obtained as

$$2 (T_2 – T_4^{**}) > 2T_y – w + 1\ T_2 > T_4^{**} \quad (18)$$

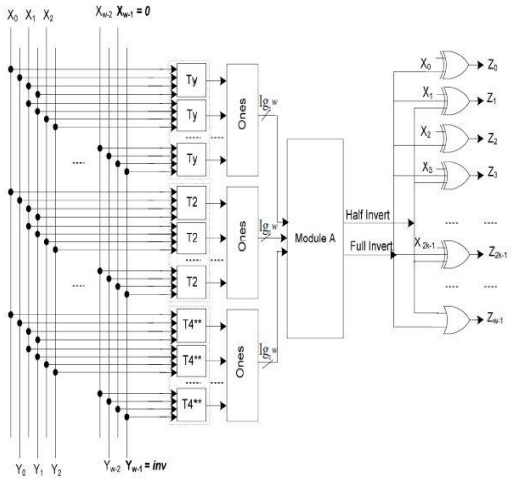

Fig 2 Encoding Architecture scheme II

When none of (16) or (18) is satisfied, no inversion will be performed.

2) ENCODING ARCHITECTURE

The operating principles of this encoder are similar to those of the encoder implementing Scheme I. The proposed encoding architecture, which is based on the odd invert condition of (16) and the full invert condition of (18), is shown in Fig. 2. Here again, the w^{th} bit of the previously and the full invert condition of (18) is shown in Fig.3.2. Here again, the w^{th} bit of the previously encoded body flit is indicated with inv which defines if it was odd or full inverted (inv = 1) or left as it was (inv = 0). In this encoder, in addition to the Ty block in the Scheme I encoder, we have the T_2 and T_4** blocks which determine if the inversion based on the transition types T_2 and T_4** should be taken place for the link power reduction. The second stage is formed by a set of 1s blocks which count the number of 1s in their inputs. The output of these blocks has the width of log2 w. The output of the top 1s block determines the number of transitions that odd inverting of pair bits leads to the link power reduction. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power.

Based on the number of 1s for each transition type, Module A decides if an odd invert or full invert action should be performed for the power reduction. For this module, if (16) or (18) is satisfied, the corresponding output signal will become "1." In case no invert action should be taken place, none of the output is set to "1." Module A can be implemented using full-adder and comparator blocks. The middle 1s block identifies the number of transitions whose full inverting of pair bits leads to the link power reduction. Finally, the bottom 1s block specifies the number of transitions whose full inverting of pair bits leads to the increased link power. The scheme compares the current data with the previous one to decide whether the odd, full, or no inversion of the current data can give rise to the link power reduction. The circuit diagram of the decoder is shown in Fig. 3.3 The w bits of the incoming (previous) body flit are indicated by Z_i (R_i), i = 0, 1, . . . ,w − 1. The w^{th} bit of the body flit is indicated by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). For the decoder, we only need to have the T_y block to determine which action has been taken place in the encoder. A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode.

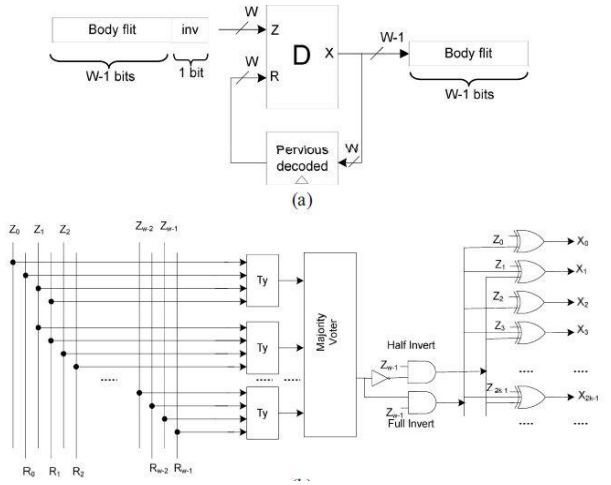

Fig. 3 Decoder architecture scheme (a) Circuit diagram. (b) Internal view of the decoder block (D).

Based on the outputs of these blocks, the majority voter block checks the validity of the inequality given by. If the output is "0" ("1") and the inv = 1,it means that half (full) inversion of the bits has been performed. Using this output and the logical gates, the inversion action is determined. If two inversion bits were used, the overhead of the decoder hardware could be substantially reduced.

3) CLOCK GATING

Gated clock is a well known method for reducing power consumption in synchronous digital circuits. By this method the clock signal is not applied to the flip flop when the circuit is in idle condition. This reduces the power consumption. Fig. 4 shows the diagram with clock gating. In a digital circuit the power consumption can be accounted due to the following factors:

1) Power consumed by combinatorial logic whose values are changing on each clock edge
2) Power consumed by flip-flops.

Of the above two, the second one contributes to most of the power usage. A flip flop consumes power whenever the applied clock signal changes, due to the charging and discharging of the capacitor. If the frequency of the clock is high then the power consumed is also high. Gated clock is a method to reduce this frequency. In today's semiconductor designs, lower power consumption is mandatory for mobile and handheld applications for longer battery life and even networking or storage devices for low carbon footprint requirements. It is good design idea to turn off the clock when it is not needed. Automatic clock gating is supported by modern EDA tools. They identify the circuits where clock gating can be inserted.

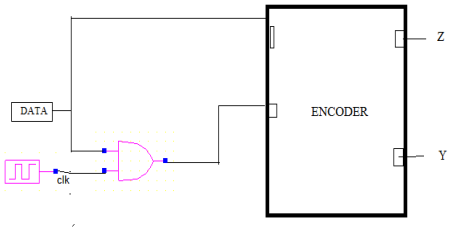

Fig. 4 Proposed architecture

There are two types of clock gating styles available. They are:

1) Latch-based clock gating
2) Latch-free clock gating

The latch-free clock gating style uses a simple AND or OR gate (depending on the edge on which flip-flops are triggered). Here if enable signal goes inactive in between the clock pulse or if it multiple times then gated clock output either can terminate prematurely or generate multiple clock pulses. The latch-based clock gating style adds a level-sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock. Clock power consumes 60-70 percent of total chip power and is expected to significantly increase in the next generation of designs at 45nm and below. This is due to the fact that power is directly proportional to voltage and the frequency of the clock as shown in the following equation:

Power = Capacitance * (Voltage) 2 * (Frequency)

Hence, reducing clock power is very important. Clock gating is a key power reduction technique used by many designers and is typically implemented by gate-level power synthesis tools. Advantage of this method is that clock gating does not require modifications to RTL description.

IV. SIMULATION RESULTS

The proposed Data Encoding Technique is implemented by using Spartan-3 device xc3s400 - 4tq144. The comparison between those two systems has been done based on the parameters like number of slices, number of IO's, number of bonded IOBs, number of slice flip-flops and time consumption. System level testing may be performed with the ModelSim logic simulator and such test programs must also be written in HDL languages. Test bench programs may include simulated input signal waveforms or monitors which observe and verify the outputs of the device under test. The simulation result for data encoding is shown in Fig. 5. The result for gate encoding without and with clock gating are shown in Fig. 6 and Fig. 7.

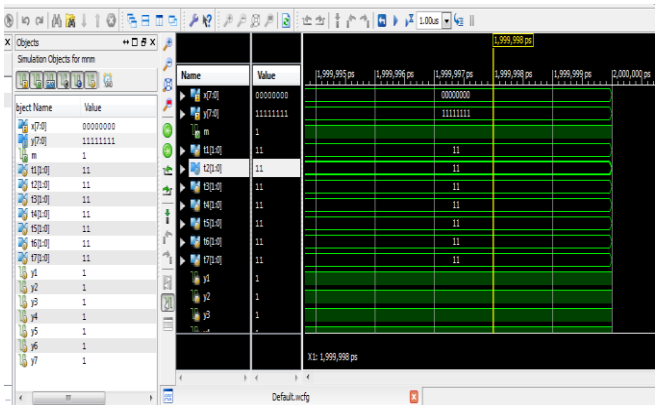

Fig. 5 Simulation Result for data encoding

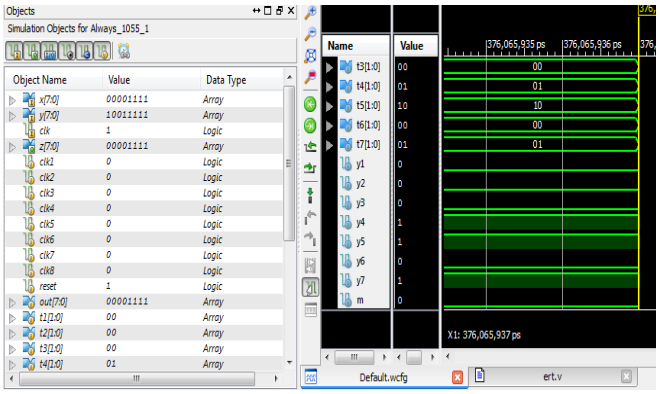

Fig. 6 Simulation Result for data encoding without clockgating

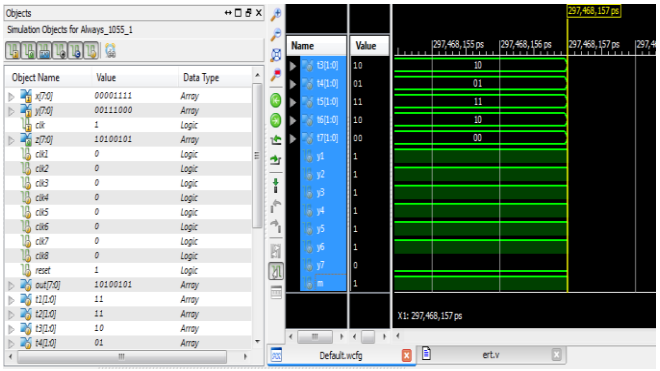

Fig. 7 Simulation Result for data encoding with clockgating

V. PERFORMANCE ANALYSIS

The diagram given below is shown that there is a considerable reduction in time and power based on the implementation results which have been done by using Spartan-3 processor. The proposed system significantly reduces power consumption when compared to the existing system.

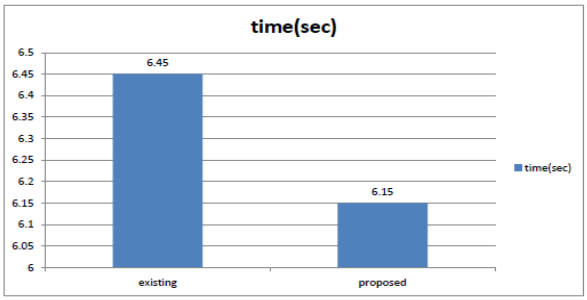

Fig. 8 Power Consumption

VI. CONCLUSION AND FUTURE WORK

We have proposed a set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the rationale behind the proposed schemes is to minimize not only the switching activity, but also (and in particular) the coupling switching activity which is mainly responsible for link power dissipation in the deep sub micro meter technology region. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. The encoders implementing the proposed schemes have been assessed in terms of power dissipation. In the future, we would extend this work to more advanced buses/communication devices in order to reduce power consumption and to implement in FPGA kit.

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