International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:268
Vol.2, No.3, March 2013 DOI:10.15693/ijaist/2013.v2i3.42-47

# Performance Analysis Of Real Time Architecture Using Pes Technique

**M.DURGADEVI[1]B.MUTHUPANDIAN[2]Dr.R.GANESAN[3]**
[1] PG Scholar, SIT Engg. College, Kariyapatti-626 115
[2] Asst.Prof /ECE, SIT Engg. College, Kariyapatti-626 115
[3] Prof/HOD, SIT Engg College, Kariyapatti-626 115
Anna University Chennai, India

***Abstract*: Scan based delay testing is currently mostly implemented using launch-on-capture (LOC) delay tests. Launch-on-shift (LOS) tests are more effective, improving fault coverage with significantly fewer test vectors, but require a fast scan enable signal. To reduce the volume of test data ,a partial enhanced scheme ,which replaces only 1% chosen regular scan flip-flops in the scan chain with the enhanced scan chain, can also achieve most of the fault coverage while minimizing area overhead. A flip-flop selection strategy presented for partial enhanced scan designs shows a very favourable trade-off between fault coverage and test data volume.**

***Index Terms:* Test Data Volume reduction, Fault coverage, Launch On Capture(LOC), Launch On Shift(LOS).**

## I.INTRODUCTION

Advances in Fabrication technology has enabled VLSI engineers to go to sub micron technology allowing them to pack millions of transistors in a single chip. As the number of elements inside a chip started increasing exponentially there was also a sharp rise in the post manufacturing defects/faults in the chip. As the elements and their interconnects started becoming smaller and smaller, the probability of interconnects getting short to ground or power line or getting short with each other also went high. Not only interconnects, the faults in components like shorting of drain and source of MOS transistors also went up. So post manufacture testing of VLSI became an important issue. Generally testing VLSI circuits require a number of discrete test equipments. Traditionally the practice was to control the equipments manually. The disadvantages were slow speed of testing, Manufacturing defects that cause timing errors have become a serious concern. Delay fault, which is typically caused by these physical defects can induce violation of the circuit's timing requirement.[21], [13].In order to achieve a satisfactory defect level it is thus significant to conduct effective delay testing.

Path delay and transition delay fault models [3], [4] are two commonly adopted models to detect physical delay defects. The transition delay fault (TDF) model is the most widely used model to test delay faults compared to path delay fault. There are many fault models, such as Gate delay model, Transistor delay model, Segment delay model and In line resistive delay model. In the lumped transition (gate) delay fault model, a delay defect is assumed to make the fault site charge or discharge more slowly than normal. These are defined as slow-to-rise and slow-to-fall transition delay faults. In the path delay fault model, the delay defect in the circuit is assumed to cause the cumulative delay of a combinational path to exceed some specified duration, which normally is one nominal clock period [2].

For transition delay fault model, one advantage is that the total fault number is measurable and is twice total faulty sites. Besides, tests are easy to generate and a stuck at fault test generator can be easily modified to generate transition fault tests. Compared with transition delay fault testing, path delay fault testing can in theory detect more delay faults, because in the transition delay testing the delay on the faulty gate may be compensated for by the delay on other faster gates in the path which is used to propagate transition. However, the number of possible paths in the circuit grows up exponentially with the increase of the number of gates. Hence, it is impractical to detect all path delays in a circuit, especially for large SOCs.

## II. SCAN BASED DELAY TESTING

scan based delay testing uses two-vector test patterns <V1, V2>. The first vector V1 is scanned into the flip-flops and used to initialize the logic values at the input of the combinational logic block, which is the circuit under test (CUT). A second vector V2 is then used to launch transitions at these inputs and propagate these transitions to the outputs of the CUT, which are then captured back in the scan chains. Generally speaking, compared with LOC delay tests, LOS delay tests display better TDF (Transition Delay Fault) [9] coverage [7, 10, 11] and typically reach this coverage with fewer test patterns. , in practice only LOC can actually be applied to most circuits because LOS requires a high speed global scan enable signal. In large SOCs, it is difficult to design scan enable signals with sufficient drivability to drive all scan flip-flops of the circuit within the timing constraints. Scan enable signals must also synchronize at the input port of each scan flip-flop with minimal timing skew. This requires routing the scan enable signals as additional clock signals, which is expensive to implement and is not currently supported in most scan-based designs. Consequently, there is considerable interest in developing low cost designs to support LOS scan based delay tests. Such a capability can potentially also allow combining LOS and LOC tests for even higher TDF coverage.

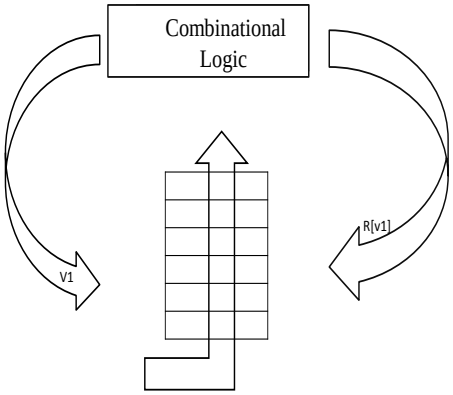



FIG. 1 SCAN BASED DELAY TESTING

The schematic waveforms in Figure-2 illustrate the timing associated with of executing LOS and LOC delay tests. The scan enable must be held high for the duration when the first test vector V1 is scanned into the scan chain. This is typically done using a slow scan clock. The waveforms in Figure 1-5 assume positive edge triggered flip-flops, and show the last scan clock pulse, which makes the V1 vector available at the CUT inputs following the positive clock edge. For the LOC test, the scan enable is then made low and enough time is allowed to elapse to allow the change in this slow global signal to take effect throughout the chip before two timed high speed clock pulses are applied to launch V2 and capture the CUT's response to this input change. Because scan enable is low (functional mode) at the first high speed launch clock edge, the V2 vector captured in the flip-flops and applied to the CUT is the circuit's response to V1, corresponding to a launch-on-capture (LOC) test. The time between the two fast clock edges must match the operational clock rate to ensure that the delay test checks that the CUT outputs reach the correct logic values within the functional clock period. These captured test results are again scanned out at a slow scan rate.

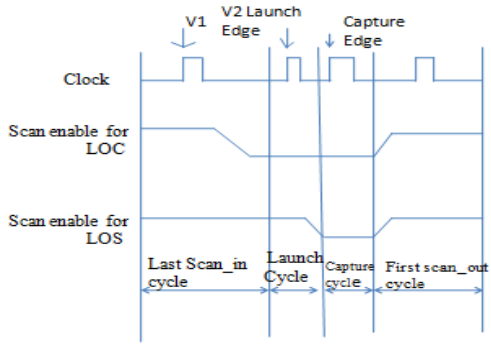



FIG.2 WAVEFORMS FOR LOS AND LOC DELAY TEST

In the LOS delay test, the second delay test vector V2 is obtained by shifting one bit from V1. In this case, the scan enable signal must remain high (in the scan shift mode) for one more active clock edge after V1 is shifted in, until V2 is launched at the flip-flop outputs on the positive edge of the first fast clock. Scan enable must then be quickly switched low (to the functional mode) so that the CUT's response to V2 can be captured back in the flip-flop. Because the scan enable must switch within the timed fast clock interval in this case, it is important for this global signal to reach all the flip-flops in the design within tight timing constraints. This requires that the scan enable signal for LOS testing be routed as a timing critical signal, just like a clock signal. However, this is very expensive, and not supported in most scan designs. Therefore, scan based delay tests today mostly employ the LOC mode.

### i. SCAN ELEMENTS

There are two kinds of commonly used scan elements for scan based structural delay testing. One is MUX (multiplexer) based scan flip-flop (SFF); the other is Level Sensitive Scan Design (LSSD) .

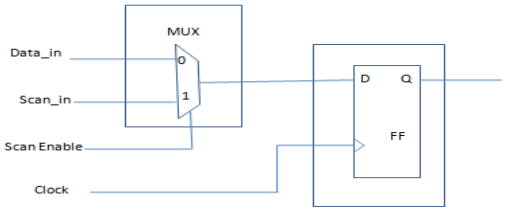



FIG.3 REGULAR SCAN FLIP-FLOP

To build a scan flip-flop, a multiplexer (MUX) is added on the data path of a regular D flip-flop, as shown in Figure 1-1. When Scan Enable signal is set to logic '0', DFF accepts data from the input "Data_in". When Scan Enable signal is set to logic '1', DFF accepts data from the input "Scan_in". For scan based structural delay testing, a number of SFFs are serialized into a scan chain, as shown in Figure 1-2. When Scan_enable (in Figure 1-2) is set to '1', each SFF captures and stores data from the primary input ("Scan_in") or the output ("Q") of its preceding SFF. Then, data can be scanned into or out of SFFs through the scan chain. Therefore, when Scan_enable is set to '1', SFFs operate under "shift mode" or "scan mode". When Scan_enable is set to '0', each SFF captures and stores data from outputs of Combinational Logic. After stimuli employed on the Combinational Logic, the responses of Combinational Logic can be captured in the scan chain. Therefore, when Scan_enable is set to '0', SFFs operate under "function mode" or "capture mode".

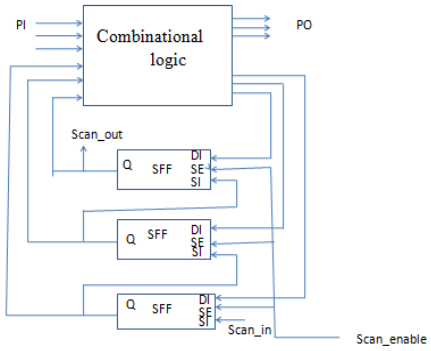



FIG.4 COMBINATIONAL LOGIC FOR REGULAR SCAN FLIP-FLOP

## III PARTIAL ENHANCED SCAN FLIP-FLOP

Although enhanced scan techniques have been around for a long time, they have rarely been used in practice so far because of the prohibitive area overhead. However, recent interest in achieving high delay test coverage from scan based tests, beyond what is possible from traditional LOC tests, to detect small delay defects and perhaps also avoid the need for at-speed functional tests, has revived interest in such schemes . In this section we investigate a strategy for realizing most of the TDF coverage gains achievable from enhanced scan at a fraction of the cost by implementing partial enhanced scan designs.. One of the specific problems addressed in the earlier work was: starting from a (full) enhanced scan chain, what flip-flops can be replaced with regular flip-flops without reducing the achievable path delay coverage. We want to identify a relatively small number (1%) of flip-flops in the scan chain such that when these are replaced by enhanced scan flip-flops, the majority (60-90%) of the additional coverage achievable by going to an all-enhanced scan flip-flop design is already realized. This is possible if we can develop a flip-flop selection scheme that gives a coverage versus fraction of enhanced scan flip-flops trade-off as shown in Figure-5. Such a methodology can then offer attractive low cost options for partial enhanced scan designs as shown in Figure-7.

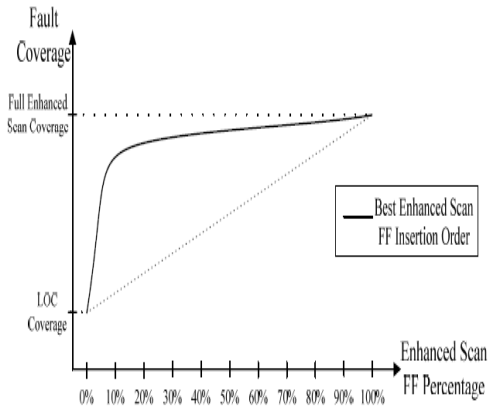



FIG. 5 PERCENTAGE AND FAULT COVERAGE OF PARTIAL ENHANCED SCAN

Unfortunately, in all of the enhanced scan designs control signals capable of switching at operational clock speeds are needed to ensure proper test timing. For example, it is well understood that the scan enable signal must be capable of at-speed switching to support the LOS tests needed by the design in Figure -7.Implementing high speed control signals is very expensive, loosely comparable in cost to an extra clock signal. Such signals must be avoided in any low cost design which attempts cost savings from a partial enhanced scan methodology. If the enhanced scan flip-flop in Figure 6 is used in a partial enhanced scan design, along with a slow scan enable, the enhanced scan flip-flops can launch arbitrary two bit patterns at their outputs during the V1 to V2 transition, while the regular scan flip-flops must operate in the LOC mode (LOS is not supported by a slow scan enable). This implies that the lower bound TDF coverage of such a partial enhanced scan design is just the LOC coverage (with 0% enhanced scan flip-flops in the scan chain). Our goal is to select an increasing number of flip-flops in the scan chain to convert to enhanced scan flip-flops in such a manner that for a given number of enhanced flip-flops in the partial scan chain, the TDF coverage is the maximum, as shown in Figure 6.

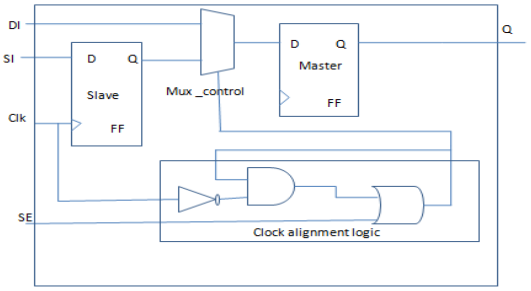



FIG.6 ENHANCED SCAN CELL

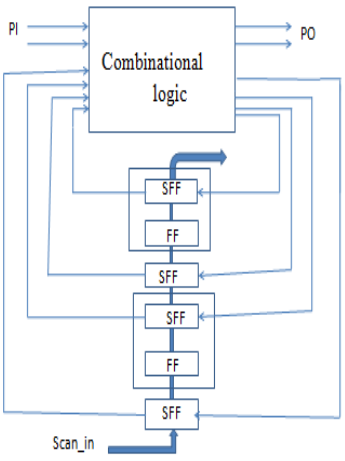



FIG.7 COMBINATIONAL LOGIC FOR PARTIAL ENHANCED SCAN

## IV EXPERIMENTAL RESULTS

The transition delay test generations are conducted for both the normal scan circuits and partial enhanced scan circuits, respectively. The results of the experiments for the benchmark circuits in Table II. The total number of scan cells in each benchmark is shown in column 2. The achieved TDF coverage and the corresponding number of test patterns of the CUT using the pure LOC delay fault testing approach are given in columns 3 and 4, respectively. In order to reduce the hardware overhead, the replaced numbers of enhanced scan cells are limited to only 1% and 2% of the total number of scan cells in each benchmark circuit. The columns under "#rep" represent the number of regular scan cells which are replaced with enhanced scan cells. In order to study the effectiveness of the test pattern count reduction with the proposed approach, we conduct the experiment in which the target TDF coverage of the proposed approach is limited to the fault coverage obtained by the pure LOC approach. Clearly, the effectiveness of test pattern count reduction with the proposed approach is significant for all sample benchmark circuits. For example, for S15850 by replacing 1% of regular scan cells with enhanced scan cells, the number of generated test patterns is only 31% of that for pure LOC approach to achieve equal TDF coverage. Note that when 2% of scan cells are replaced by enhanced scan cells in S15850, the test pattern count can be reduced up to 14%. It should be noted that the maximum achievable TDF coverage can be improved in the proposed approach due to the alleviation of functional dependency to obtain the launch vector. Hence we conduct another experiment in which the target TDF coverage is not limited.

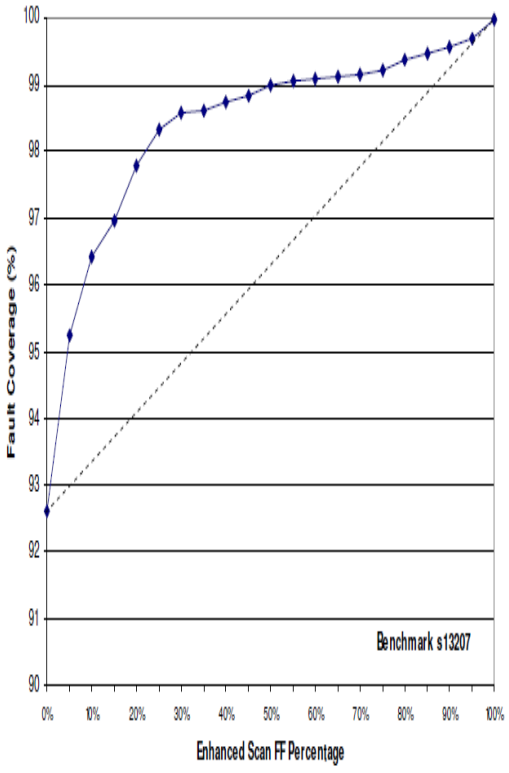
TABLE I
BENCHMARK CIRCUITS

| Circuit name | Number Of FFs | Number Of Inverters | Number Of Gates |
|---|---|---|---|
| S13207 | 638 | 5378 | 7951 |
| S15850 | 534 | 6324 | 9772 |
| S38417 | 1636 | 13470 | 22179 |
| S38584 | 1426 | 7805 | 19253 |

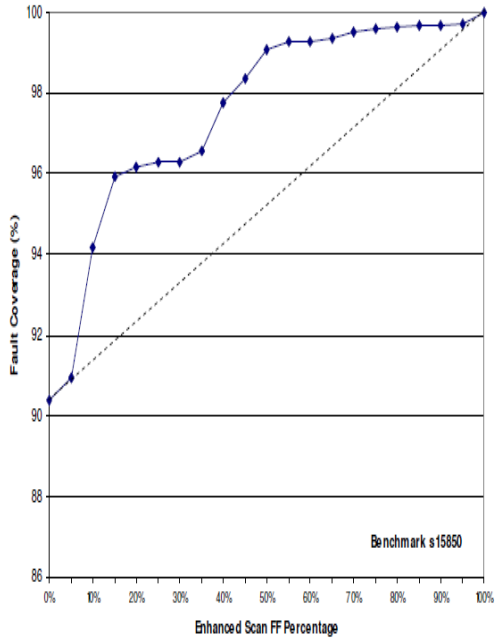
TABLE II
TEST DATA VOLUME COMPARISONS

| Circuit | Test data volume | Ratio of 1% replaced | Ratio of 2% replaced | #rep |
|---|---|---|---|---|
| S13207 | 163096 | 51% | 31% | 7 |
| S15850 | 146124 | 31% | 14% | 6 |
| S38417 | 134732 | 33% | 6% | 16 |
| S38584 | 139340 | 315 | 7% | 15 |

enhanced scan cells, the TDF coverage of S13207 is increased by as much as 8.7%. It should also be noted that the length of the circuit scan chain would become longer when replacing the regular scan cells with enhanced counter parts. Hence, as compared to the pure LOC approach, test data volume for each test pattern would be increased by the amount of replaced enhanced scan cells. Both approaches still have the same TDF coverage. The overall volume of test data is calculated by multiplying the length of each test pattern (including scan chain data and PI data) with the total number of test patterns. The column under "Test data volume (bits)" gives the overall volume of test data generated by the pure LOC approach. The sub-column "1% replaced" and "2% replaced" under the column "Ratio of test data volume (%)" gives the ratio of the overall volume of test data generated by the proposed approach to that of test data generated by the pure LOC approach, in which the replaced numbers of enhanced scan cells are limited to only 1% and 2% of the total number of scan cells for each benchmark circuit, respectively. From the experimental results we can see that a significant reduction (more than 50%) of the test data volume is obtained by the proposed approach. It is worthy of note that the ratio of the test pattern count is very close to that for the test data volume for each benchmark circuit due to the number of replaceable scan cells is limited in the proposed approach.



BENCHMARK S13207




BENCHMARK S15857 BASED ON MONTE-CARLO SIMULATION

Observe that the plots are now monotonically decreasing in slope and achieve the highest TDF coverage with the least number of enhanced scan flip-flops. Furthermore, they suggest that 50% of the coverage gain achievable by full enhanced scan designs over LOC can be obtained from 1%carefully selected enhanced scan flip-flops. Note that we have quite arbitrarily picked 5% set size for the flip-flops to interchange. Using a larger, a granularity set size can reduce the computational effort on the part of the interchange procedure, but leads to somewhat lower TDF coverage for the same fraction of enhanced flip-flops. This is because the "best" flip-flops cannot be individually selected. Using a smaller set size improves the results, but can become computationally prohibitive.

## V CONCLUSION AND FUTURE WORK

The reduction of Test data Volume and high Fault Coverage can be achieved by replacing only 1% of regular scan cells with the enhanced scan cells. Experimental results on larger IWLS 2005 benchmark circuits show that with the same fault coverage, the proposed approach can reduce the test data volume to a half in comparison with the pure LOC approach.

Future work includes the reduction of test data and high fault coverage at the receiver of NOC in order to achieve the low power of the circuit.

## REFERENCES

[1] J. Savir and S. Patil, 1994 "On broad-side delay test", Very Large Scale Integration (VLSI) Systems, vol. 2, pp. 368.

[2] J. Saxena, K. M. Butler, J. Gatt, R. Raghuraman, S. P. Kumar, S. Basu, D. J Campbell and J. Berech, 2002 "Scan- based transition fault testing - implementation and low cost test challenges", in Proc. International Test Conference, pp. 1120-1129.

[3] J. A. Waicukauski, E. Lindbloom, B. Rosen and V. Iyengar, 1987 "Transition fault simulation", IEEE Design & Test of Computers, vol. 4, pp. 32- 38.

[4] Zhen chen , 2009 "The ATPG conflict-Driven scheme for high transition fault coverage and low test cost," VLSI test Symp, pp.146-151.

[5] Z. Zhang, S. M. Reddy, I. Pomeranz, X. Lin and J. Rajski, 2006 "Scan tests with multiple fault activation cycles for delay faults", in Proc. VLSI Test Symposium, pp. 343- 348.

[6] J. Abraham, U. Goel and A. Kumar,2006 "Multi-cycle sensitizable transition delay faults", in Proc. VLSI Test Symposium, pp. 306-311.

[7] N. Ahmed, C. P. Ravikumar, M. Tehranipoor and J. Plusquellic, 2005 "At-speed transition fault testing with low speed scan enable", in Proc. VLSI Test Symposium, pp. 42-4.

[8] N. Ahmed, M. Tehranipoor and C. P. Ravikumar, 2005 "Enhanced launch-off-capture transition fault testing", in Proc. International Test Conference, pp. 246- 255.

[9] N. Devtaprasanna, A. Gunda, P. Krishnamurthy, S. M. Reddy and I. Pomeranz , 2005"Methods for improving transition delay fault coverage using broadside tests", in Proc. International Test Conference, pp. 256-265.

[10] G. Xu and A. D. Singh, 2007 "Achieving high transition delay fault coverage with partial DTSFF scan chains," presented at the Int. Test Conf., Santa Clara, CA, paper 17.

[11] C. J. Lin and S. M. Reddy, , Sep. 1987. "On delay fault testing in logic circuits," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 6, no. 5, pp. 694–703.

[12] J. Savir and S. Patil, 1994 "On broad-side delay test," in Proc. VLSI Test Symp., pp. 284–290.

[13] J. Savir,1992 "Skew-load transition test: Part I, calculus," in Proc. Int. Test Conf., pp. 705–713.

[14] N. Ahmed, M. Tehranipoor, C. P. Ravikumar, and K. M. Butler, May 2007"Local at-speed scan enable generation for transition fault testing using low cost testers," IEEE Trans. Comput.-Aided Design of Integr. Circuits Syst., vol. 26, no. 5, pp. 896–906..

[15] B. Dervisoglu and G. Stong, 1991"Design for testability: Using scan path techniques for path-delay test and measurement," in Proc. Int. Test Conf., pp. 365– 374.

[16] Wei Li, Chaowen Yu, Reddy,S,M,Pomeranz,2003 "A Scan BIST generation method using a Markov source and partial bit- fixing ,"in Design automation conference.,pp. 554- 559.

[17] Amory, A.M.;Briao E;Cota,E;Lubaszewski, 2005"A Scalable test strategy for NOC routers,"in Proc.Int.Test.Conf,pp. 9- 599.
[18] Wohl, P.;Waiukauski,J.A,Colburn,J.E, 2012 "Enhancing testability by structured partial scan," VLSI Test Symp.,pp.152- 157.
[19] Wang and L-C, 2004 "Critical path selection for delay fault testing based upon a statistical timing model,," IEEE Trans on Nov pp.1550-1565.
[20] Songwei pei, Huawei Li, and Xiaowei Li,2012 "Flip-Flop selection for partial enhanced scan to reduce transition test data volume," IEEE Trans on VLSI Systems. pp.2157- 2169.

International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:268
Vol.2, No.3, March 2013
DOI:10.15693/ijaist/2013.v2i3.42-47