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Vlsi Implementation Of Multilayer Adaptive Error Control For Network On Chip Links

M.Jeyabharathi [1] C.Sujatha[2] R.Ganesan[3]
P.G. Student Associate Professor Professor/HOD

Sethu Institute of Technology, Madurai

Abstract-**We propose a framework that allows Multilayer Adaptive error control in a Noc links,to simultaneously improve reliability,performance and energy efficiency.Error control adaptation is extended to a Multilayer approach communicating between datalink,network layer and physical layer to further reduce energy consumption.We employ End-to-End error control in network layer in low noise and enhance the error control capability in high noise regions by turning on hop-to-hop error control in the router and Hybrid error control in the physical layer typically results in huge energy consumption.Another major contribution is a protocol to switch between these layers at runtime. It can detect as well as correct more than two byte of data compared to previous work which can correct two byte of data and it detect error in more than two byte of data.Compared to previous solutions, the propsed method achieves upto 89% energy reduction and improve average latency by upto 68%.We exploited the resources of the three layers,which improves quality of error correction process.** The **proposed design provides the interconnects with powerful error correction capability and thus effectively increases signal integrity and noise immunity. As a result, these interconnects may carry data with lower signal power and/or higher transmission rates.**

***IndexTerms*— Multilayer, Energy efficiency ,error control coding (ECC) , Network-on-chip (NOC), on-chip interconnect, reliability.**

I INTRODUCTION

NETWORKS-on-chip (NoCs) provide an elegant approach to managing interconnect complexity [1]–[5], facilitating integration of heterogeneous intellectual property (IP) cores by separating computation and communication. Because of their modular design and regular topologies, NoCs achieve better scalability and more predictable electrical parameters than traditional buses .the three essential components of NoCs—links, network interfaces (NIs), and routers. Links facilitate communication between routers; Nis transform bit-streams from IP cores into packets for transmission to routers and vice versa; routers extract the destination address from each received packet and pass the packet to its intended destination. NoCs are a good solution to managing integration of a large number of cores in nano scale systems.

In these deeply scaled technologies, reliability[9] is a critical parameter, increased coupling noise affects information transmission on the NoC links[8][9] ; reduced critical charge accompanying technology scaling makes registers and logic circuits more susceptible to noise and process and environmental variations exacerbate delay uncertainties . One method of improving reliability is the use of error control. Incorporating error control in NoCs leads to performance degradation, as well as increases in energy consumption and area overhead. Adding error control features to an existing NoC is not as simple as including an error control module; the flow control, routing algorithms, and buffer management all need modification to support error control. Moreover, various noise conditions must be modelled to facilitate a complete evaluation of error control capabilities.

Error control methods have been widely investigated at the data link layer. Error protection can be incorporated in the routing algorithm at the network layer. Probabilistic flooding algorithms can correct errors without retransmissions by transmitting multiple copies of packets. Unfortunately, sending multiple copies of packets typically results in large redundancy, and thus, energy consumption.ECC adaptation in the data link layer (i.e., hop-to-hop ECC), configuring the ECC codec in each router and adjusting the number of redundant wires in each link[6][7]. Hop-to-hop ECC[1]-[3] can prevent error propagation, but may waste energy if the link error rate is low.ECC is network-layer ECC (i.e., end-to-end ECC), which protects a message packet without detecting or correcting errors in the middle of the route. To consider a wide range of operating environments and the associated over-head costs, we propose a framework that can adapt ECC strength across data link and network layers to improve reliability and energy efficiency while maintaining performance.

II ERROR CONTROL POLICIES IN NOC

There are a number of solutions to handle the increasing number of errors due to technology scaling in NoC. Information redundancy or coding is one of the most feasible solutions. Nowadays the research has focused on handling limited number of error, single or double. When considering future technology scaling down, it is expected that the error rates increase drastically, these errors can be categorized into two types: transient errors which causes the component to malfunction for some time, other type is permanent errors which cause the component to malfunction forever. An efficient fault tolerance approach should consider occurrence of multiple simultaneous permanent and transient errors.

A. Hop-to-hop error control

In the widely used packet-based communication, each packet consists of data units called flits. The first flit of a packet (header) decides the routing path of the packet, and then crossbar in each router is set to forward the packet to next router. Hop-to-Hop ECC[1]-[5] is performed in the data link layer , the flits are encoded and decoded for error correction/detection in each hop of the transmission from the sender to the receiver. In order to perform the Hop-to-Hop Switch error control policy. Four encoders and four decoders are needed to be connected to each input and output, respectively. The received codeword is decoded and sent to the NI or saved in buffers or encoded and sent to S, N, W or E to continue its routing path to the destination NI. Merits and demerits of the control are as follows

1)Hop to Hop method captures error and recover the corrupted flit within current hop.

2)It prevents error accumulation and decreases need for powerful error correction codes.

3)It adds complexity to router design.

4)The communication energy on long on-chip interconnect becomes comparable to the computation energy as technology scales ; the unnecessary encoding/decoding operations waste energy when noise conditions are favourable.

B. End-to-end error control

End-to-end error control typically is performed on the entire packet in source/destination end. An acknowledge packet is sent back to the source end to request retransmitting the packet Network-layer error control coding is executed only in the network interface and does not detect or correct errors at intermediate hops in the route. merits and demerits are as follows

1) Error control does not increase router complexity and link width between hops.

2) Power consumption of end-to-end error control is less than that of hop-to-hop error control when the error rate, the route length and the number of retransmissions is small.

III RELATED WORKS

A. dual layer ECC cooperation

To exploit the benefits of hop-to-hop and end-to-end ECC for a wide range of variable noise scenarios, existing resources in different NoC layers are combined. Extend ECC adaptation from single layer to dual layer to improve energy efficiency and reliability, while maintaining performance[11]

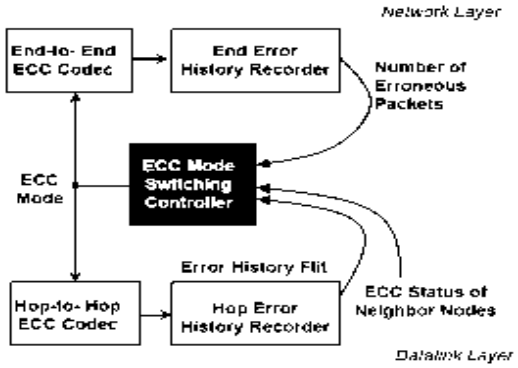

Figure 1.Dual layer cooperation ECC

A protocol for runtime ECC mode switching is proposed: only employ end-to-end ECC in low noise conditions and enhance the error control strength by turning on hop-to-hop ECC if noise increases; disable the hop-to-hop ECC when noise condition becomes favourable. Implement dual-layer adaptive error control coding. Simply combining end-to-end error control with hop-to hop error control typically results in huge energy consumption. The proposed utilization of product codes can realize non-interrupting ECC mode switching at run time. Error-tag-shifting technique [1]-[3]to record hop-to-hop ECC detection outcomes and pass them to the destination, assisting in ECC mode switching.

B . Router Architecture

The primary function of a router is to connect networks together and keep certain kinds of broadcast traffic under control. Router is the active component of network and is the key to achieve reliability and performance standard.Router supporting dual layer ECC [1]differs from conventional router design in ECC mode switch, Mode propagation counter, EHF update unit differentiate our work from conventional is shown in Figure 2. For mesh NoCs, a router typically has five input/output ports-north, south, east, west, and local. The information extractor obtains the destination address from the packet header flit. The arbiter facilitates connection between input and output ports. For a router capable of error control, NACK feedback from neighbour routers *(NACK_in)* is used by the arbiter to control first-input-first-output (FIFO) and channel reservation. The network interface executes part of the proposed ECC mode switching protocol counting the number of errors detected in the time interval and determining whether to request an ECC mode switch.Dual layer ECC codec is used for encoding and decoding purpose.

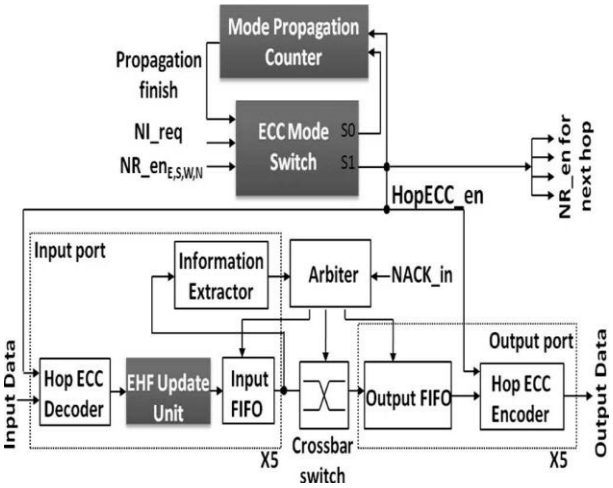

Figure 2. Router architecture

C . ECC mode switching protocol

An advanced error detection and correction protocol was invented to go a step beyond simple parity checking, Called ECC, which stands for error correcting circuits, error correcting code, or error detection code, this protocol not only detects both single-bit and multi-bit errors, it will actually correct single-bit errors[12] on the fly, transparently. Like parity checking, ECC requires a setting in the BIOS program to be enabled. Often there are two; one turns on parity checking and the other tells the system to use ECC mode.the mode switching depends on the information exchange between data link and network layers. In mode 1 (end-to-end ECC), the network interface assesses the global noise condition by counting the number of errors detected by the destination decoder, and informs the data link layer if it should use hop-to-hop ECC. In mode 2 (end-to-end ECC combined with hop-to-hop ECC), the network interface comprehensively evaluates the global noise condition with its local error counter and information passed by the error history flit, which is filled by the *EHF Update Unit* in the data link layer.

D. Drawbacks of existing system

- Error detection correction process time is complex
- More no of peripherals required for multi hop loop
- Error correction rate is poor
- Limited application can used
- Area overhead

IV PROPOSED METHOD

In this paper different error protection techniques for NoCs are presented. They are integrated into a NoC design framework,which targets FPGA-based implementations as well as VLSI implementations.Using this generic and modular framework NoCs can be easily generated allowing to modify NoC-specific parameters, like e.g. word length, error protection technique or routing algorithm.

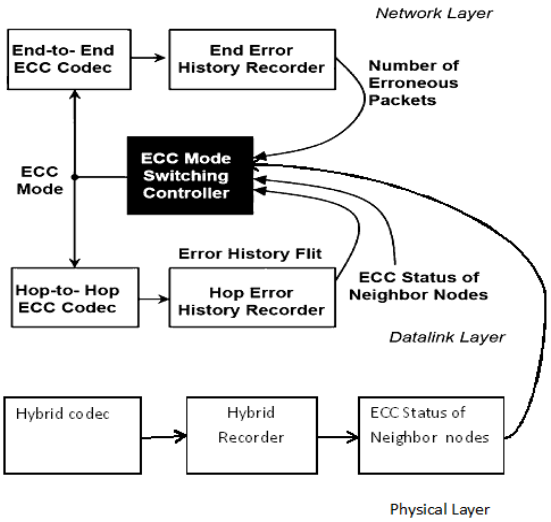

figure 3. Proposed Multilayer architecture

In this paper, we present a comprehensive study on the adaptive control schemes and the stability issues of this family of protocols over some centralized controlled network topologies.In proposed architecture, physical layer is introduced along with data link and network layer to perform Multilayer Adaptive error control.Hybrid error control is used using ECC mode switching unit. It can detect as well as correct more than two byte of data compared to previous work which can correct two byte of data and it detect error in more than Two byte of data.

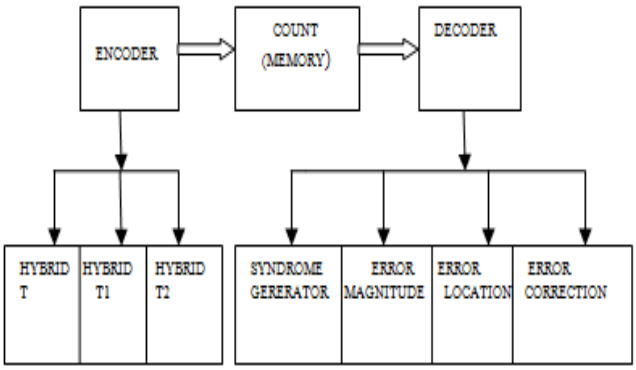

Figure 4.proposed hybrid codec architecture

The proposed design Shown in Figure 3. is designed to operate over system-level interconnects such as network-on-chip, inter-chip, and backplane interconnects. proposed design provides these interconnects with powerful error correction capability and thus effectively increases signal integrity and noise immunity. As a result, these interconnects may carry data with lower signal power and/or higher transmission rates. proposed design is designed such that support for it may be tightly integrated into high-speed, low-latency system-level I/O interfaces. Encoding and decoding may be performed at system core speeds with low

chip area. A Multilayer Error correction technique is introduced in a Network on-Chip to detect and correct more than two byte data.A physical layer is included along with the dual layer (Network and Data-link layer) named as a Hybrid Multilayer ECC.The code is very much suited from VLSI design viewpoint and requires significantly less hardware and power .In figure 4. Hybrid codec consist of the following steps like Syndrome Generation,Error Magnitude detection Error Location identification and Error correction . This Hybrid Multilayer technique is based on byte error correcting code . This scheme can correct errors provided errors are confined to information or check byte only.This scheme cannot correct if the errors are distributed both in information and check byteThe current work identifies weakness and limitation of existing Multilayer based byte ECC and proposes an improved Multilayer based double byte ECC which overcomes the identified weakness.This technique can easily be extended for correcting more than two byte errors.

V EXPERIMENTAL RESULTS

Router architecture using Multilayer ECC was implemented in VHDL and synthesized. The resulting power, Latency,delay are estimated. Energy efficiency of Mutilayer ECC are calculated and compared with the obtained results.

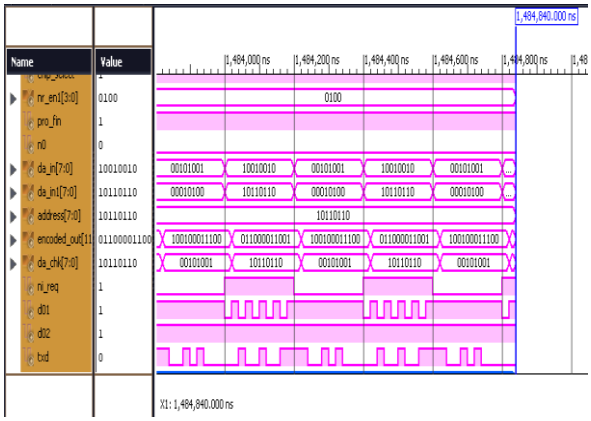

Figure 4 simulation waveform

In Figure 4, The given input data is encoded and original data is decoded at the output by using Multilayer layer Adaptive error control to improve energy efficiency.

A. Power measurements

An initial power characterization of the designs was obtained by streaming data through a single router and measuring the dissipated power.(shown in Figure 5)

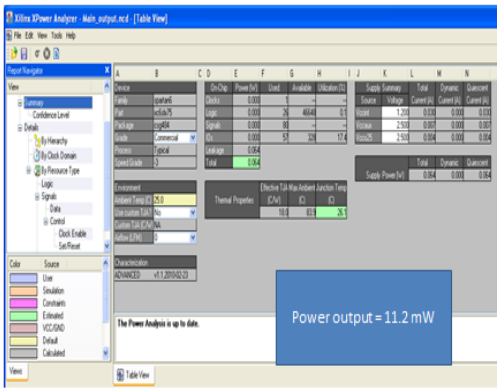

Figure 5.power output

Four fixed traffic streams were defined, one originating at each of the North, South, East, and West ports of the router, with each one transmitting a stream of packets to the opposite router port.

B. Comparison results

The proposed multilayer architecture was implemented using VHDL and the results are compared with the previous values are shown in Table1 and Table 2.

COMPARED RESULTS	ENERGY REDUCTION	LATENCY REDUCTION	ENERGY USAGE	LATENCY USAGE
EXISTING RESULTS	72%	64%	28	36
RESULT OBTAINED	89%	67%	11	33

Table 1. Energy reduction comparison chart

COMPARED DESIGNS	AREA	DELAY	LEAKAGE POWER
CONVENTIONAL ROUTING UNIT	100	100	100
EXISTING ROUTING UNIT	102.2	102.5	102.4
PROPOSED ROUTING UNIT	22%	100	100

Table 2. output parameter comparison chart

Analysis of the results in Table 2, shows by exploiting the resources of the both error control methods and cooperation of dual layer error control ,Energy reduction of 89% was obtained.

VI CONCLUSION

We have proposed a Multilayer adaptive error control in NOC Architecture to address the performance, energy and reliability issues in a variable noise and traffic environment. With the assistance of dual layer framework configuration of error control codec used in the datalink layer and network Layer and Hybrid codec in Physical layer can consider both the noise conditions and network congestion. As result,

Latency, throughput, energy and reliability are simultaneously managed .Reliability, average energy and Latency reduction is achieved by Network layer End-to-end Error Control Coding.Hop-to-hop error control reduce error propagation and accumulation.Error correction process time ,byte error correction and Packet error rate is reduced by hybrid mode.We exploited the resources of the three layers,which improves quality of error correction process. The proposed design provides the interconnects with powerful error correction capability and thus effectively increases signal integrity and noise immunity. As a result, these interconnects may carry data with lower signal power and/or higher transmission rates.

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Author Profile

Mrs.M.Jeyabharathi received her B.E degree in Electronics and Communication Engineering from Arulmigu Kalasalingam College of Engineering , Krishnankovil , Tamilnadu She is presently pursuing her M.E (VLSI Design) from Sethu Institute of Technology, Tamilnadu.Her research interests include design for testability and VLSI/NoC design verification.

MRS.C.Sujatha received her B.E degree in Electronics and Communication Engineering from P.S.N.A College of Engineering and Technology, Dindigul, Tamil Nadu,India in 1997 and M.E degree in Applied Electronics from P.S.N.A College of Engineering and Technology, Dindigul, Tamil Nadu, India in 2004. She has more than 10 years of teaching experience. Presently she is working as Associate Professor, Department of Electronics and Communication Engineering, Sethu Institute of Technology, Kariapatti, Tamil Nadu, India. She is doing research in the area of Image Processing based on FPGA under the guidance of Dr.D.Selvathi, Prof. /ECE Dept., Mepco Schlenk Engineering College, Sivakasi,Tamilnadu,India.Her research interest is FPGA based image processing.

Dr.R.Ganesan received his B.E. Instrumentation & Control Engineering from Arulmigu Kalasalingam College of Engineering and ME (Instrumentation) from Madras Institute of Technology in the year 1991 and 1999 respectively. He has completed his PhD from Anna University, Chennai, India in 2010. He is presently working as Professor and head in the department of M.E-VLSI Design at Sethu Institute of Technology, India. He has published more than 25 research papers in the National & International Journals/ Conferences.
His research interests are VLSI design, Image Processing, Neural Networks and Genetic algorithms.