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VLSI design and performance analysis of multi channel ADC using MTS algorithm

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Abstract— **This paper proposes a multi-channel low power digital ramp analog-to-digital converter (ADC) and the Metastable-then-set (MTS) algorithm is to eliminate the metastability problem in this ADC to result the output . Here the effects of power consumption and performance of ADC also have been measured with MTS algorithm. A prototype ADC was implemented in 0.13-µm CMOS technology and operated under a 1.2 V supply at a sampling rate of 50 MS/s. The measured total power dissipation of a single channel ADC is 470 µW. The flag synchronization technique minimizes the crosstalk among the channel .The VLSI implementation was done using Xilinx and Multisim Simulator.**

Index Terms — Digital Ramp ADC, low Power, Multi channel, Metastable-then-set (MTS)

I. INTRODUCTION

The SARADC is the popular architecture to achieve the low power with advanced CMOS technology [1],[5]. It is used for wide range from low frequency to giga hertz level. Generally ADC applications are used for Data acquisition, audio, voice band and speed (sampling rate > 10MS/s) .In the existing model the ASAR ADC with the solution of metastablity and possible low power was achieved for dual channel only . In the proposed model a multi channel digital ramp ADC with MTS algorithm and its effect on power consumption is elucidated.

A. Essentials of SAR ADC

Since the SAR ADC uses the comparator instead of the operational amplifier for ADC operation ,it consumes the low power. It is also used to implement the binary search algorithm. Basically it contains the blocks such as ,Successive Approximation Register (SAR),Sample-and-Hold Stage (S/H),DAC comparator its function explained as follows .first of all the input voltage is sampled by sample and hold block then the MSB bit sets to high level logic and others are low [2]. To implement the binary search algorithm if its $V_{IN} < V_{DAC}$ then the output of the comparator is low level logic other wise logic high .Then the SAR control moves to next MSB to set as high and does the another comparison it continuous till the LSB bit. The ADC. process is successful once this is completed. Then N –bit digital words can be read from the register [Fig 1]

B. State of Metastability

It occurs in all latching comparator when the input is near to reference signal, it takes the more time to result the output . its output also will be intermediate level . It is called as Metastability. so this is to be avoided for precise digital output.

This paper is organized as follows. In the Section II the MTS algorithm, its implementation in the Related work. In Section III proposed model is explained. Section IV presents the Results and parameters Measurement then the Section V concludes the paper.

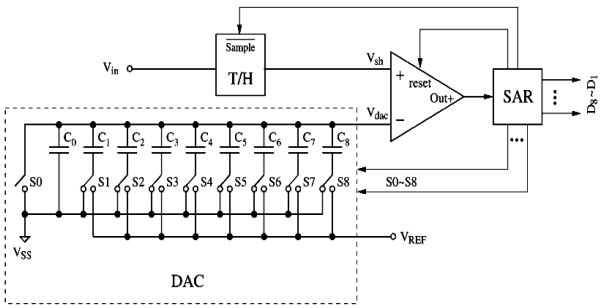


Fig. 1. N-bit SAR ADC architecture

II. RELATED WORK

A. MTS algorithm for Metastability

The ASAR ADC avoids the the usage of internal clock pulse for self triggering operation as it is asynchronous [2]. When the input to the comparator is small it suffers from metastabilty and also it takes the long time for conversion .The [Fig 2(a)] shows the block diagram of ASAR ADC and its related waveform [Fig 2(b)] . By using output of XOR except the first latching command other following operations are self conducted .It's output to notifies that whether the bit decision is completed or not. When the (VDAC≈ VSH) , it takes the long time for ADC output that is metastabilty situation is occurred. It is only after the MSB

bit decision is completed .The remaining LSB are sequentially decided to be zero. To assure that end of conversion for given time the metastabilty problem has to solved .Now the MTS algorithm is applied to solve it by assigning the unresolved codes on the chip and to complete the conversion and also it eradicates the unnecessary decision cycles .The Fig 3(a) shows the modified block diagram . Here the metastabilty detector (MD) is added [Fig 3(a)] and its waveform is shown [Fig 3 (b)]

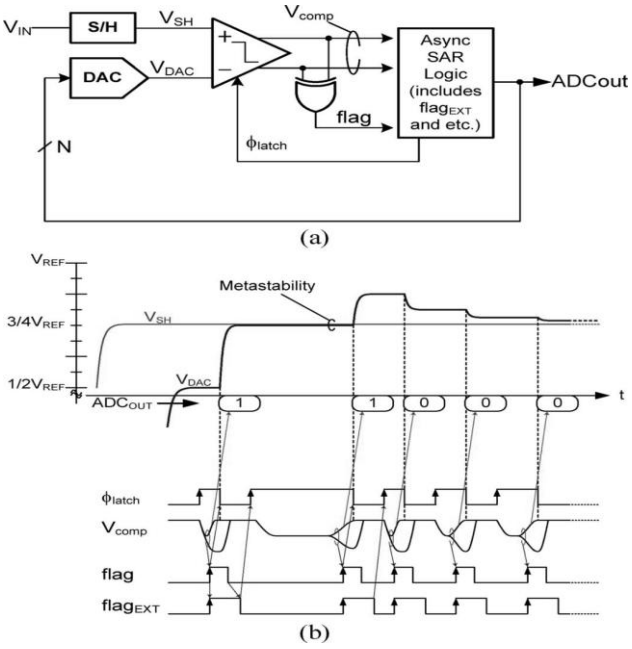
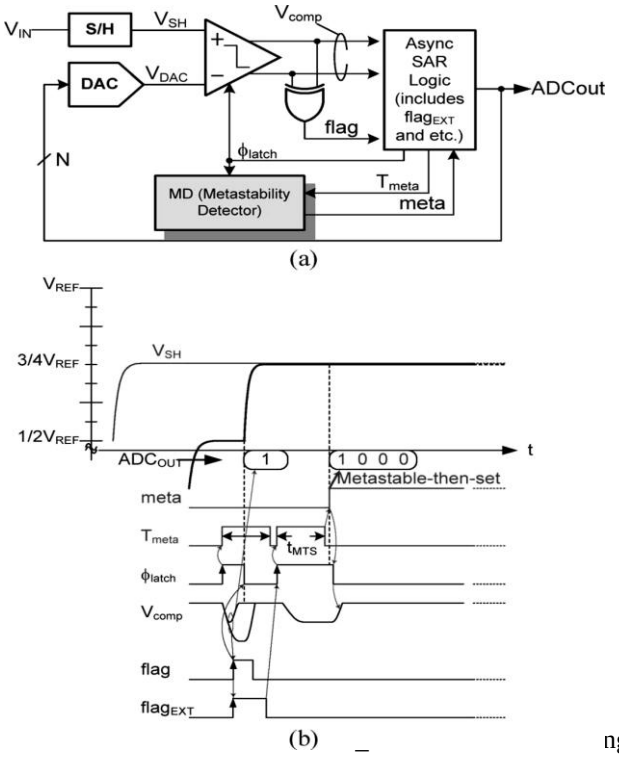


Fig . 2. (a) Block diagram of an asynchronous SAR ADC and (b) its timing diagram.

B. MTS Algorithm implementation

To authenticate MTS algorithm ,the following process are done . The time tMTS is represented for the signal Tmeta .For test purpose the ramp signal is used instead of the Tmeta . it rises with the φlatch . if it reaches the threshold (VTH_meta) before the latching is completed , it considered as metastable state . As soon as it occurs the signal meta turns on. The ramp signal is reset for both flag (or) meta appears. The time tMTS is used to control the operation. The tMTS is adjusted by changing the slope of the ramp. For ramp generation the current source (IMD) and a capacitor (CMD) are used. The slope of the ramp is increased for fixed VTH-meta and tMTS is reduced .Integrator begins to charge at the rising edge of φlatch. Integration is finished when flag=1 (or) when the metastability is detected . For VTH_meta, inverter 1 plays the important role [fig 4] .its value will be approximately half of the supply voltage. The latch is composed with inv1 and inv 2 and it holds the meta=1 till next input is sampled .To control the slope of the ramp the value of IMD is controlled externally [3] .The [fig 4b] shows the simulation waveform for with and without metastability occurrence . From this wave



ng decision are omitted for further latching commands. By considering the time period tMTS the current and power consumption can be calculated for all sections such as digital, analog and DAC section. Then the total power value is measured for same applied voltage.

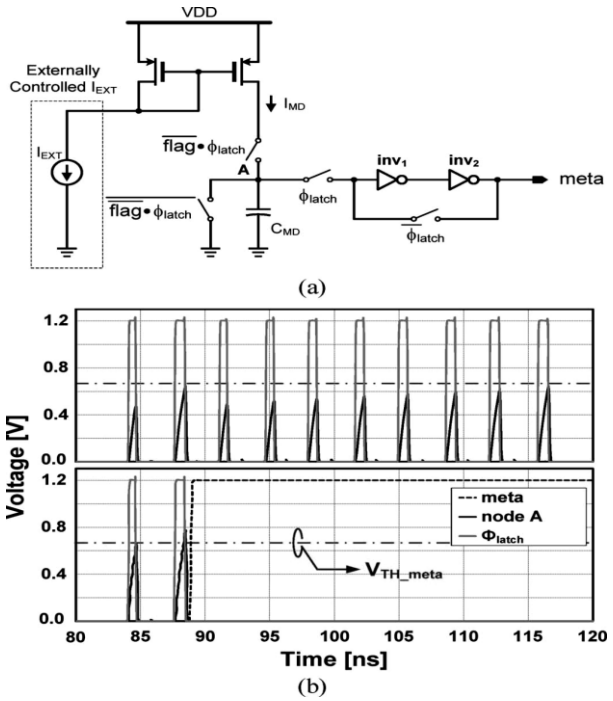


Fig .4. (a) Hardware implementation of metastable detector and (b) its simulation result

C. Negative aspect of Existing method

1) Metastability problem is solved for only two channels

2) Hardware complexity is more

3) DAC Switching takes more power

4) Implemented for 8.3 bits only

5) Sampling rate is less

III. PROPOSED MODEL

A. Multi Chennai Low power digital Ramp ADC

Minimizing the power consumption is a major goal in many designs. In the ADC, the clock rate is operational constraint when it is specified for given sampling rate. The sampling rate may affect the power consumption of an ADC .so the sampling rate is changed compared with conventional method. In the existing method of ASAR ADC it consumes the power of 570µW per channel with low sampling rate and also uses the MTS algorithm for only dual channel only.

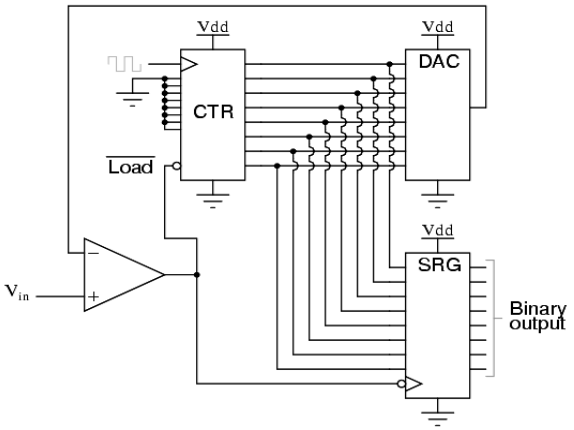


Fig.5. Digital Ramp ADC

so in the proposed model of low power multi channel digital ramp ADC [Fig 5] is presented .it is also called as counter type ADC. since it uses the shift register and counter, its hardware is simple .Here The counter counts the clock pulses and its output is given to input of DAC. The comparator compare the DAC output and Vin .Its output will be logic high when Vin > VDAC otherwise logic is low .Now due to transition comparator output causes the shift register to load whenever the binary count is being output by counter. secondly, the counter will receive a low signal on the active-low LOAD input, causing it to reset to '00000000' on the next clock pulse. The effect of this circuit is to produce a DAC output that ramps up to whatever level the analog input signal is at, output the binary number corresponding to that level, and start over again.

B. Methodology used

The proposed uses the R-2R string based DAC **.** so it **c**onsumes less power compared with capacitor array based DAC in conventional ASAR ADC because it has the parasitic capacitance effect and also ramp ADC is designed for the multi-channel operation [4]. as the metastability occurs in the comparator based ADC design, the MTS (Metastable then set) algorithm [1] is applied to eliminate this condition and the low power is also achieved with the total power consumption of a single channel ADC is 470 µW. The flag synchronization technique minimizes the crosstalk among the channels .It was implemented in 0.13-µm CMOS technology and operated under a 1.2 V supply at a sampling rate of 50 MS/s [4]. The reference voltage is shared by all channels . To measure the power the time period of test signal and sampling rate are varied . And also the power measured for all sections such as digital, analog and DAC . Then the total power value is measured for same applied voltage.

IV. RESULTS AND PARAMETERS MEASUREMENT

A. Simulation Results

The Fig 6 shows the logic output of the given block diagram without metastability detector. The Fig 7, Fig 8 shows the simulation result of With and Without metastabilty for a proposed ADC.

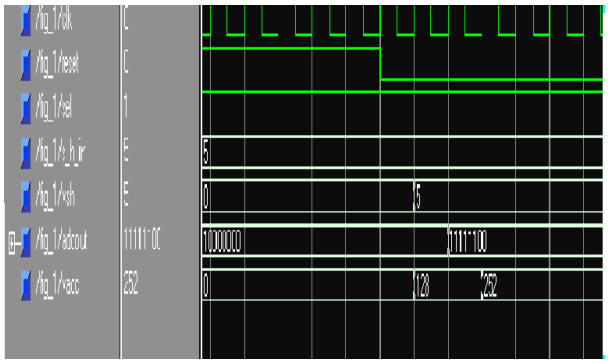


Fig .6 . Logic output of Fig. 2 (a)

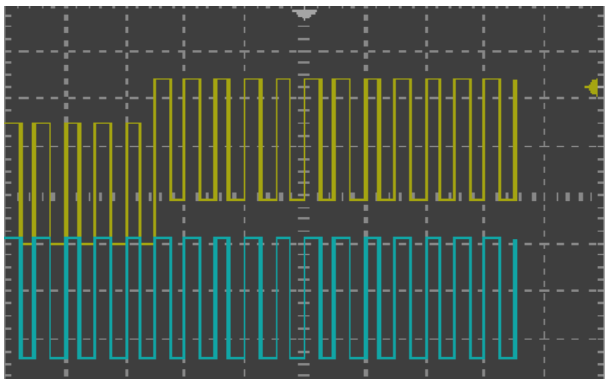


Fig. 7. Metastability condition in ADC

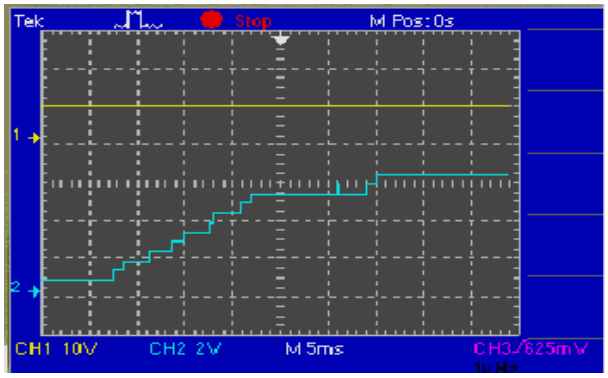


Fig. 8. Without metastabilty after MTS algorithm

B. Parameters measured

The proposed VLSI architecture of multi channel low power Digital Ramp ADC was implemented using VHDL. The Table-1 shows the different measured values.

TABLE I .MEASURED POWER

Parameters	**Values**	
Sampling Rate	50 MS/ s	
Power consumption (Single channel) @ 1.2 V	Analog	45 µW
	Digital	315 µW
	DAC Switching	110 µW
	Total	470 µW
Effective number of bits	10 bits	

V.CONCLUSION

This paper examines the potential usage of a multi-channel digital ramp ADC with solutions for metastability, crosstalk and low power achievement.The proposed model offers the low power, better sampling rate and simple hardware architecture when compared with the conventional technique. Application of MTS algorithm not only solves the metastability problem but also shows possible power savings. The flag synchronization technique reduces the crosstalk between among channels and common reference is shared by all channels for dynamic performance efficiently.

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