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The Effect of PSNA and Temperature Coefficient from the Threshold Voltages of nmos and pmos Device

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***Abstract*--This paper presents an implementation of a cmos voltage reference core designed with the mutual compensation of the threshold voltages of nmos and pmos device and to see the effects of temperature coefficient and power supply noise attenuation, since they play a major role for enhancing the application range in vlsi design, by using different circuit parameters the problem of fixed voltage reference value is also been eliminated. Here the temperature dependence of the carrier mobility is greatly reduced without using sub threshold characteristics.The experimental results is implemented with 180nm with a supply voltage of 3v and the temperature coefficient and PSNA are found to be 13.3ppm/˚C and 6.56mW using CADENCE analog environment VIRTUOSO. The results are tabulated and the future work is to enhance the PSNA with decreased power dissipation and temperature coefficient which will expand the application range of the designed reference core.**

Index terms- CMOS voltage reference ,power supply noise attenuation, temperature co-efficient, carrier mobility.

I. Introduction

Voltage references are used in almost all analog and digital systems for their high accuracy and temperature independence .

Either diodes or bipolar junction transistors (BJTs) are used in conventional bandgap reference (BGR) circuits. In a standard CMOS process, a parasitic vertical BJT is widely used to implement a BGR. Unfortunately, the parasitic BJTs are usually not very well characterized, and more area will be also occupied.

As an alternative, voltage references in MOS technology can be also implemented by the principle of threshold voltage difference, which is based on selective channel implant flat band voltage difference with different gate materials and work-function difference with different gate doping .However, these reported solutions are not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed. In[13]a weighted difference between the gate–source voltages of two MOS transistors is used to implement voltage references. Design solutions of this type compensate the temperature dependence of carrier mobility only at the reference temperature, thereby providing a degraded temperature coefficient when the circuit is not at the reference temperature [9]. In [9], MOSFET-only voltage references without the temperature dependence of mobility are realized. Either special devices or subthreshold characteristics are required to implement the circuits. Special devices will need extra manufacture steps, which will increase the cost of fabrication. Although low power can be easily achieved, transistors biased in the subthreshold region may complicate the design process, where accurate device models are not usually available, particularly in digital CMOS technologies, and can be greatly influenced by the variations of process. Based on a weighting function of threshold voltages, a new architecture for a high-precision CMOS voltage reference with enhancement-mode MOS transistors biased in the strong inversion region is presented in this brief, which overcomes the problems listed above. The structure is quite simple, and the chip area is small. Only MOS transistors and resistors are used.

Hence in this process by overcoming all those disadvantages, here, by utilizing mutual compensation of the threshold voltages of enhancement-mode nMOS and pMOS transistors, a novel temperature-stable non bandgap voltage reference has been proposed and implemented by standard 180nm CMOS technology without any special device or sub threshold transistor. The complete suppression of the temperature dependence of carrier mobility in the whole temperature range is realized, and the output reference voltage can be flexibly adjusted by resistor ratios in accordance with the requirement of systems. Negative feedback branches are embedded in the proposed structure to improve the PSNA and line regulation further.

Research in this paper focuses on reducing the power dissipation and temperature coefficient and to enhance the power supply noise attenuation The section II gives a complete background analysis of the existing research work, section III describes about

the designed voltage reference section IV describes the linear voltage associated with the threshold voltage and the voltage reference generator ,section V includes the experimental and analysis.

II. Related Work

Various researches are conducted in the field of voltage reference. Some of the interesting and key notes is explained below:

A. Bendali and Y. Audet [1] proposed a project describing a 1-V current reference fabricated in a standard CMOS process. Temperature compensation is achieved from a bandgap reference core using a trans impedance amplifier in order to generate an intermediate voltage reference,Vref. This voltage applied to the gate of a carefully sized nMOS output transistor provides a reference drain current, Iref, nearly independent of temperature by mutual compensation of mobility and threshold voltage variations.

G. Iannaccone and G. De Vita [9] proposed a project where The objective is to developed an extreme low power voltage reference generator operating with a supply voltage ranging from 0.9 to 4 V and had been implemented in AMS 0.35- m CMOS process. The maximum supply current measured at the maximum supply voltage and at 80˚C is 70 nA. A temperature coefficient of 10 ppm/˚C is achieved as the combined effect of 1) a perfect suppression of the temperature dependence of mobility; 2) the compensation of the channel length modulation effect on the temperature coefficient; and 3) the absence of the body effect. The power supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz is lower than 53 and 42 dB, respectively. The occupied chip area is 0.045 mm².

K. N. Leung and P. K. T. Mok [13] proposed a CMOS voltage reference, which is based on the weighted difference of the gate–source voltages of an NMOST and a PMOST operating in saturation region. The voltage reference is designed for CMOS low dropout linear regulators and has been implemented in a standard 0.6- m CMOS technology.

F. Franco and P. S. Crovetti [18] proposed a project describing a new circuit integrated on silicon, which generates temperature-independent bias currents. Such a circuit is firstly employed to obtain a current reference with first-order temperature compensation, then it is modified to obtain second-order temperature compensation. The operation principle of the new circuits is described and the relationships between design and technology process parameters are derived. These circuits have been designed by a 0.35 m BiCMOS technology process and the thermal drift of the reference current has been evaluated by computer simulations.

J. Redoute and M. Steyaert [21] proposed a project that evaluates the effect of conducted electromagnetic interference (EMI) that is injected in the power supply of a classic Kuijk bandgap reference voltage circuit. Two modified Kuijk bandgap topologies with high immunity to EMI are introduced and compared to the original structure. Measurements of a test IC confirm the theoretical analyses.

III. PRINCIPLE OF THE VOLTAGE REFERENCE

The magnitude of the threshold voltage is a linear function of temperature

$$|VTH(T)| = |VTH(To)| - \alpha VT(T - To) \quad (1)$$

where ,

T0 is the reference temperature, and

αVT is the TC of the threshold voltage.

The nonlinear temperature dependence of mobility can be expressed as $\mu(T) = \mu(To)(T/To)\alpha$.

Where, μ(T0) is the carrier mobility at temperature T0, and α is usually between −1.5 and −2.

Due to the nonlinear temperature behavior of mobility, the TCs of the output voltage in many structures are usually degraded as a result of incomplete cancellation. A significant reducti mobility's TC is then needed for better performance, which is solved in the designed voltage reference. Fig.1 shows the concept of the proposed voltage reference core.

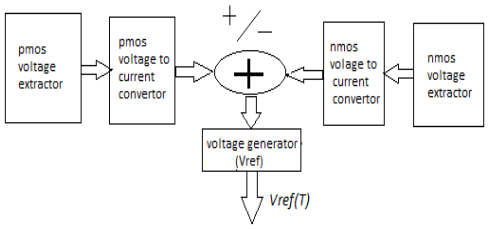

Figure 1.Block diagram of the voltage reference

Two threshold voltage extractor circuits are used to obtain voltages, namely, VPTTVn and VPTTVp, which are proportional to threshold voltages (PTTVs) of nMOS and pMOS, respectively. The temperature dependence of the two PTTVs, which are linear functions consistent with equation (1), is illustrated with dashed frames in Fig.1. Then, the two PTTVs are converted into currents by V −I converters for the convenience of superposition. By subtracting these currents in a proportion required by the technology, the TC can be cancelled, and the resulting voltage can be adjusted to the desired level through the I–V converter.

All resistors used in the proposed design are made by the same material. To be convenient for description, the TC of the resistors is temporarily

ignored, and the influence of the resistances' TC on the proposed voltage reference will be considered at the end of the analysis .

IV. SCHEMATINC AND WORKING

The Linear Voltage Associated With Threshold Voltage can be explained as follows. The VPPTVn extractor is shown in the right part of Fig.2. All the transistors work in the active region. Although the structure is similar to the one employed in the previous paper, the design methods are completely different. There it was used to achieve a first order temperature-compensated current reference. The main idea was to eliminate the positive temperature drift of transistors' overdrive voltages with the help of the mobility's negative drift. However, the extractor circuit is designed to extract the transistors' threshold voltage instead of the temperature compensated current reference. The extractor principle is utilizing the quadratic strong inversion current model. The relationship can be expressed as

$$\mathbf{Vgs=Vth+\sqrt{(2Id/(\mu CoxW/L)}} \quad (2)$$

Where,

VTH is the threshold voltage,

ID is the drain current,

μ is the carrier mobility,

COX is the oxide capacitance per unit area

W/L is the width length ratio of the MOSFET transistor's channel.

Given

(W/L)MP5 =4(W/L)MP4 = 4(W/L)MP6,

and the W/L ratios of transistors MN1, MN2, and MN3 are the same, the voltage VPTTVn can be derived with the help of Kirchhoff's law and equation (2), i.e.,

$$\mathbf{VPTTVn=VTH(MN1)+VTH(Mn2)-VTH(Mn3)} \quad (3)$$

In a standard p-substrate n-well CMOS process, all the nMOSFETs can only be fabricated in the same p-substrate. Hence, transistors MN1 and MN3 have bulk-bias, which affects the threshold voltage's value and temperature dependence. The difference between VTH(MN1) and VTH(MN3) is mainly determined by the difference between VGS(MN2) and VPTTVn. In order to minimize the difference, the effective method is to minimize the overdrive voltage, which is realized by making the W/L ratios of MN1, MN2, and MN3 large enough. This way, VTH(MN1) and VTH(MN3) can be approximately equal, and the voltage VPTTVn is simplified as

$$\mathbf{VPTTVn = VTH(MN2)} \quad (4)$$

Therefore, VPTTVn is PTTV of nMOS without the effect of carrier mobility. That means VPTTVn will be strongly linear with temperature, which has a negative TC. Even if different bulk bias produces slightly different threshold voltages for MN1 and MN3, these threshold voltages still have linear dependence on temperature . That will not change the temperature characteristics of VPTTVn. The current, i.e., IPTTVn, can be expressed as IPTTVn = VTH(MN2)/(4R1).

The power-supply noise attenuation (PSNA) represents the anti-interference ability of the output to supply disturbances, such as crosstalk, noise, and so on. Therefore, the higher the PSNA is, the better the performance of reference .In order to enhance the PSNA and line regulation without great increase in supply voltage, a negative feedback loop formed by MN4, MN5, and MP6 is embedded in the circuit instead of cascade structure. Through this method, the difference between voltages at nodes A and B can be reduced by properly setting the sizes of MN4 and MN5, and the output terms can be stabilized. As a result, errors introduced by channel-length modulation can be neglected, and relatively long channels are not necessary for all transistors in the circuit, which are essential in conventional structures. Accordingly, chip area can be greatly reduced. Given the voltage at node B rose due to the change of supply voltage VDD, the voltage at node C would fall. Then, the voltage of node A would rise. Since the effect of the negative feedback loop formed by MP5, MN1, MN2, MN3, and R1 is greater than that of the positive feedback loop of MP4, the voltage at node B would fall, and vice versa.

The rightmost part in Fig.2 is the startup circuit for the VPPTVn extractor. As the voltages at nodes A and B are low, and the voltage at node C is high at the beginning of the startup process, MS3 turns on. Then, the voltage at node C will be pulled down, and there will be a current flowing into MP4 and MP5. As a result, the voltages at nodes A and B will rise. Therefore, the proposed VPTTVn extractor is driven toward the desired stable state. MS3 can be turned off when the voltage at node A exceeds some amount. Thus, the startup circuit will not the normal operation of the proposed extractor The VPTTVp extractor, whose theory is similar to the VPTTVn extractor, is shown in the left part of Fig.2. The current, i.e., IPTTVp, can be expressed as IPTTVp =|VTH(MP1)|/(4R2).

The middle part in Fig.2 is the voltage reference generator. As previously analyzed, IPTTVn and IPTTVp are PTTVs of nMOS and pMOS, respectively. Although both IPTTVn and IPTTVp have negative TCs, they are different in value. With current-mode approach, these two currents can be subtracted with different weighting values to form a near zero-TC output voltage. Taking into consideration the W/L ratios shown in Fig.2, the reference voltage VREF can be described by

$$\mathbf{Vref=(k1/4)(R3/R2)\{|Vth(MP1)|-(k2/k1)(R2/R1)Vth(MN2)\}} \quad (5)$$

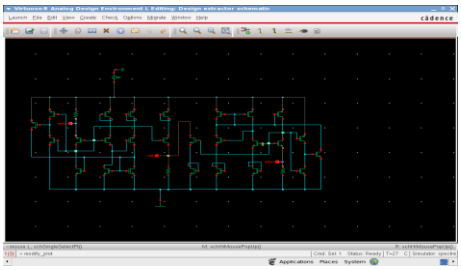

Figure 2. Schematic Of The Voltage Reference Core.

Hence, VREF is based upon two linear voltages. The coefficients k1, k2, and R2/R1 are used to cancel the TC differences between threshold voltages of nMOS and pMOS, whereas the coefficient (k1R3)/(4R2) is used to set the reference voltage to a desired level. Regardless of temperature value, the effect of mobility's temperature dependence is also completely removed. Since equation (7) indicates all resistors used in the circuit appear in the form of resistor ratios, the TC of the resistances has little influence on the reference output voltage by using the same type resistors.

V.EXPERIMENTAL RESULTS

Output waveforms

Figure.3 Temperature dependence of the BGR at 3V

The output waveform shows the temperature dependence of the proposed band gap reference circuit at 3V ,likewise the samples are taken for different input voltages 1.8V,3V,4.5V. The corresponding outputs from the extractors are also observed.

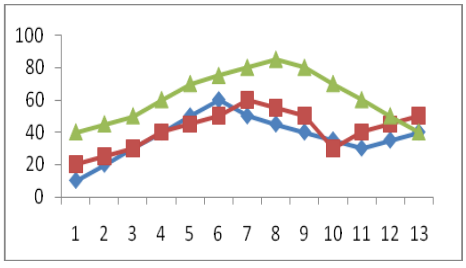

Fig ure 4. Measured temperature dependence of three trimmed samples

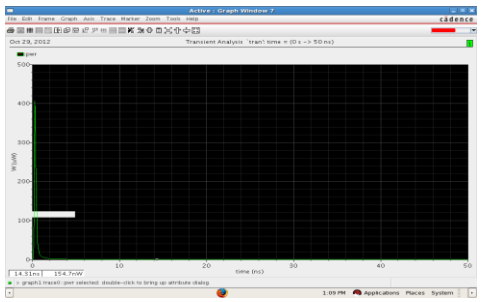

Figure 5.Transient Power Analysis Of The Voltage Reference Core

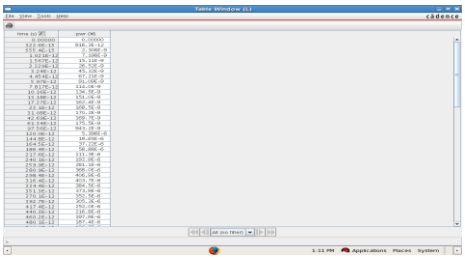

Figure 6. Power Table Of The Voltage Reference Core

The graph in fig 5.17 shows the transient power analysis of the voltage reference core in terms of watts and the fig 1.1 is the table representing the graph 5.18 in terms of values. Hence the power is found to be 154.7 nW

Parameter	proposed	Leung et al[13]	Lam et al[3]
Technology	180nm	180nm	180nm
Supply voltage	1.8|3|4.5 V	1.4-3V	1.75V
Supply current	8µA	9.7µA	6.6µA
Temperature coefficient	13.3	34.7	11.8
Line regulation	0.3mV/V	0.533mV/ V	1.28mV/ V
PSNA	6.5mW	179.8nW	154nW

Table 1: Comparison Chat

It summarizes a comparison on the results of the voltage reference and other voltage references reported in literature, which were fabricated with a CMOS process. The supply current of the proposed voltage reference is comparable to other solutions listed in Table I. Moreover, from Table I, it can be noted that the PSNA and the line regulation are superior to other voltage references already presented in the literature and the power is found to be 154.7nW.

VI. CONCLUSION

The complete suppression of the temperature dependence of carrier mobility in the whole temperature range is realized, and the output reference voltage can be flexibly adjusted by resistor ratios in accordance with the requirement of systems. Negative feedback branches are embedded in the structure to improve the PSNA and line regulation further. It is observed that the PSNA and line regulation are enhanced in the proposed system. Future research based on the implemented voltage reference circuit theory is to lower Temperature coefficient and power dissipation further that will greatly expand the application range of the proposed voltage reference.

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