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Subthreshold Design of Second Generation Current Conveyor

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***Abstract*—Current mode circuits like current conveyors have attained significant importance especially in the field of current analog ICs design as compared to their voltage mode counterparts due to higher speed, lower power consumption and lesser chip area. This paper presents the design and optimization of ultra-low power second generation current conveyor (CCII) in the subthreshold region. Optimal sizing of transistors for different designs has been done at low supply voltages ranging from ±0.7V to ±0.25V. A design operating at supply voltage of ±0.25V and bias current of 20pA was found to be optimal. HSPICE simulations were performed to measure various performance parameters of CCII at the 32nm technology node.**

Index terms –ultra-low power,subthreshold, current conveyor,current mirror,non-minimal length design.

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I. INTRODUCTION

Ultra-low-power (ULP) design is important for biomedical systems. These systems should be small, consume minimum power and dissipate minimum heat. A fully implanted system with a battery that has a limited number of wireless recharges must operate under stringent low-power constraints such that constant surgery is not needed to change the battery in a patient. Thus, ULP operation will always be paramount in implantable biomedical systems [1]. ULP demands that the transistors should operate in the subthreshold regime where the supply voltage is lower than the threshold voltage of a MOS transistor.

A. Subthreshold operation of a MOS transistor

In subthreshold regime, the drain current in a MOSFET is given by

$$I_D = I_0 \frac{W}{L} e^{\frac{Vgs - Vth}{nVt}} (1 - e^{-Vds/Vt}) \qquad (1)$$

whereI_0 is the technology dependent subthreshold current extrapolated for $Vgs = Vth$, $Vt = kT/q$ is the thermal voltage, $\frac{W}{L}$ is the aspect ratio and 'n' is the subthreshold factor [2]. The operation of MOS device in subthreshold region is necessary for ultra low power circuits [3]. A whole class of CMOS circuits has been developed for the weak inversion operation of MOS device [4]. The MOS device can be used to achieve higher gain in subthreshold region as I_D is exponentially dependent upon Vgs. But the speed of subthreshold circuits is severely limited because of large device sizes and low drain current [5]. It is possible to operate devices at quite low voltages in the range of 0.25-0.3V without sacrificing their functionality in subthreshold regime that reduces power consumption at the cost of reduced speed.

There is a need of a basic building block that can be used to implement large number of different analog functions and that too in the subthreshold region. Second generation current conveyor (CCII) can be regarded as a real competitor for the operational amplifier (OPAMP). The classical OPAMP has suffered from constant gain band-width product problem and has low slew rate at its output. It has unreliable frequency response and remains unsatisfactory for high frequency applications. CCII, being a current mode device, has larger dynamic range, higher band-width, greater linearity, simpler circuitry, lower power consumption, and reduced chip area as compared to their voltage mode counterparts like Operational amplifiers. Due to its flexibility and versatility, CCII finds applications in realising impedance convertors, integrators, differentiators, filters etc. [6-9]. Few low voltage CCII structures have been reported so far operating at a supply voltage of 1V or less but they are unable to meet ultra-low power constraint on account of their complex structure [10-12]. Current conveyor structures, characteristics and performance have been investigated in super-threshold region [13-14]but to the best of our knowledge its design, performance and characteristics have not yet been explored under subthresholdcondition. Hence, this paper investigates, for the first time, the design and optimization of a CCII under subthreshold condition.

The rest of the paper is organized as follows. A brief introduction of CCII is given in section 2. Section 3 and 4 dealwith the design and performance analysis of various parameters of CCII for different designs.In section 5, variability analysis of optimal design is done using Monte Carlo analysis followed by the design of an instrumentation amplifier based on the designed CCII in section 6. Section 7 then concludes the paper.

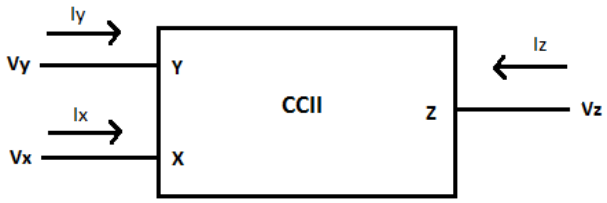


Figure 1 CCII block diagram

II. BASICS OF SECOND GENERATION CURRENT CONVEYOR

The first generation current conveyor was introduced by Sedra and Smith in 1968. Later in 1970, they came up with a novel type of current conveyor known as second generation current conveyor [20-21]. Second generation current conveyor (CCII) is basically a versatile current mode (CM) device which conveys current with unity gain from the input port to the output port. With one high input impedance, one low input impedance and one high output impedance, it is a suitable element for both voltage-mode and current-mode circuits and can be used to perform many useful functions. The block diagram representation of CCII and its internal transistor implementation are shown in Figures 1 and 2 respectively.

The characteristic equations of the dual output current conveyor can be represented as follows:

$I_Y=0$ (2)

$V_X=V_Y$(3)

$I_Z=\pm I_X$ (4)

where V_X and V_Y are the voltages at ports X and Y, respectively. I_X and I_Y are the currents entering ports X and Y. Moreover, I_{Z+} is the positive-type output current and I_{Z-} is the negative type output current. Ideally, a current conveyor should satisfy the following conditions:

1) Infinite input impedance (R_Y) at port Y.
2) Zero input impedance (R_X) at port X for current inputs.
3) Infinite output impedance (R_Z) at port Z.
4) Unity current transfer gain between ports X and Z.
5) Unity voltage transfer gain between ports Y and X.
6) Infinite bandwidth.

III.CCII STRUCTURES AND DESIGN CONSIDERATIONS

Figure 2 uses a mixed translinear loop (transistors M1–M4) as the input of the CCII. Transistors M9, M10 and M11, M13 form two current mirrors that allow the mixed loop to be dc biased by the current. The input transistors present a high input impedance at port Y and a low impedance at port X. This configuration acts as a voltage follower. The output Z copies the current flowing through port X and is realized in the conventional manner using two complementary mirrors as current follower.

The following section presents the design of a translinear loop based CCII in the subthreshold regime. The critical issue in designing translinear based CCII structure in the superthreshold region is the matching of NMOS and PMOS loop components in which μ_n and μ_p are process dependent parameters [14]. The situation becomes more critical in subthreshold region especially for submicron devices. Considering the various trade off conditions, different designs of translinear CCII structures are simulated using PTM 32nm level-54 model [16]. The performance evaluation of each design is carried out on the basis of various key characteristics of CCII namely current gain (α), voltage gain (β), current bandwidth, voltage bandwidth, resistances and their respective bandwidths at various ports of CCII.

A. Design of classic translinear structure

The design begins by transistor sizing on the basis of mobilities of NMOS and PMOS transistors. The adjusted aspect ratios of different transistors in [13, 23] are such that will keep all the transistors in the saturation region and they utilize 0.35 µm and 0.25 µm CMOS process parameters respectively. The optimal sizing of each transistor in this design of the current conveyor is done according [13, 23] using 32nm technology node. The supply voltage and bias current are adjusted such that all the transistors operate in the subthreshold region ($V_{gs}<V_{th}$). The aspect ratios of the transistors are listed in Table 1.

The supply voltage is varied from ±0.7V to ±0.3V and the bias current is also changed for a particular supply voltage keeping all the transistors in the subthreshold region. All simulations are performed using HSPICE and performance parameters variations are plotted in Figures 4-10. Table 2 lists the performance parameters at ±0.3V supply voltage and at a bias current of 5nA and is compared with [13].

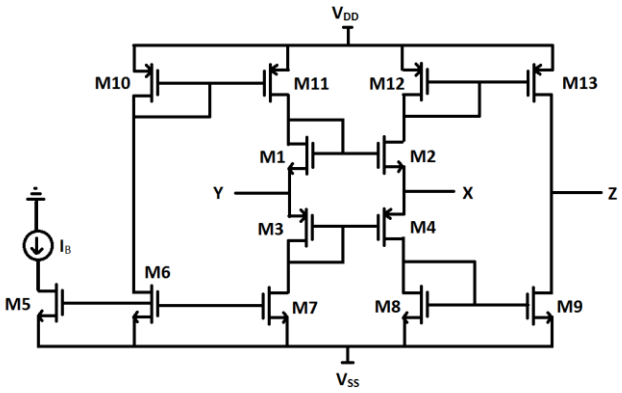


Figure 2 CMOS based circuit of CCII

Table 1. Transistors channel widths and lengths

Transistor	W/L
M1-M2	1.28µm / 0.064µm
M3-M4	2.048µm / 0.064µm
M5-M9	0.768µm / 0.064µm
M10-M13	1.28µm / 0.064µm

Table 2. Performance parameters of CCII

	[13]	This Design
V_{DD}	±1.5 V	±0.3 V
I_B	50 µA	5 nA
α	1.02	1.0413
β	0.9515	0.9328
α-3dB (MHz)	393	5.38

β-3dB (MHz)	503	6.14
R_X	1.44 kΩ	3.81 MΩ
R_Y	37.54 kΩ	124.06 MΩ
R_Z	197.1 kΩ	185 MΩ
3dB R_X (MHz)	-	18.7
3dB R_Y (MHz)	-	0.182
3dB R_Z (MHz)	-	0.374

It can be observed from Table 2 that as the supply voltage and bias currents are reduced, there is a significant reduction in power dissipation as the transistors are moved into the subthreshold region at the cost of reduced bandwidth and higher port resistances. However, there is a considerable current mismatch in the current mirror as we move deep into the subthreshold region by reducing the bias current and supply voltage due to drain induced barrier (DIBL) lowering as explained below.

B. Subthreshold current mirror

By using equation 1, the ratio of drain currents of M1 and M2 can be written as follows:

$$\frac{I_{out}}{I_{in}} = \frac{I_0(\frac{W}{L})_2 e^{\frac{Vgs\,2-Vth2}{nVt}}(1-e^{-Vds\,2/Vt})}{I_0(\frac{W}{L})_1 e^{\frac{Vgs\,1-Vth1}{nVt}}(1-e^{-Vds\,1/Vt})} \quad (5)$$

If both transistors have the same aspect ratio and Vds>4Vt ≈100mV, then $\left(1-e^{-\frac{Vds}{Vt}}\right)$ ≈1, and hence, the above equation can be re-written as:

$$\frac{I_{out}}{I_{in}} = \frac{e^{\frac{Vgs\,2-Vth2}{nVt}}}{e^{\frac{Vgs\,1-Vth1}{nVt}}} \quad (6)$$

In equation 1, the threshold voltage Vth also depends on the drain-source voltage Vds (through the drain induced barrier lowering (DIBL) effect) and the bulk-source voltage Vbs (through the body effect) according to

$$Vth = Vth0 - \lambda dsVds - \lambda bsVbs \quad (7)$$

where$\lambda ds > 0$ is the DIBL coefficient and $\lambda bs > 0$ is the body effect coefficient [24].

Since $Vgs1 = Vgs2$ and source and body are at same potential, so $Vbs = 0$, hence the above equation reduces to,

$$\frac{I_{out}}{I_{in}} = e^{\frac{Vth1-Vth2}{nVt}}$$

$$\frac{I_{out}}{I_{in}} = e^{\frac{\lambda ds\,(Vds\,2-Vds\,1)}{nVt}}$$

$$\frac{I_{out}}{I_{in}} = e^{\frac{\lambda ds\ \Delta Vds}{nVt}} \quad (8)$$

Where, $\Delta Vds = Vds2 - Vds1$

Hence, current mismatch in subthreshold current mirror is exponentially dependent on drain to source voltage mismatch.

The expressions for the current gain (α) and voltage gain (β) is given as [25]

$$\alpha = \frac{I_Z}{I_X} = \frac{g_{m2}g_{m8}g_{m13}+g_{m4}g_{m9}g_{m12}}{g_{m8}g_{m12}(g_{m2}+g_{m4})} \quad (9)$$

$$\beta = \frac{V_X}{V_Y} = \frac{g_{m2}+g_{m4}}{g_{m2}+g_{m4}+(rds2)^{-1}+(rds4)^{-1}} \quad (10)$$

It can be deduced from Figure 4 that for a particular supply voltage as the bias current increases, current gain tends towards unity. When the bias current increases, drain to source voltage mismatch of current mirrors reduces and hence from equation (8), current mismatch also reduces.Thus, current gain comes closer to unity.

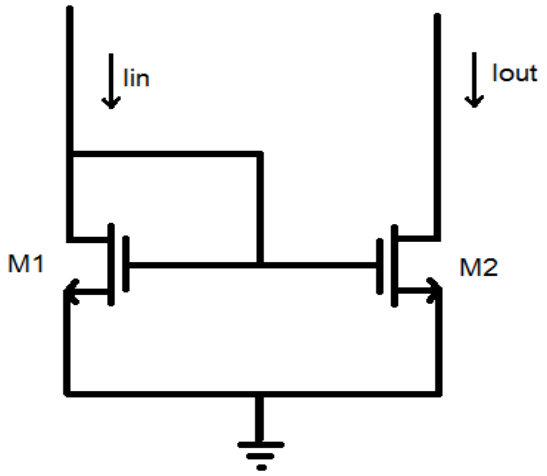


Figure 3. Basic Current Mirror circuit

Figure 5 shows the variation of the voltage gain with the bias current and the trends are just the reverse of Figure 4. For a constant supply voltage, if bias current increases then the deviation of the voltage gain from unity increases. As bias current increases, drain to source resistances r_{ds} reduces and hence from equation (10) voltage gain β deviates away from unity with β<1. It is possible to find the optimum supply voltage and bias current by the intersection of current and voltage gains curves which gives least possible deviations in current gain and voltage gain. Figures 6-7 show the variation of the voltage and the current bandwidths with the bias current respectively. Simulation results indicate that both the 3-dB current and voltage bandwidths decrease as the bias current and supply voltage reduce. The observed reduction in the bandwidths is due to the lower value of transconductance at lower current /voltagelevels**.** Furthermore, it is observed from Figures 8-10 that the resistances at ports X, Y, and Z increase in a similar manner on the reduction of bias current and supply voltage due to lower current level. The observed trends indicate that an optimum supply voltage and bias current have to be investigated to achieve optimum performance of a CCII.

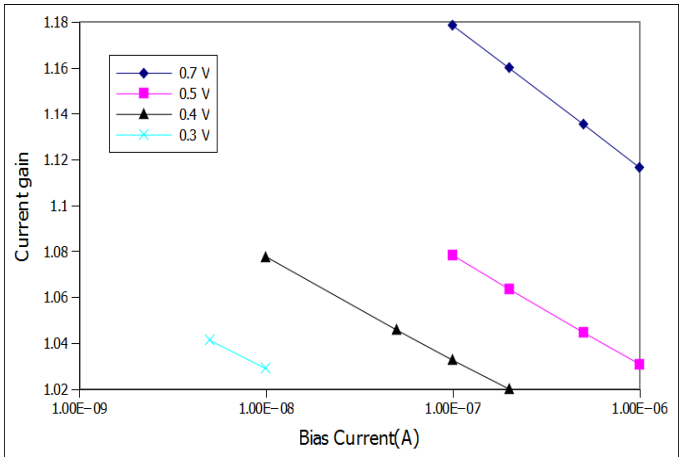


Figure 4

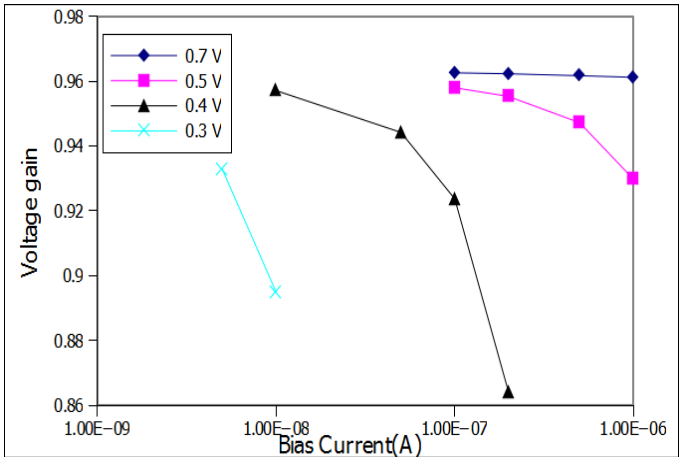


Figure 5

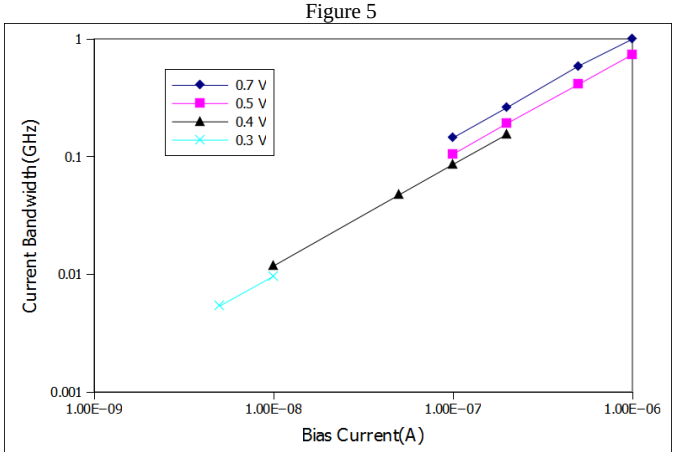


Figure 6

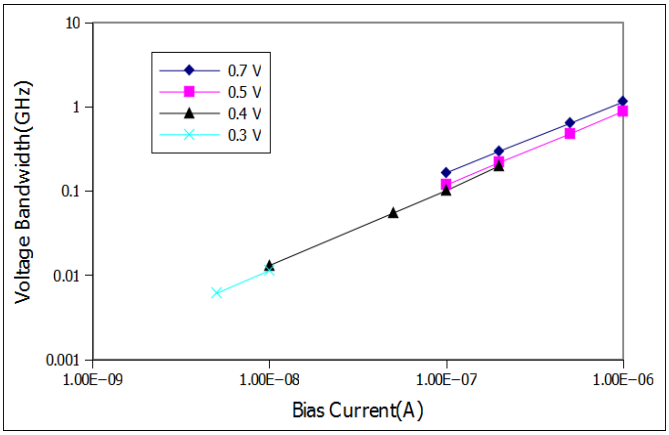


Figure 7

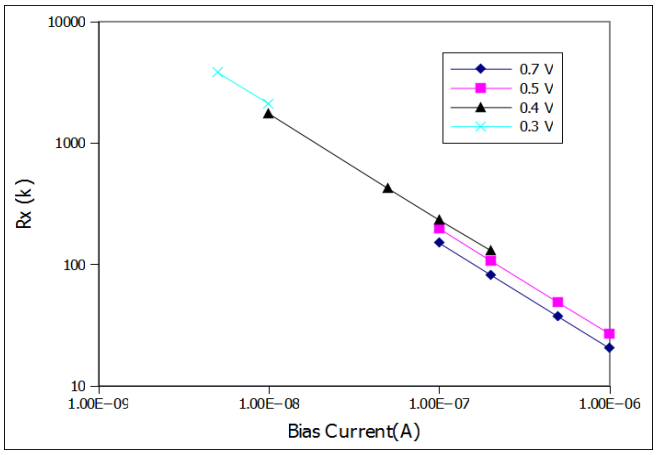


Figure 8

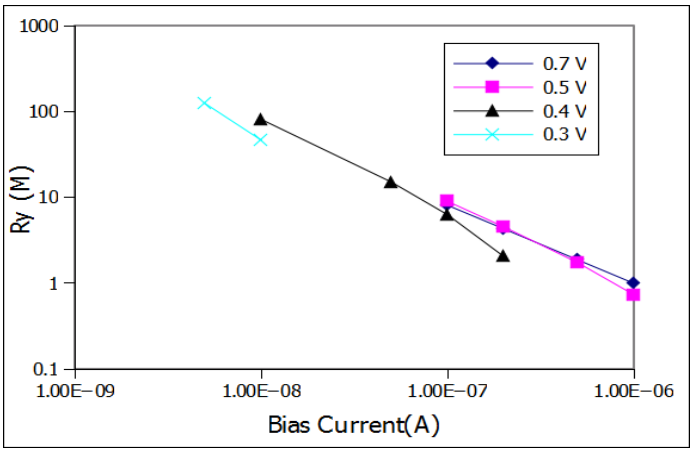


Figure 9

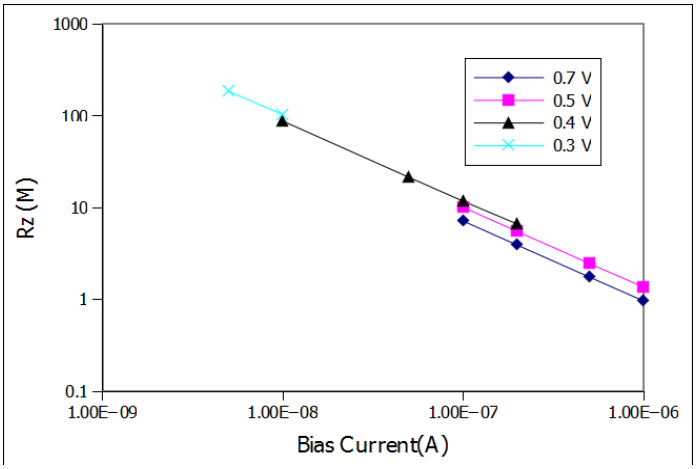


Figure 10

IV. NON-MINIMAL LENGTH DESIGNS OF CCII

This section investigates different designs by incorporating non-minimal length of transistors and various performance parameters have been evaluated keeping all the transistors in the subthreshold regime. The various designs and their aspect ratios are listed in Table 3. To begin with, aspect ratios of M5-M9 (NMOS) are chosen depending upon silicon area consumption allowance. Depending on the μ_n/μ_p ratio of 32nm technology, aspect ratios of M10-M13 (PMOS) are chosen to be 3.5 times that of M5-M9. For M1-M2 and M3-M4, aspect ratios are chosen to be 1.5 times of M5-M9 and M10-M13 respectively. Design 1 to Design 4 follows the same procedural steps of choosing the aspect ratios of various transistors. As shown in Table 3, aspect ratios of M5-M9 are subsequently scaled down from 5 to 0.25 from Design 1 to Design 4.

Supply voltage is varied from ±0.3V to ±0.25V and bias current is varied from 750 pA to 20 pA for different designs. As one moves from Design 1 to Design 4, significant reduction in power consumption is obtained, resistances at Y and Z terminal change from tens of giga ohms to hundreds of giga ohms while resistance at X terminal is also increasing from tens of mega ohms to around thousands of mega ohms. This increase in resistance R_x is due to the inverse dependence of resistance on the bias current [19]. Current and voltage bandwidths lie in the range of hundreds of kilohertz which is suitable for biomedical applications. The lengths of transistors have to be non-minimal in subthreshold design to reduce current mismatch. For this reason, lengths of the transistors have been taken five to six times of L_{min}, which ensures that the currents mismatch is within ±10% limit on account of high output resistance.The variation of different performance parameters of CCII with total area of the device for each design is shown in Figures 11-13. It can be deduced from Figure 11 that as the total area increases, voltage and current gains follow same trends of approaching unity.

Table 3W/L ratios of different designs

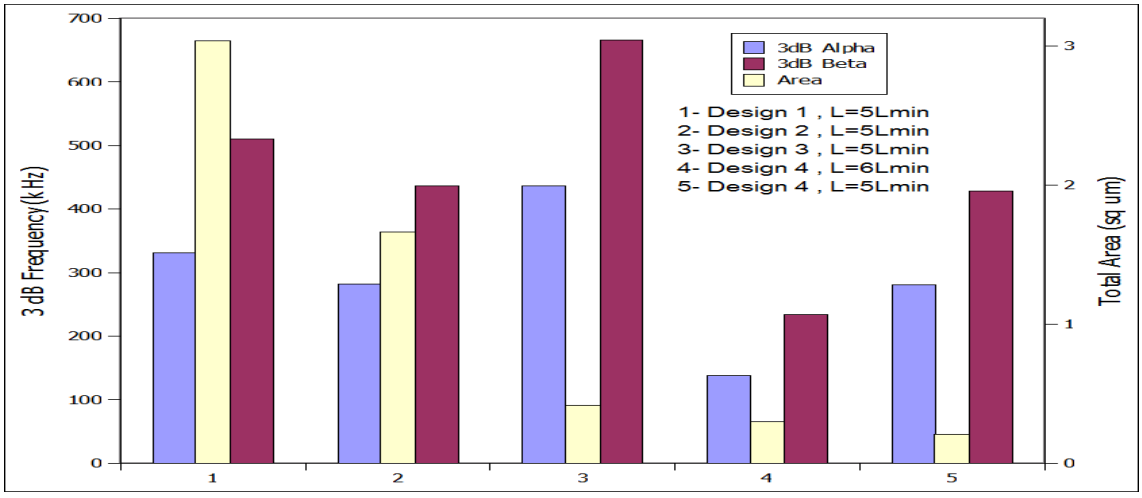
	M1-M2	M3-M4	M5-M9	M10-M13
Design 1	7.5	26.25	5	17.5
Design 2	3	10.5	2	7
Design 3	0.75	2.625	0.5	1.75
Design 4	0.375	1.3125	0.25	0.875

For a particular design (4,5 in Figure 11), if we increase area by increasing the lengths of the transistors, then current and voltage gains come closer to unity. From Figure 12, it is obvious that if area increases for a given design (4, 5 in Figure 12) then voltage and current bandwidths decrease because of the increase in device capacitances. Figure 13 shows that if area reduces then resistances seen by different ports increase. Thus, we can see that for Design 4 having $L=5L_{min}$, the area is minimum. But in this design two transistor's widths come out to be less than $1.5L_{min}$. In order to ensure that the width of each and every transistor is at least $1.5L_{min}$, Design 4 having $L=6L_{min}$ is taken into consideration. It can be operated at 20pA bias current and at even lower supply voltage of ±0.25 V. The power dissipation for this particular design is also minimum and it shows better trade off in performance parameters amongst all the implemented designs, thereby, making it the most optimal design.

Table 4 Performance parameters for different Designs.

		Design 1 $L=5L_{min}$	Design 2 $L=5L_{min}$	Design 3 $L=5L_{min}$	Design 4 $L=5L_{min}$	Design 4 $L=6L_{min}$
1	V_{DD} (V)	±0.3	±0.3	±0.3	±0.3	±0.25
2	I_B (pA)	750	250	100	30	20
3	α	1.0107	1.0106	1.0100	1.0100	1.002
4	β	0.9830	0.9845	0.9812	0.9824	0.9722
5	α-3dB (KHz)	331	282	437	281	138
6	β-3dB (KHz)	510	437	666	428	234
7	R_X (M)	23.63	69.76	182.49	588.22	887.52
8	R_Y (G)	3.096	9.263	21.2232	69.54	72.48
9	R_Z (G)	4.080	7.09	32.5	85.1	113
10	Current deviation	±7.5%	±9.8 %	±5%	±9.66%	±8.9 %
11	Area (μm^2)	3.040	1.664	0.416	0.208	0.299

Figure 11



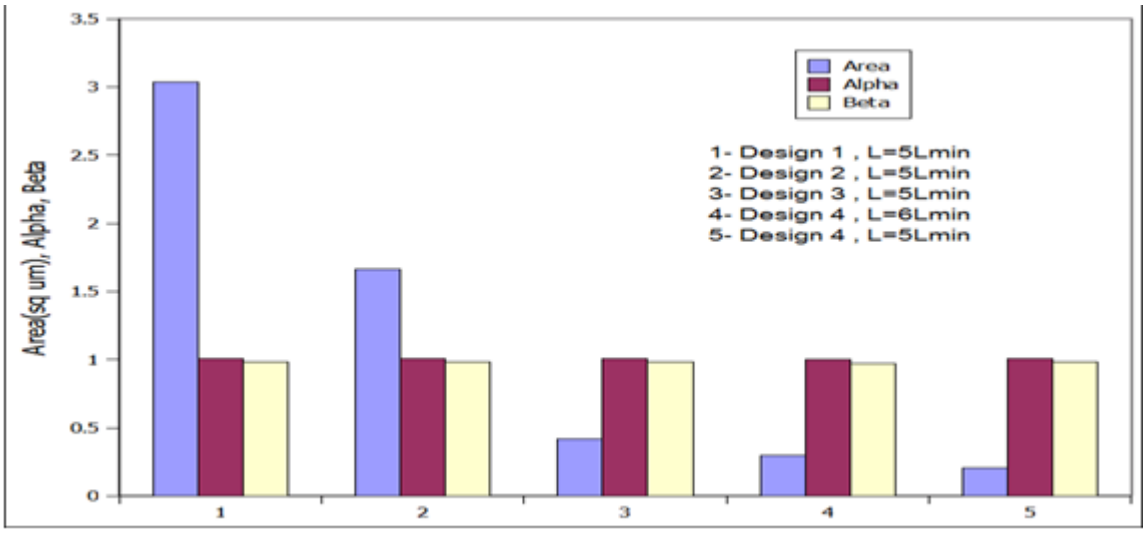


Figure 12

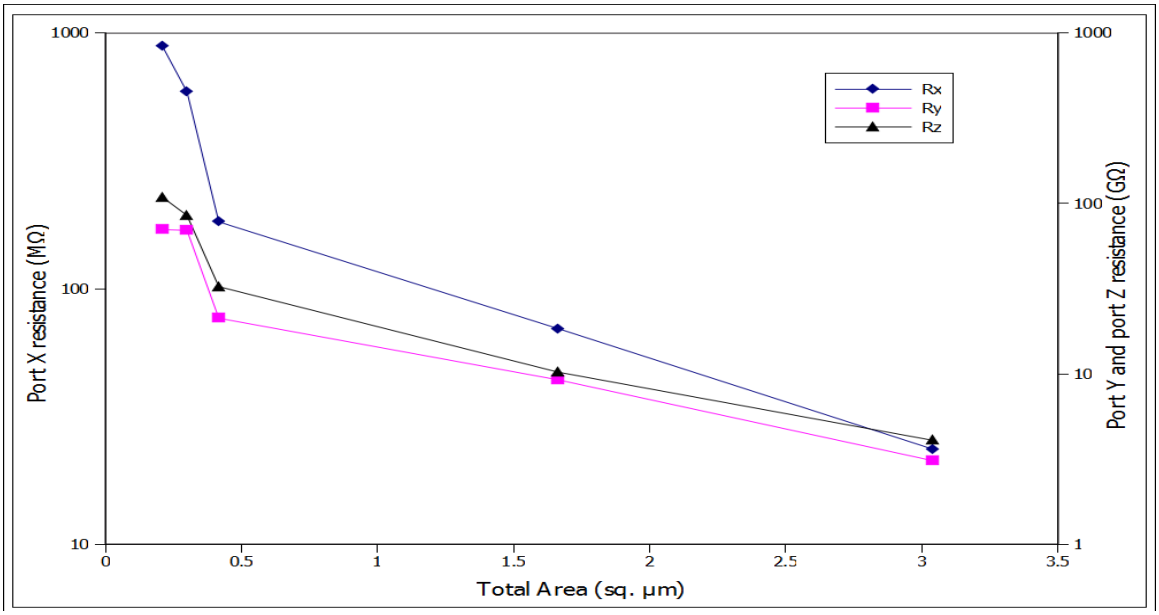


Figure 13

V. VARIABILITY ANALYSIS OF OPTIMAL DESIGN

In order to test the robustness of Design 4 having $L=6L_{min}$, variability analysis is carried out as this has become a metric of equal importance as the challenge is to design reliable circuits with unreliable devices at highly scaled technology node such as 32 nm [15]. Performance parameters (Current gain and voltage gain) of CCII are estimated with MC (Monte Carlo) simulation using 32 nm PTM. The channel length (L) and channel width (W) are assumed to have independent Gaussian distributions with 3σ variation of 10% [17]. Performance metrics in this work are estimated with 2000 sample size [18].

Figures 14-15 show Monte Carlo simulation results of the current and voltage gain. It can be observed from these figures that variations in the current and voltage gains are within acceptable limits (closer to unity with ±10% in variation) in the low frequency range where most of the biomedical systems operate.

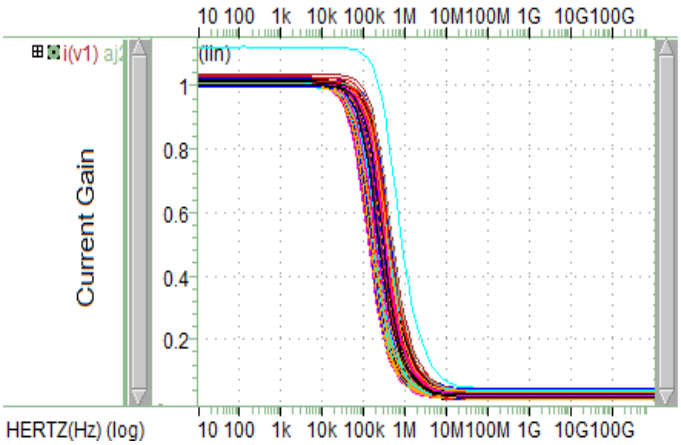


Figure 14 Current gain vs Frequency

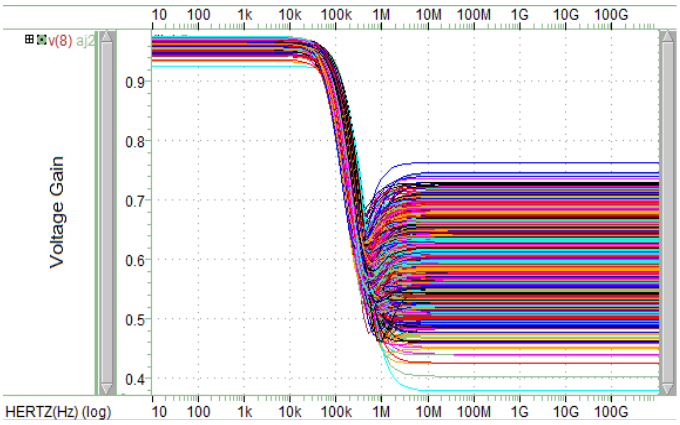


Figure 15 Voltage gain vs Frequency

VI. DESIGN OF INSTRUMENTATION AMPLIFIER BASED ON CCII

To validate the optimal design of CCII (Design 4 having $L=6L_{min}$), an instrumentation amplifier, shown in Figure 16, is simulated using HSPICE [22]. The amplifier is designed for a differential gain of 27 dB. The frequency response is shown in Figure 17. The simulated gain obtained is 24 dB which shows good agreement with the designed value.

VII. CONCLUSION

This paper has successfully presented the various designs of second generation current conveyors (CCII) under subthreshold condition. Various performance parameters have been calculated for various designs by choosing the W/L ratios in such a way so as to preserve the functionality of the CCII device. The design 4 with $L=6L_{min}$, operating at ±0.25V and at a bias current of 20pA, was found tobe optimal and more robust as compared to other designs, thus making it most suitable for ultra low power applications.

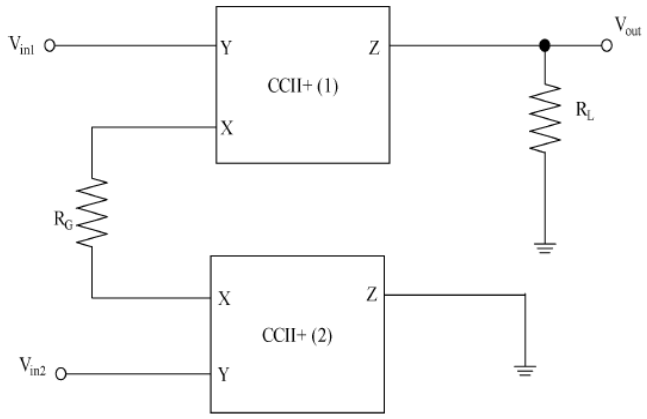


Figure 16 Instrumentation Amplifier based on CCII

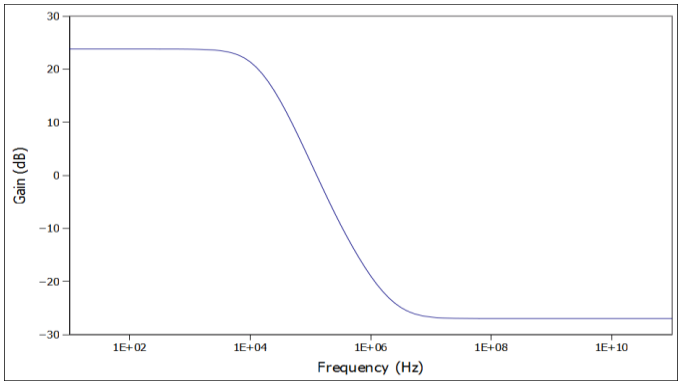


Figure 17 Frequency response of Instrumentation Amplifier

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