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Pulse Triggered Flip Flop Design using Signal Feed Through Scheme for Area and Power Reduction

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Abstract- **In this brief, a low-power flip-flop design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF designs and achieves a better speed and power performance. The simulations are done using Microwind DSCH analysis software tools. Our proposed system simulations are done under 180nm technology and the results are compared with other conventional flip-flops. . Also the simulation of parametric analysis and layout has been done for the proposed D-flip flop and proposed FF design using clock gating. Hence, our proposed system is showing better output than the other flip-flops. By using clock gating concept in proposed flip flop design power consumption has been reduced by 54.01 % and area by 76.23 % on 180 nm technology.**

Index Terms — DSCH, Flip-Flop, low power, Microwind, Pulse triggered

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property [1]. High performance flip flops are key elements in the design of contemporary high-speed integrated circuits. Most of the current designs are synchronous, which implies that flip-flops and latches are concerned in one way or another in the data and control paths [2]. It is significant to save power in these flip-flops and latches without compromising state reliability or performance. Several researchers have worked on low power flip-flop design, but they are mostly focused on one or a few types of flip-flops or applications [3]. The main tradeoffs of any flip-flop are very important for a Power consumption of the clock system increases considerably and clock uncertainties take a significant part of the clock cycle at high frequencies. Non-ideal clock distribution fallout degradation of the clock waveform, power supply noise and crosstalk.In these circuits, high clock frequencies are generally gained by using a fine grain pipeline in which only few logic levels are inserted between pipeline stages [4]. Pulse-triggered FF has been considered a popular alternative to the master–slave based FF on the applications of high-speed operations an explicit-type P-FF, the designs of a pulse generator and latch are separate. Implicit pulse generation is often considered to be more powerful, more efficient than an explicit pulse generation [6]. In an implicit-type P-FF, the pulse generator is a built. In the logic of the latch design and no explicit pulse signals are generated. In an explicit-type PFF, the designs of a pulse generator and latch are separate. Implicit pulse generation is often considered to be more powerful, more efficient than an explicit pulse generation. Designers are striving for the small silicon area, higher speed, low power consumption and reliability due to ever increasing demand and popularity of portable electronics. With the increasing use of mobile devices, consumer electronics markets demand a stringent constraint on reducing the power dissipation. In this paper, we are presenting a new type of implicit P-FF with reduced number of transistors which will reduce the overall power area as well as delay. In the earlier period, the VLSI designers were more bent towards the performance and area of the circuits. Cost and Reliability also gained core importance, whereas power consumption was a peripheral consideration for them. In recent years, however, this has begun to change at a very fast rate and power is being given equal importance in comparison to the area and speed [7]. The main issues in the performance are power dissipation and propagation delay. Power consumption is one of the basic constraints in any integrated circuit. There is always a trade- off between power and performance [8]. In CMOS circuit there are 3 sources of power dissipation, first static power dissipation which relates to the logical states of the circuits and independent of switching activity. The second is short circuit power dissipation when both NMOS and PMOS transistor in the circuit is turned on simultaneously for a short duration of time during switching [9]. Flip-flops are important timing elements in digital circuits which have a great impact on circuit power consumption and speed. In digital electronics, the power-delay product which is also known as switching energy, is FOM (figure of merit) correlated with the energy efficiency of a logic gate. The power delay product is used to evaluate the performance of CMOS process. Logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors [11].

II Conventional FF Designs-

Different conventional FF design techniques used are explained as below:Ep-DCO contains a NAND logic–based generator and semi dynamic true-single–phase –clock structured latch design. The pulse width is determined by the delay of three inverters. This gives rise to large switching power dissipation.

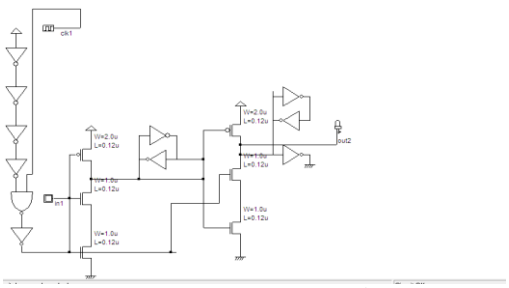

Figure 1: Schematic design of conventional Ep-DCO

Input /output waveform of conventional ep-DCO has been shown below:

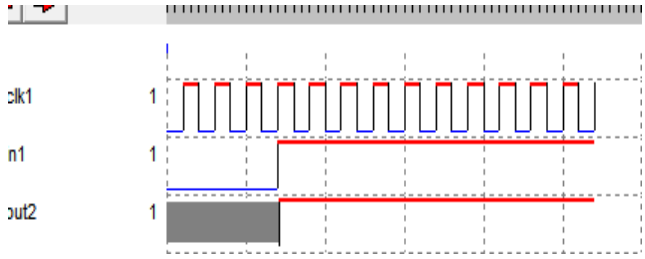

Figure 2: I/O waveform of Ep-DCO

Figure 3 shows a conditional discharged (CD) technique. An extra NMOS transistor controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node is simplified and consists of an inverter plus a pull-up PMOS transistor only.

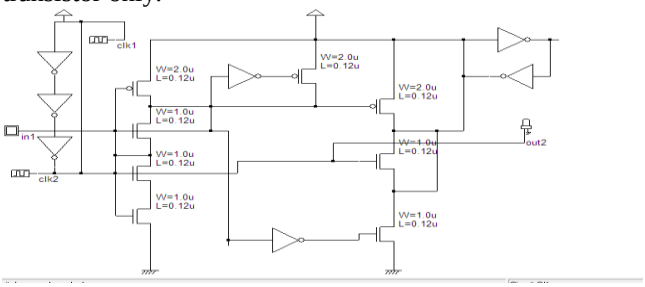

Figure 3: Schematic design of conventional CDFF

Input /output waveform of conventional CDFF has been shown below:

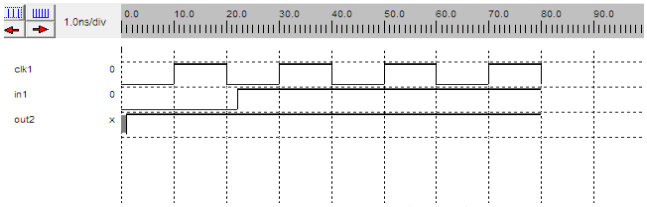

Figure 4: I/O waveform of CDFF

Fig. 3 shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. The node is thus exempted from periodically recharge. It exhibits a longer data to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption [7].

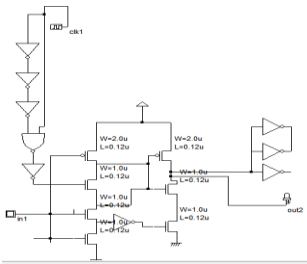

Figure 5: Schematic design of conventional SCDFF

Input /output waveform of conventional SCDFF has been shown below:

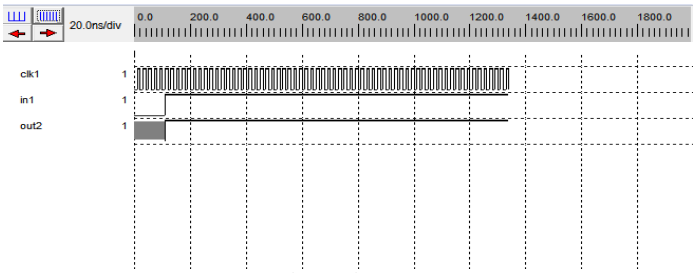

Figure 6:I/O waveform of conventional SCDFF

Figure 7. shows MHLFF also uses a static latch. The keeper logic at the node is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintain the level of nodes.*When* Q equals 0. Despite its circuit simplicity, the MHLFF counts two drawbacks. First, since a node *X* is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further,because a level-degraded clock pulse is applied to the discharging transistor MN3. Second, node *X* becomes floating in certain cases and its value may drift causing extra DC power.

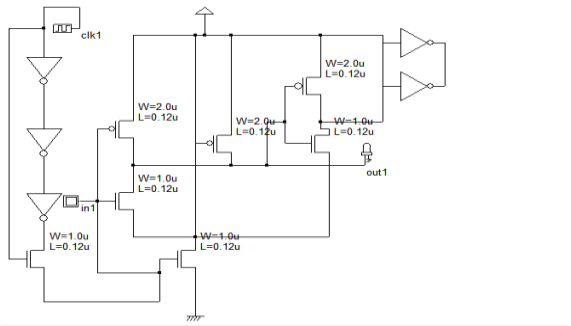

Figure 7: Schematic design of conventional MHFF

Input /output waveform of conventional MHLFF has been shown below:

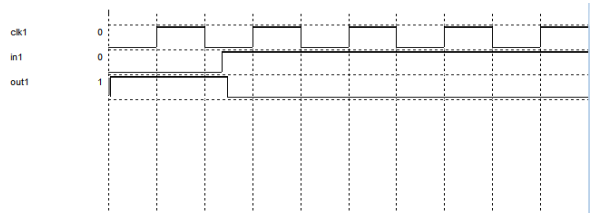

Figure 8: I/O waveform of MHFF

III. PROPOSED SCHEMATIC DESIGN REALIZATION-

Proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. This gives rise to a pseudo-NMOS logic style, design, and the charge keeper circuit for the internal node can be saved.In addition to the circuit simplicity, this approach also reduces the load capacitance of the node. Second, a pass transistor controlled by the pulse clock is included so that input data can drive node Q of the latch directly. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed, pass transistor provides a discharging

path. The principles of FF operations of the proposed design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor which keeps the input stage of the FF from any driving effort. The loading effect of the input source is not significant. In particular, thus discharging does not correspond to the critical path delay.

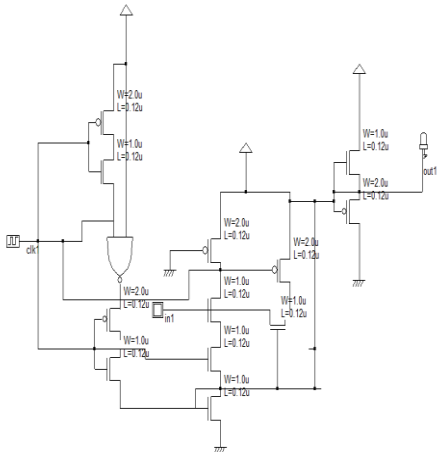

Figure 9:Proposed Design of Conventional D flip flop

Input /output waveform of conventional FF has been shown below:

Figure 10: I/O waveform of Conventional D flip flop

Proposed schematic design, realization of D ff using clock gating with low power consumption has been shown below:

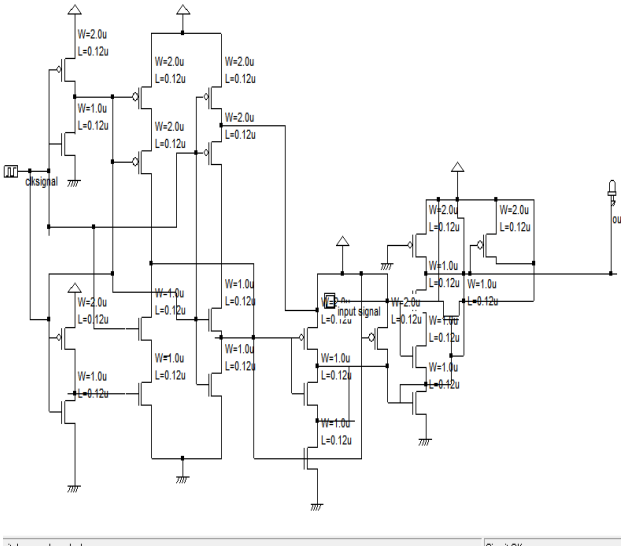

Figure 11: Proposed Design of D flip flop using clock gating

Input /output waveform of conventional FFusing clock gating has been shown below:

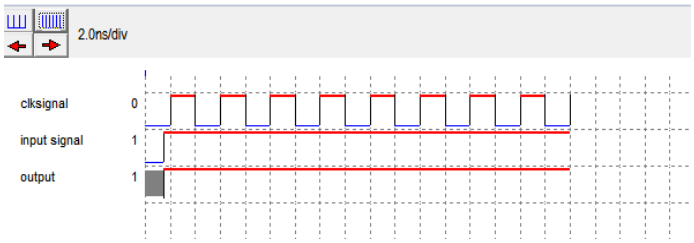

Figure 12: I/O waveform of D flip flop using clock gating

Table I. Comparative Analysis of Proposed D-FF in terms of area and power with other existing design

Parameter	D FF using CMOS [Existing] [1]	Hybrid D-flip flop [Proposed]
Area	285μm^2	213μm^2
Power	0.739μW	0.555μW

The table I show that the reversible D flip-flop designed by using clock gating consumes less area and power as compared to the reversible D flip-flop designed by CMOS.

IV. LAYOUT ANALYSIS

For complex circuits it becomes very complicated to conduct the manual layout so the automatic layout generation approach is preferred. Before the layout simulation, the schematic diagram has been designed in the DSCH design tool. After the schematic diagram the Verilog file is generated with the DSCH design tool. This Verilog file is understandable by the Microwind to construct the layout with exact desired design rules. The other way to create the layout is by PMOS and NMOS devices using cell generator provided by the microwind.

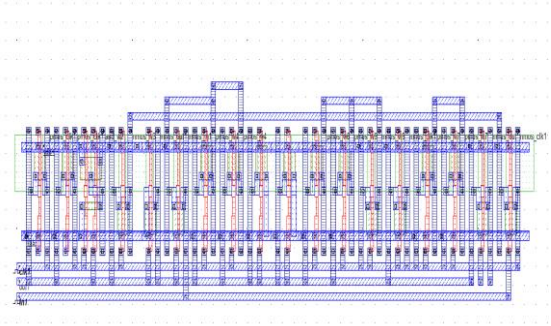

Figure 13: Layout of proposed D-flip flop

The figure 13 shows the layout of hybrid reversible D-flip flop at 180nm technology in Microwind back end design tool.

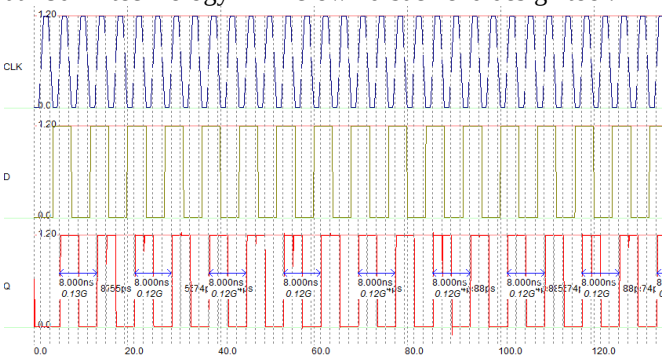

Figure 14: Analog Simulation of proposed D-flip flop

The analog simulation is done Microwind back end design tool. The analog simulation has been carried out to know the power consumption at different temperatures and voltages. Analog simulation is carried out for proposed D-flip flop at 180nm technology.

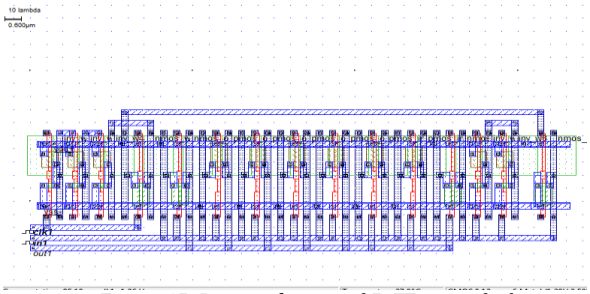

Figure 15: Layout of proposed D FF using clock gating

The figure 15 shows the layout of proposed D FF using clock gating the at 180nm technology. This layout is generated automatically in Microwind back end design tool by using the verilog file which is generated in DSCH design tool.
Analog simulation of proposed D FF using clock gating has been shown in figure 16.

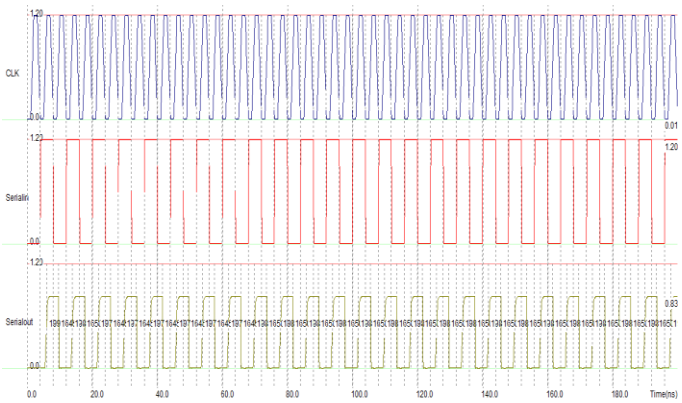

Figure 16: Analog Simulation proposed D FF using clock gating

The analog simulation for the proposed D FF has been carried out to know the power consumption at different temperatures and voltages. Analog simulation is carried out for proposed reversible shift register at 180nm technology.

V. SIMULATION RESULTS

The performance of proposed D FF using clock gating has been carried out in terms of power and area on 180nm technology. Simulation has been performed using Microwind back end design tool. Results are measured in terms of variation in power with respect to the variation in temperature and voltage.

Table III. Power Variation with Supply Voltage

V_{dd}(V)	Power(µW)	
	Proposed D-FF by CMOS [Existing]	Proposed D-FF using clock gating
0	0.469	0.186
0.6	0.01	0.001
1.2	0.158	0.08
1.8	0.254	0.176
2.4	0.329	0.297
3	0.409	0.309
3.6	0.611	0.321
4.2	0.726	0.435
4.8	0.785	0.447

The variation in power with the supply voltage at 180nm is given in the table III. This table shows that the power variation with supply voltage is less in the proposed design as compared to the existing design.

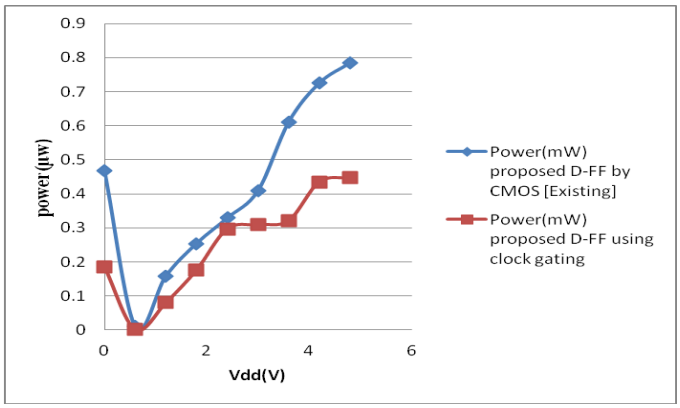

Figure 17: Power Variation with Supply Voltage

The graph in the figure 17 shows the variation in power with supply voltage at 180nm technology. The variation in power with respect to supply voltage is less in the proposed design as compare to the existing design.

Table V. Power Variation with Temperature

t°	Power(µW)	
	Proposed D-FF by CMOS [Existing]	Proposed D-FF using clock gating
20	0.09	0.056
40	0.1	0.057
60	0.101	0.069
80	0.103	0.072
100	0.105	0.085
120	0.110	0.088

The variation in power with the temperature of clock gating D-flip flop at 180nm is given in the table IV. This table shows that the power variation with temperature is less on the proposed design as compared to the existing design.

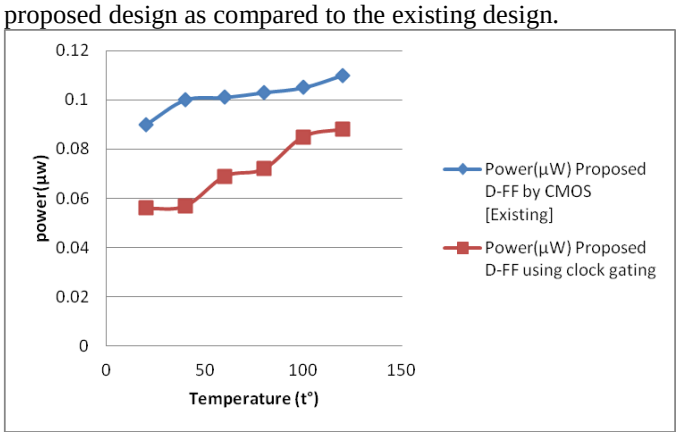

Figure 18: Power Variation with Temperature

The graph in the figure 18 shows the variation in power with the temperature at 180nm technology. The variation in power with respect to temperature is less on the proposed design as compared to the existing design.
Comparison table in term of Power consumption and Area using different techniques has been shown below:

Table IV. Power and Area comparison of different techniques

Various Techniques used	Existing Design [3]				
	Ep-DCO	CDFF	SCDFF	MHFF	Proposed Flip Flop using clock gating
Power (µw)	1.39	0.63	1.75	0.76	0.55
Area (μm^2)	478	321	314	231	213

VII. CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style, consisting of a pass transistor and a pseudo-NMOS logic. The key idea was to provide a signal feed-trough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects. Area and simulation of proposed D Flip Flop shown on 180nm technology. Area of the proposed design is 213µm^{2}on 180nm technology. At 3.6V input supply voltage the proposed SR has shown an improvement of 54.01% in power on 180nm technology.

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