Performance Comparison of Multirate Compressor and Expander in VLSI Platform

[1]Dhurga bai .I, [2]Muthupandi .R
[1]Assitant Professor, [2]P.G. Student of TheniKammavarSangam College of Technology.

***Abstract*—different filters are widely used in multi-rate signal processing as a filter for both compression and expansion process. The objective is to implement compressor and expander using different multi-rate filters with multiplier less structure. So these types of filters utilize limited hardware's and consume less power. The compressor and expander designed and synthesized in QUATRUS II Software with different filter structures and the target is to choose the optimized filter structure for the expansion and compression. The comparison will be made over the performance criteria like area, power, and delay.**

***Index Terms*—Cascaded integrator comb (CIC), down sampling, decimation factor, finite impulse response.**

I. INTRODUCTION

The rapid growth of very large scale Integration (VLSI) unit with the need for FPGA (Field Programmable Gate Array) has been widely applied in the field of digital signal processing, because of its reprogram ability,reconfigure ability, low cost, high logic density and high reliability. Sample rate conversion (SRC) is the process of changing sampling rate of data stream from a specific sampling rate to another sampling rate. With the conversion of communication and software market SRC is a necessary component in many of today's applications, like CDs, Audio players, Multitask Digital audio workstations, Tape recorders, computer communication, WiMAX, WiFi etc.

In most of these applications, very high quality sample rate converter is required. Most high quality SRCs currently available in the market employ adigital filter that provides the required quality by up sampling the data to a very high sampling rate-Followed by down sampling to the required output sampling rate. The digital filters used in the SRC are the strong options for removing noise, shaping spectrum and minimizing Inter Symbol Interference (ISI) in communication system.

The CIC filter is one which is used for larger data rate changes. The use of non-recursive filter structures has been increasing in the recent years for various applications. This is due to the low power consumption and increase in the circuit speed, especially when the decimation factor and the filter order are high. The frequency response of CIC (Cascaded-integrator comb) decimation filter with various techniques has been reported in the past few decades by many researchers.

In 1981, Eugene Hogenauer [1] has proposed a class of digital filter without multipliers for interpolation and decimation and used limited storage elements to have better economical hardwareimplementations. The filter was designated as CIC filter, because it consists of an equal number of integrator sections operating at the high sampling rate and a comb section operating at the low sampling rate as compared to Integrator section.

II. CASCADED INTEGRATOR-COMB FILTER

CIC (cascaded-integrator-comb) filter is widely used as the sample rate change filter due to its simplicity. The CIC filters are multiplier less structures, consisting of only adders and delay elements which is a great advantage when aiming at low power consumption. These filters are frequently used in digital down and up converters. The Direct implementation of CIC decimation filter is shown in Fig.1.

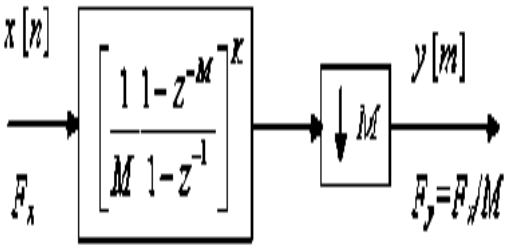

Fig.1.Direct Implementation Structure of CIC filters.

In direct implementation of CIC decimation filter structure the whole circuit is operate at maximum sampling frequency *Fx*before decimation takes place. Hence the power consumption of direct implementation CIC decimation filter is very high. So in this paper, we present a different representation of the CIC filter structure for decimation. The transfer function of the cascaded-comb decimation filter shown in Fig.1 is given by,

$$H(z)=\left[\frac{1}{M}\frac{1-z^{-M}}{1-z^{-1}}\right]^{K} \quad (1)$$

A. Decimation Filters

Multi-rate DSP is the process of converting data sampled at one rate (Fs1) to data sampledat another rate (Fs2). If Fs1 > Fs2, the process is called decimation. The function of a decimator is to take data that was sampled at one rate and change it to new data sampled at a lower rate. The data must be modified in such a way that when it is sampled at the lower rate the original signal is preserved. A pictorial representation of the decimation process is shown in below Fig.2.

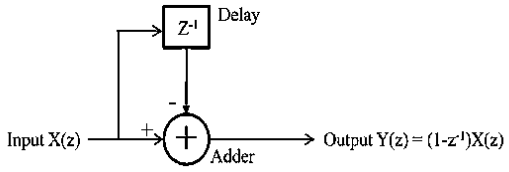

Fig.2. A Basic Decimator

The decimator has two parts. An input section that samples at a rate of Fs and an outputsection that samples at a rate of (1/m) Fs, where *m* is a positive integer greater than 1. The structure of the basic decimator indicates that for every *m* input samples there will be 1 output sample. Let us explain the frequency domain view of the decimation.

B. Interpolation Filters

An integrator is a single-pole IIR filter with a unity feedback coefficient which also acts as an accumulator. The transfer function for an integrator on the z-plane is shown in equation2 [3].

$$H_{integrator} = \frac{1}{1-Z^{-1}} \quad (2)$$

The time domain representation of equation (2) is shown in equation (3). From equation (3), it can be seen that the function of the integrator is to add the present input to the past output.

$$y[n] = y[n-1] + x[n] \quad (3)$$

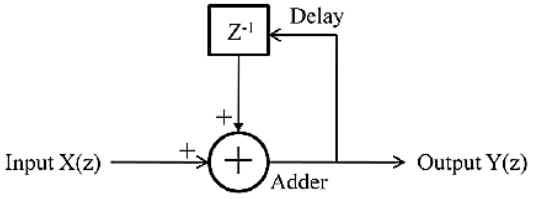

Fig.3. A Basic Interpolator

C. CIC Decimation Filters

Downsampling by a factor R is a process where every R^{th}sample is retained while the R-1 samples in between are discarded. The output sample rate hence decreases by a factor of R. Decimation is a process where anti-aliasing filtering precedes the downsampling process. The CIC decimator is obtained by interchanging the order of the comb and the integrator sections in the CIC filter structure, such that the comb section comes first, followed by the downsampler. Interchanging the comb and integrator section does not affect the functioning of the filter as it is linear. Fig.4. depicts the CIC decimator structure.

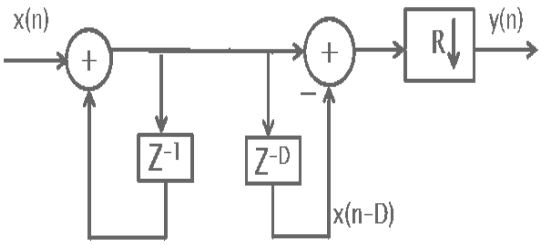

Fig.4.CIC Decimator

In CIC filters, interchanging the order of the comb section andthe integrator section does not affect the functionality of the filter as it is linear. However placing the comb section on that side of the filter which is operating at a lower sample rate reduces the memory requirements in the delay. The new differential delay of the comb section is then reduced to N=D/R .The new comb section now functions at a lower clock frequency.This implementation is depicted in Fig.5.

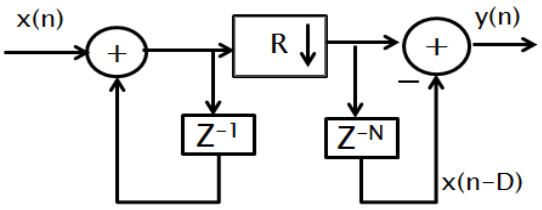

Fig.5.Single Stage CIC Decimator

This decimation filter can be realized using a cascade of log2*M* FIR filter. This structure shown in Fig.5.is called as 'non-recursive structure' because there are only FIR filters needed for implementation. So there is no stability related issues in non-recursive structure. Reducing sampling rate in the earlier stages helps to reduce the power consumption. For an M stage CIC decimator the DC gain is given by(NR) M and for an M stage interpolator it is (NR) M / R. Hence bit growth process occurs at the output. The output bit width should be large enough in order to accommodate the bit growth occurring in the internal stages. The bit width of the output data of a CIC decimator is

$$Bmax = Bin + \log2\ (RN)\ M \qquad (4)$$

Where Bin is the bit width of the input data.

An efficient implementation technique for CIC decimator to reduce bit growth is the non-recursive decimator. [2] Bit growth occurs due to the presence of integrators. The transfer function of a recursive CIC decimator is

$$H\ (z) = [(1\text{-}z\text{-}R) / (1\text{-}z\text{-}1)]^{L} \qquad (5)$$

where R is the down sampling rate and L is the number ofstages. The differential delay(D) is one. The transfer function can be expressed as:

$$H\ (z) = (1+ z^{-1} + z^{-2} + \ldots. z^{-R+1})^{L} \qquad (6)$$

If the downsampling rate R can be expressed as a power of 2,then by means of polynomial factoring the above expression can be factored as:

$$H\ (z) = (1+ z^{-1})^{L}\ (1+ z^{-2})^{L}\ (1+ z^{-4})^{L}. \ldots (1+ z^{2^{J-1}})^{L} \qquad (7)$$

The advantage of the non-recursive decimator is that theintegrator section is removed and this reduces the bit growth phenomenon occurring at the intermediate stages of the filter. In this structure, bit growth occurs at the rate of only L bits per stage.

D. CIC Interpolation Filter

Upsampling by a factor R is the process of inserting R-1 zero valued samples between original samples in order to increase the sampling rate. The output sample rate increases by a factor R. Upsampling by R adds to the original signal R-1 undesired spectral images which are centred at multiples of the original sampling rate. CIC filters are used as anti-imaging filters for interpolated signals in order to remove the unwanted spectral images. The comb section precedes the integrator in a CIC interpolator fig.6 depicts the CIC interpolator structure.

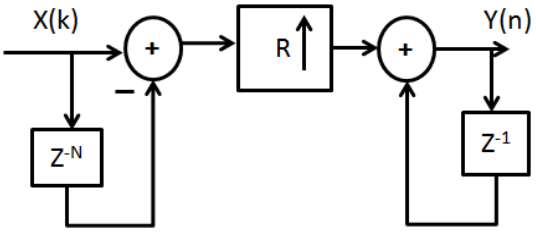

Fig.6.Single Stage CICInterpolator

E. N Stage CIC Decimation and Interpolation Filter

The transfer function of the cascaded comb decimation filter given in equation (8) can be rewritten in simplified form as,

$$H(Z) = \prod_{i=0}^{\log_2 M-1}(1 + Z^{-2^i})^{K} \qquad (8)$$

This decimation filter can be realized using a cascade of log2*M* FIR filter. Structure shown in fig.7 is called as 'non-recursive structure' because there are only FIR filters needed for implementation. So there is no stability related issues in non-recursive structure. Reducing sampling rate in the earlier stages helps to reduce the power consumption. For an M stage CIC decimator the DC gain is given by (NR) M and for an M stage interpolator it is (NR) M / R. Hence bit growth process occurs at the output. The output bit width should be large enough in order to accommodate the bit growth occurring in the internal stages. The bit width of the output data of a CIC decimator is

$$Bmax = Bin + \log_2\ (RN)\ M \qquad (9)$$

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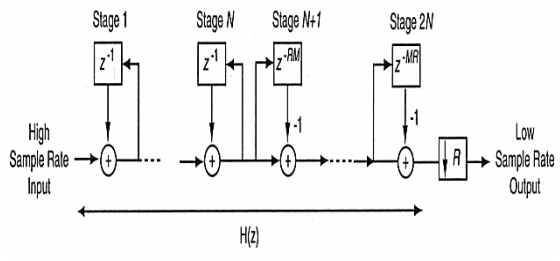

Fig.7.N[th] Stage CICDecimator

The integrator section of CIC filters consists of N ideal digital integrator stages operating at the high sampling rate fs. Each stage is implemented as a one-pole filter with a unity feedback coefficient. The comb section operates at the low sampling rates fs/M, where M is the integer rate change factor. This section consists of *N* comb stages with a differential delay of *D* samples per stage.

The differential delay is a filter design parameter used to control the filter's frequency response. In practice, the differential delay is usually held to *D*= 1 or 2. The system function for a single comb stage referenced to the high sampling rate. There is a rate change switch between the two filter sections.comb stage referenced to the high sampling rate. There is a rate change switch between the two filter sections.

For decimation, the switch sub samples the output of the last integrator stage, reducing the sampling rate from *f*sto *fs/M.* and for interpolation, the switch causes a rate increase by a factor of M by inserting *M - 1* zero valued samples between consecutive samples of the comb section output.The system function for the composite CIC filter referenced to the high sampling rate fs.It is implicit from the last form of the system function that the CIC filter is functionally equivalent to a cascade of N uniform FIR filter stages.

A conventional implementation consists of a cascade of *N* stages each requiring MD storage registers and one accumulator. Taking advantage of the rate change factor, one of the *N* stages can be simplified to use only *D* storage registers.

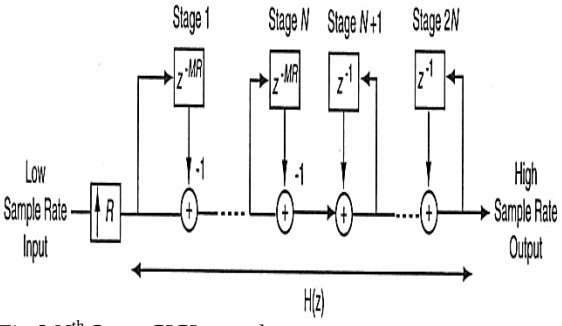

Fig.8.N[th] Stage CICInterpolator

III. POLYPHASE CIC INTERPOLATION AND DECIMATION STRUCTURES

This is a three-step process. First, *M* signals are formed from *h*(*n*), where *h*(*n*) is a sum of *M* partial signals,

$$h_i = h(nM + i) \quad (10)$$

Second, the *hi*(*n*) are upsampled by *M*, i.e.,

$$h_i^M(n) = \begin{cases} h_i\left(\frac{n}{m}\right) & , \ for\ n = 0, \pm L, \dots \dots \\ 0 & , \ otherwise \end{cases} \quad (11)$$

Third, summing all the shifted version is

$$h(n) = \sum_{i=0}^{M-1} Z^{-i} H_i(Z^m) \quad (12)$$

The noble identities allows to move the order of upsampling/downsampling and filtering [7]. Combination of the polyphase representation and noble identities gives the efficient realization of multirate structures. For example with *M*=2, the polyphase representation of *H*(*z*) is derived from equation (12) as

$$H(Z) = H_0(Z^2) + Z^{-1}H_1(Z^2) \quad (13)$$

From the above equation, *H*(*z*) is an addition of two sub filters and a delay. Using the noble identities, the upsampler is moved forward. In reality the polyphase interpolator, where a device called commutator is used instead of summation at the output.

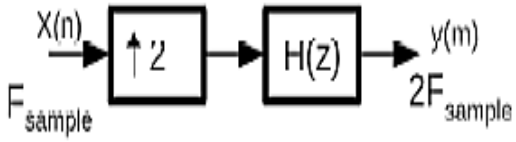

Fig.9.Interpolation by 2

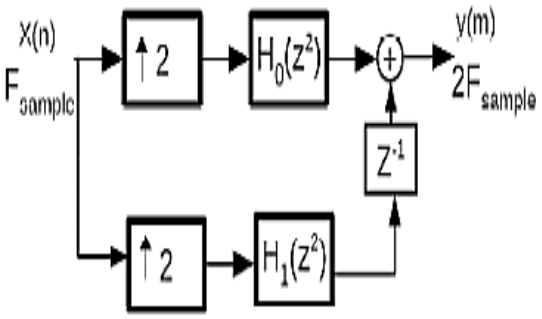

Fig.10.Polyphase CIC Interpolator for M=2

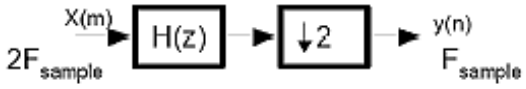

Fig.11.Decimation by 2

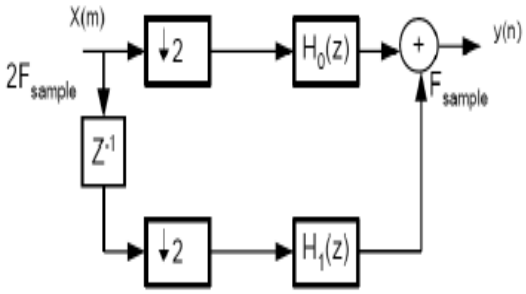

Fig.12.Polyphase CIC Decimator for M=2

At each time instant, the inputs of the summation has only one non-zero sample, so the output can be taken alternatively, beginning from the upper branch. A decimator is derived from the interpolator by reversing the signal-flow graph and replacing theupsampler by a downsampler [8].

IV. EXPERIMENTAL RESULTS

Quartus II development software provides a complete design environment for System on a Programmable Chip (SOPC) design. Quartus II offers easy design entry (using schematics, block diagrams, AHDL, VHDL, Verilog and System Verilog), powerful logic synthesis, functional and timing simulation, device programming and verification. The QUARTUS II Simulation Software used to perform both CIC and Polyphase Decimation, interpolation filters (in chapter 3) and find out utilize limited hardware's, delay and power consumption.Decimation is a process where anti-aliasing filtering precedes the down sampling process. The CIC decimator is obtained by interchanging the order of the comb and the integrator sections in the CIC filter structure, such that the comb section comes first, followed by the down sampler. The advantage of the non-recursive decimator is that the integrator section is removed and this reduces the bit growth phenomenon occurring at the intermediate stages of the filter. In this structure, bit growth occurs at the rate of only L bits per stage. The integrator stage and the differentiator stage operate at different frequency.

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Comparison of Performance over the device utilization summary, power dissipation, and delay for CIC Decimation Versus Polyphase CIC Decimation with stage N, Decimation Rate factor R=8, Differential Delay M=1Comparison of Performance over the device utilization summary, power dissipation, and delay for CIC Interpolation Versus Polyphase CIC Interpolation with stage N, Decimation Rate factor R=3, Differential Delay M=1

Table1. Performance Comparison of CIC versus Polyphase CIC Decimation Filters

Device utilization	CIC Decimator R=8, M=1			Polyphase CIC Decimator R=8, M=1		
	1	2	3	1	2	3
Total logic element	77	130	195	77	130	195
Total comb. Function	42	92	154	42	92	154
Total register	77	130	195	77	130	195
No.of Add & sub	2	4	6	2	4	6
Counters	1	1	1	1	1	1
I/O pins	39	42	45	39	42	45
Power Dissipation (mW)	2.69	3.28	4.18	0.97	2.09	2.79
Delay (ns)	6.97	8.384	11.30	4.34	4.90	5.54

Table2. Performance Comparison of CIC versus Polyphase CIC Interpolation Filters

Device utilization	CIC Interpolator R=3, M=1			Modified CIC interpolator R=3, M=1		
	1	2	3	1	2	3
Total logic element	99	139	183	99	139	183
Total comb. Function	51	89	137	51	89	137
Total register	66	14	146	66	14	146
No.of Add & sub	2	4	6	2	4	6
Counters	1	1	1	1	1	1
I/O pins	36	38	40	36	38	40
Power Dissi. (mW)	2.5	2.93	3.27	1.4	1.67	2.34
Delay (ns)	9.421	12.255	15.089	5.89	6.02	7.564

CONCULSION

The CIC Filter structures are implemented with the help of Altera Quartus II Software considering decimation factor 8 and interpolation factor is 3 the results are obtained. The performance of the filter with two structures was compared. The result shows that each CIC filter structure has some advantages and disadvantages. Both structures utilize same device utilization, polyphase CIC structure consumes less power compared to other structures. Comparing two CIC filter structures, the polyphase CIC structure consumes less power and utilizes less device utilization. Further to increase performance by means of Compensation CIC decimation and interpolation filters.

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