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Operating The Sram Cell Architecture With The High Efficient And Reduced Memory Size

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Abstract -- In emerging embedded applications such as wireless sensor network, the key metric is minimizing energy dissipation rather than processor speeds. Minimum energy analysis of CMOS circuits estimate the optimal operating point of clock frequency, supply voltages, and threshold voltages. The minimum energy analysis shows that the optimal power supplies typically occur in sub threshold. New SRAM architecture is developed for the high efficient and reduced memory size structure that to be operate in the low power supply, improved throughput, reduced memory size, reduced leakage power and high performance. This be done in a Cadence Virtuoso tool of 180nm gpdk library function. A marginal bitline leakage compensation compensates for the bitline leakage current also reduced in this technique which becomes comparable to a read current at subthreshold supply voltages.

Index Terms—CMOS digital integrated circuits, CMOS memory circuits, coprocessors, design methodology, digital signal processors, leakage currents, logic design, subthreshold CMOS circuits.

I. INTRODUCTION

Embedded static random-access memories (SRAMs) dominate the power consumption, area, performance, and yield of emerging portable electronic devices. These devices require low energy consumption to allow long operational lifetimes as they are often battery powered. The design of subthreshold SRAMs is popularly utilized because lowering the supply voltage can quadratically reduce the energy consumption [1]. However, as the supply voltage is below the transistor threshold voltage, the variability of SRAM increases severely in design and process parameters regarding proper ratio of device strengths [2]. Major sub threshold SRAM stability issues include process-induced device variation ecreasing ION−IOFF ratio and threshold voltage random variation (σV T) [3]. The standard 6T bit cell fails to perform reliable weak-inversion operations because of read-current-disturbance-induced static noise margin (SNM) degradation. Various more-than-6T bit cells were presented to address the read reliability issue, such as 8T bit cells [4], [5]. They added two transistors as the read buffer to isolate the storage node from the bitline, resulting in better read stability.

The soft-error problem becomes more critical for ultralow voltage SRAMs than super threshold SRAMs because the critical charge in storage node is much less. As reported in [6], the soft-error rate increases by 18% for every 10% supply voltage reduction. In order to enhance subthreshold SRAMs' soft-error immunity, the bit-interleaving scheme is always preferred. It can spatially separate bits of a word in the row, and only simple single-bit error correction coding is needed. However, the read buffered 8T bit cell designed with the bit-interleaving scheme suffered from write-half-select disturbance. To solve the issue, an array architecture and circuits with 12% area overhead, compared to 8T SRAM design, were presented in [7]. The array architecture addressed the half-select problem by decoupling large bitline capacitance from half-selected cells. In [8], a fully differential 10T bit cell was presented for high read stability. Meanwhile, it can be designed with bit-interleaving scheme by vertical and horizontal wordlines. It required boosted wordline technique to maintain robust write operation. Recently, a fully differential 8T SRAM with a column-based dynamic supply scheme was presented in [9].

By utilizing different cell supply voltages for basic modes, it successfully separated the read/write/standby operations to allow it to be bit interleaved. In this brief, we propose a 9T bit cell with enhanced write ability by inserting a pass transistor into the cross-coupled inverter pair. To allow the bit-interleaving array scheme for 9T bit cells, two additional write wordlines (WWL/WWLb) are used. Some preliminary results were first presented in [10]. Advanced iso-area SRAM stability analysis and fabricated test chip experimental results are proposed in this work. The remainder of this brief is organized as follows: Section IIdescribes the basic operations and layout considerations of our 9T bit cell. Advanced iso-area SRAM Vmin analysis is discussed in Section III. Section IV shows the implementation of a 1-kb 9T SRAM with the bit-interleaving array scheme and the measurement results. The final section concludes this work.

II. RELATED WORK

A. Wang and A. Chandrakasan [5] have proposed, a new sub threshold logic and memory design methodologies are developed and demonstrated on a Fast Fourier transform processor. The FFT processor uses an energy-aware architecture that allows for variable FFT length (128-1024 point), variable bit-

precision (8b and 16b) and was designed to investigate the estimated minimum energy point. The FFT processor is fabricated using a standard 0.18µm CMOS logic process and operates down to 180mV.

B.H. Calhoun and A.Chandrakasan [6]. Have proposed a paper that overcomes the limits of low-voltage operation of traditional six-transistor. They propose an alternative bitcell that functions at much lower voltages. The measurements confirm that a 256-kb 65-nm SRAM test chip using the bitcell operates into sub threshold to below 400mV. At this low voltage, the memory offers substantial power and energy savings at the cost of speed, and makes it well-suited to energy-constrained applications.

L.Chang, D.M.Fried, J.Hergenrother, J.W.Sleight, R.H.Dennard, R.K.Montoye, L.Sekaric, S.J.McNab, and A.W.Topol [7] have proposed to analyze the read stability N-curve metrics and compares them with the commonly used static noise margin (SNM). The new write ability metrics derived from the N-curve are compared with the traditional write-trip point definition. Finally, these metrics are used to investigate the impact of the intra-die variability on the stability of the cell by using a statistically-aware circuit optimization approach and the results were compared with the worst-case or corner-based design.

M.E.Sinangil, N.Verma and A.P.Chandrakasan [10].have proposed the highly energy constrained applications, such as wireless sensor nodes and biomedical implants, preferentially operate at low voltage levels and at low frequencies to be close to the minimum energy point

SRAM that is designed for both sub-V_t and above-V_t operation. The design is operational from 250mV which is in deep sub-V_t region to 1.2V which is the nominal-V_{DD} for the process.

III. Objectives & Overview Of The Proposed Mechanism

A. Objectives

Ultra low voltage and low power SRAM design is critical in embedded systems such as biomedical implants, self-powered wireless sensors, and energy harvesting devices, in which battery life or input power is of main concern . The aim of the proposed work is to reduce the power consumption by operating the SRAM in sub/near-threshold region, by which it is possible to reach the minimum energy point, which substantially reduces the power consumption. Leakage compensation using the replica bitline, additional transistors to make the leakage independent of data, virtual ground and negative wordline voltage are the techniques proposed to combat the effect of data dependent leakage at the cost of more area and/or power than that of the existing systems as presented with Cadence Virtuoso tool.

- The structure that is to be operated in the low power supply.
- Improved throughput.
- Reduced memory size.
- Reduced leakage power.
- High performance.

B. Overview of the proposed Mechanism

SRAM dominate the power consumption, area, performance, and yield of emerging portable electronic devices.With the increased demand of the on-chip memory in the wireless implantable/wearable biomedical sensors. These types of applications have medium to low speed requirements, while the budget for the power is very tight. In the sub/near-threshold regime, the conventional six-transistor SRAM shows poor functionality, especially on read stability, writes ability, and half-selected cells. Techniques and methods have been proposed to address these three issues in the past. To address issues related to read stability, decoupling read port from write has been introduced to separate read and write paths, which allows each operation to be optimized individually at the cost of additional transistors, such as 8T, 9T, and 10T cells. Apart from the read decoupling technique, other methods have been reported recently such as upsizing standard 6T, DTMOS cell, dynamic read decoupling, and Schmitt-Trigger-based cell. As most of the conventional read decoupling techniques use single-ended read schemes, the detection threshold varies considerably due to the leakage. For example, in an 8T cell, the leakage of each cell depends on the data stored in the cell. This dependency causes voltage variation on the read bitline, i.e., the read bitline level changes with the number of cells storing data 0 or 1 on the same bitline. Such variation makes the detection more challenging.

IV. Proposed System

A. Two-level cache memory architecture

Fig. 1 shows the block diagram of the 0.8-V 128-kb four-way set-associative two-level CMOS cache memory. As shown in the figure, in order to implement the two-stage /BLOTC tag-compare scheme in L2 with an 8-T TC and a 10-T SLS memory cell with the G/F data sense amp structure, this cache memory is designed to have the memory portions, the tag portions, the tag and the data sense amps, the predecoder, and the multiplexers in two levels with 22-bit index data, 8-bit address, 8-bit write data, and 8-bit data out. The two-level hierarchical approach has been adopted in this cache memory. Level 1 is associated with the five bits of the 8-bit input address and Level 2 is referred to all eight bits of the input address. Therefore, the size of the

tag-cell array and the memory-cell array in L1 is smaller. In each level, there are four memory portions and four tag portions. In L1, each tag portion has 128* 22 TCs and 128 *32 memory cells. In L2, each tag portion contains 22 *256 TCs and 128* 256 memory cells. By adopting the two-level BLOTC/ scheme, this proposed cache memory has a reduced power consumption.

B. Tag Portion

Fig. 2 shows the schematic of each of the four tag portionsin this 0.8-V 128-kb four-way set-associative two-level CMOScache memory. As shown in the figure, in the tag portion, thereare two groups, Level 1 and Level 2. In Level 1, in each tagportion 22 32 11-T TCs with the structure havebeen used. In Level 2, both structures have been adopted to organize each tag portion of 22 256 8-TTCs. For each column of 22 TCs, all the tag sense wordlines are vertically connected to an SWL tag sense ampat top. For each row of 256 TCs, all the SBLs are horizontallyconnected to an SBL tag sense amp at right. In Level 1, the tag-compare scheme as described in [5] and [6] havebeen adopted. In each L1 TC column, there is a tag write wordline - , a tag read wordline - , and a tag sense wordline - connected vertically to the tag sense amp. In L1, there are 32 tag senseamps in total.

As for Level 2, in order to reduce power consumption, increase speed performance, and save layout area,the two-stage /BLOTC tag-compare scheme based onthe index data has been used. In each L2 TC column, a tag read wordline - , a tag write wordline and a tag sense wordline - are connected verticallyto a tag sense amp. In L2, there are 256 tag sense amps in total. During the TC access procedure, in aspecific TC column selected by the 8-bit input data address,the TCs with their respective index data bits of logic-0 areconnected to the tag sense amp at top via SWL duringthe sending period. After the sensing period of the tag sense amp, if there is a TSWL-related hit signalfor this column, the follow-up BLOTC tag sensing will beinitiated. The remaining TCs in that specific column with theirrespective index data bits of logic-1 are connected to the SBLtag sense amps via the horizontal SBL for further sensing.

If a further SBL-related hit signal can be obtained, a hit signal isgenerated to trigger the readout of the data from the specifiedmemory cell.In order to facilitate the two-level two-stage/BLOTC tag-compare scheme in L2 and tag-compare scheme in L1, innovative designs of L1/L2 TCsare used in the tag portion. These L1/L2 tag-portion-relatedcircuits, including the second-level decoder and the tag senseamp. In order to implement the scheme, Fig. 3 shows an innovative 11-T TC circuit usedin L1, which is derived from a 10-T TC circuit as shown inFig.3. In this 11-T TC, the SRAM cell portion is similarto that of the 10-T one. Unlike in the 10-T one, in this 10-TTC, only one pair of bitlines are used in both the SRAM celland the tag-compare portions. (Note that in the 10-T one, both write and read bit lines (W-BL/R-BL) are adopted.) Similarto the 10-T one, for the SRAM cell portion, a write wordline(W-WL) controls a pair of bitlines connected to the internalstorage nodes. In the tag-compare portion, instead of four nMOS devices connected between the sense wordline as in the 10-T one, three nMOS and two pMOS devices (MP2–4,MN4–5) have been used to determine the logic state of the L1TSWL. When the tag read wordline - is high, MN4is on and the MN5 is off. The tag sense wordline– is disconnected from this TC and maintains its precharged high state. When the tag read wordline - is low, MP4 ison. Under this situation, whether or not the tag sense wordline- is pulled low depends on the internal storage data(BIT) and the bitline. If the internal storage data is different from the bitline, then either MP2or MP3 is on (MP2 is on). Therefore, PS4 is high and theL1-TSWL is pulled low, indicating a miss. If the BIT is the same as the bitline, then both MP2 and MP3 are off and MN5 isoff. Thus, the L1-TSWL stays precharged high, indicating a hit.The adoption of three pMOS devices and two nMOS devices in the tag-compare portion of the 11-T TC instead of four nMOSdevices as in the 10-T one, provides advantages.

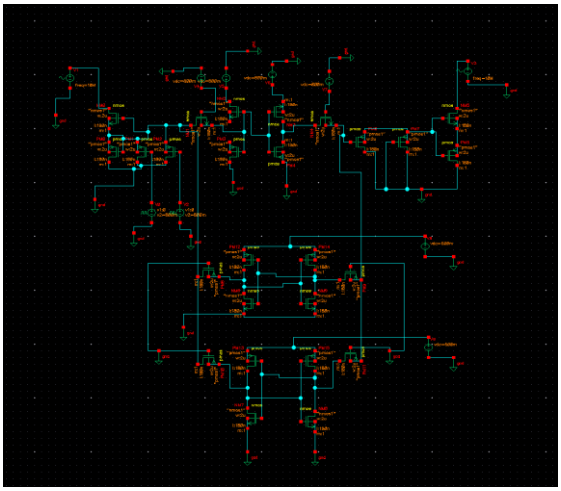

Figure 1. Schematic of SRAM cell structure

C. 8T-SRAM cell design

The 8T cell used in this work is shown in Fig. 1(b), in which atwo-transistor read stack is added to a conventional 6T cell. Theoriginal 6T word line is used exclusively for write operationswhile a second read word line is tied to the read stack. With thisconfiguration, cell disturbs during a read access are effectivelyeliminated. Depending on the impact of variability, the additional twotransistors in an 8T cell could lead to an increase in cell area overconventional 6T cells. The cell schematic, however, enables acompact layout (Fig. 2(b)) that can be placed into an array ina similar manner to 6T cells. Like the word line

in a 6T cell,the read and write word lines (RWL and WWL) in an 8T cellcan run horizontally across the cell width. The additional wordline increases metal density, which could increase wire delay orenhance capacitive coupling between adjacent word lines; however,both can be controlled with proper design.

The cell aspectratio maintains a short read bit line length in the vertical direction.In a 65 nm node technology at constant read current, thepenalty over a dense 6T cell (as might be used for higher levelcaches) is approximately 30% while a comparison with a highperformance 6T cell (as might be used for lower level caches)yields a penalty closer to 20%. A key reason for this differenceis that 6T cells require that both halves of the cell be enlarged toimprove cell read performance while 8T cells only need a sizeincrease in a single read stack. This cell size penalty over 6T canbe expected to reduce or disappear completely with technologyand voltage scaling. For the high-performance applications targeted in this work, the fabricated 8T cell size in 65 nm hardwareis 0.9 m . No additional process steps (implant masks, gate oxides,etc.) on top of a standard flow were used to build this cell.In an 8T cell, a read operation does not affect the contents ofthe cell. The worst-case static noise margin [9] is simply that for two cross-coupled inverters (Fig. 3). For a 6T cell, however, theworst-case static noise margin occurs in the read condition. Inthis case, the pass-gate disturbs the "0" storage node by pullingit up above ground, which significantly degrades the static noisemargin (Fig. 3). Even if the cell ratio for a 6T cell is increased[5] (thus trading off cell area to match that of the 8T), the 8T stillprovides a considerably improved static noise margin (Fig. 4),which significantly improves cell yield. Usage of the 8T cell is thus a more effective way to improve cell stability than simplygrowing a conventional 6T cell.Without read disturb concerns, there is no limit to the minimumratio in an 8T cell. To improve cell write margins andreduce cell area, it is desirable to minimize the width of the pull-down nFET.

While this increases variation, a write marginimprovement will generally be observed. Further write marginenhancement can be achieved by strengthening the pass-gate devices—either by lowering, reducing gate length, increasingdevice width, or expanding WWL voltage swing. Since thesetechniques do not affect stability, 8T cells can simultaneouslyimprove both stability and write ability yields. These techniquesmay, however, come at the cost of cell leakage (Fig. 5).Depending on the balance between gate and subthreshold leakage current levels, migration from a 6T cell to an 8T cellat the same supply voltage may increase cell leakage somewhatas pass-gate leakage and the two additional read stack transistorsoffset the minimum-width, high- pull-down nFETs and pull-up pFETs. On the other hand, this may be an issue sincevoltage scaling is enabled by 8T-SRAM, which reduces leakagecurrents. It should also be noted that due to asymmetry in the cellread stack, cell leakage is data-dependent.Read performance in an 8T cell is determined by the strengthof the two-transistor read stack. Due to layout restrictions, thetop read transistor is generally of smaller width, and thus likelylimits read current. Cell write performance will largely be determined by the pass-gate device strength, but may also be affectedsomewhat by asymmetric loading of the storage nodesdue to the read transistor; however, any slowdown will be mitigatedby minimization of the pull-down nFET size. Withoutstability or write margin concerns, 8T cell performance—likeregular logic—is limited only by normal power, performance, and area tradeoffs.

D. Array design implications

In contrast with conventional 6T-SRAM, 8T-SRAM arraysmust consider both the dual-port nature of the cell as well as theelimination of column select functionality in the array. Whileseparation of the read and write ports can create performanceand array efficiency benefits, the lack of column select resultsin tradeoffs for some specific array applications.

E. Read and Write Port Separation

With separate read and write ports, control circuitry in the peripheryof the array must be altered and can, in fact, be reducedover conventional 6T designs. First, port separation requires asecond set of WL drivers, which adds to the area of the array.Whereas the write WL driver is largely similar to standard WLdrivers used in 6T arrays due to similar capacitive loading, theread WL driver can be significantly reduced in size due to thesingle-ended cell read stack.At the same time, however, with separate read and write wordline signals, a read/write multiplexer is no longer needed at thelocal bit line level, which greatly simplifies local evaluation circuitry.Pass transistors normally used in 6T-SRAM to switch thelocal bit lines between write data drivers and the cell read stackcan be eliminated.

As a result, local write bit line control logicis not needed and only local read sense amplifier logic is required. Especially for high performance arrays that utilize shortlocal bit line lengths, reduction of the local evaluation circuitarea can have a sizeable impact on overall array area.Since the local evaluation circuitry no longer needs to managethe cell write bit lines, global write drivers can instead be used to control the write data. In effect, read and write paths can beindependently optimized by sharing the read and write bit linesacross different numbers of bits. In this work (Fig. 6), the writebit line is shared across 512 bits to improve array efficiency byglobally amortizing the write data driver area. The read bit line,however, is

shared across only 8 bits, which, combined with a hierarchical sensing scheme, helps to ensure a high-speed readpath. Thus, 8T-SRAM enables simultaneous optimization of theread and write paths for performance and area.

While the 8T cell removes read stability concerns, cell disturbscan also occur in unselected columns during a write event.In this case, the write word line may be turned on while the writebit lines (held high) are relied upon to ensure cell stability—asituation identical to a read disturb in a 6T cell. While it is possibleto optimize an 8T cell to withstand such write disturbs, anycell stability advantage would be lost. Instead, this issue must beaddressed by the array organization by entirely prohibiting the column select condition in an 8T array.Traditionally, column select functionality can be used to improvearray efficiency by multiplexing adjacent columns intoshared sense amplifiers.

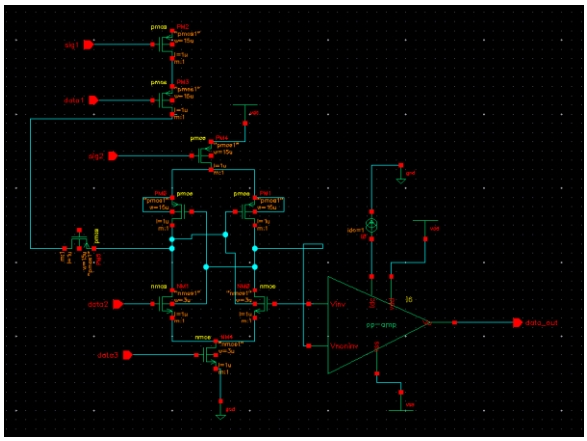

Figure 2. Schematic of multiplexer for cell

F. Elimination of Column Select

The cost includes active power, sincemultiple columns are read in a single event, and some performance,since the multiplexer has a finite delay. Column selectalso enables protection from multi-bit soft error events as bitsfrom different words can be physically interleaved to ensure thata multi-bit error can affect at most one bit per word with highprobability—an error that can be easily detected or correctedwith simple parity checking or error correcting codes (ECC).Partial word writes, in which it may be desirable to update onlya small portion of the bits sharing a single word line, may alsobe facilitated by the ability to perform column select. Each ofthese conditions must be addressed by alternative means in thedesign and organization of 8T-SRAM. To avoid column select, an 8T array should be floorplannedso that all bits in a word are spatially adjacent (Fig. 2).

The number of cells sharing a write word line is thus generally limited by the word length desired by the array architecture. Itshould be noted that this limitation applies only to the writeword line whereas the read word line could be shared acrossmultiple words. Such a floor plan may increase the wiring overheadto properly multiplex the array output, but array efficiencycan likely be maintained as column decode circuitry can beeliminated. Essentially, this column circuitry is simply movedto control the write word line. Active power in the 8T array canthus be reduced because only those columns that need to be accessedwill switch. There is no unnecessary reading of unselectedcolumns as would occur in a 6T array with column selectsince these columns reside on a separate write word line.

Since the storage element in an 8T cell is still comprised ofCMOS inverters, there is no fundamental difference in soft errorrate from a 6T cell. However, cell transistor sizing plays a roleas smaller inverter devices and the additional asymmetric readstack alters the single-bit soft error rate. Since bits from differentwords in 8T-SRAM cannot be physically interleaved, protectionfrom multi-bit soft error events must instead be achieved by interleavingthe parity or ECC code as shown in Fig. 2. Table Ishows an example for protection from soft errors affecting twoadjacent bits. Separate codes can be used for the odd and evenbits of the word to afford comparable resilience to multi-bit errorsas the physical interleaving of bits. An area penalty must beincurred over 6T arrays, however, as the number of bits neededto store the parity or ECC code increases. However, dependingon the data word length, the extra bit penalty can be small forECC (5%versus 6T arrays for a 128 bitsword and nearly negligible for parity. Such interleaving of the ECC or parity code scan be extended to handle soft error events of greater than twobits. For arrays that only use parity checking, the bit penalty incurredcan remain quite small, but if ECC is required, then the penalty incurred is larger.

For specific applications, systems requirements may dictatethe need for partial-word writes. While this likely does not affecta large number of arrays and could be potentially be eliminatedby systems architecture changes, 8T-SRAM can be modified forsuch functionality even without column select techniques. Onemethod to achieve this would be to segment the word line to thepartial-word length. Alternatively, a read-modify-write scheme[10], in which a read always precedes a write to combine thenew and old data bits, can mimic partial-word write operationswith minimal area penalty.With all the aforementioned changes to array design neededto implement 8T-SRAM, the overall effect is that improvedarray efficiency mitigates area penalties associated with a largercell, an extra WL driver, and added ECC bits. As a result, 8Tarray area can be competitive (7% at equal performance) withthat for 6T (Fig. 8). Higher speed arrays with larger 6T cells canshow even smaller area penalties as the array efficiency for sucharrays is usually low to begin with, thus minimizing the impactof the larger cell.

G.Simulation Methodology

The nominal channel doping concentration of the studiedn-type MOSFET (NMOS) devices is with 1.48×1018cm−3 inthis paper; we note that the nominal channel doping concentrationwas empirically adopted from experimental data [10].They have a SiO2 gate-oxide thickness of 1.2 nm and a TiNgate with workfunction of 4.4 eV. To estimate RDF-inducedcharacteristic fluctuation starting from 65-nm-gate devices, wefirst consider the randomness of the number and positionof discrete channel dopants. 12 500 dopants are randomlygenerated in a large cube (325 nm×325

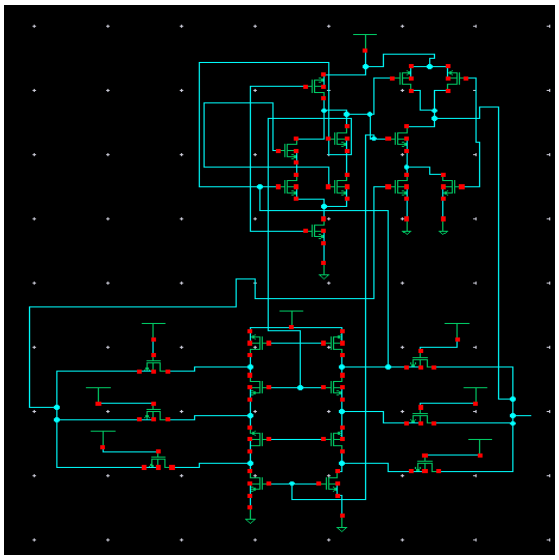

Figure 3. Operating circuit

nm×80 nm), in whichthe equivalent doping concentration is 1.48×1018cm−3, whichis rounded off to the 2nd decimal place of 1.4793×1018cm−3,as shown in Fig. 3. The large cube is then partitioned into125 sub-cubes of (65 nm × 65 nm × 16 nm). The number ofdopants may vary from 70 to 130, where the average numberis 100, as shown in Fig. 3. These sub cubes are equivalently mapped into the device channel for the3-D "atomistic" device simulation with discrete dopants, asshown in Fig. 1. Similarly, we can generate the sets ofdiscrete dopant cases for the 32-nm and 16-nm-gate transistorsas shown in Fig. 1, respectively. In Fig. 1, we apply the statistical approach to evaluate the effect, in which the magnitude of the gate length deviation and the lineedge roughness mainly follows the projections of the ITR Sroadmap [15]. The three-sigma (3) of the process-variation induced gate length deviation and line edge roughness is1.5 nm and 4.3 nm for the 16-nm and 65-nm devices, respectively.

The Vth roll-off is adopted to estimate the PVE-inducedVth fluctuation. For WKF, considering the size of metal grainsand the gate area of the devices, the device gate area iscomposed of a small number of grains as shown in Fig. 3.Since each grain orientation has different workfunction, thegate workfunction is modeled as a probabilistic distributionrather than a deterministic value. Therefore, a statisticallysound Monte-Carlo approach is advanced for examining suchdistribution. The gate area is partitioned into several partsaccording to the average grain size. The gate areas are(65 nm×65 nm), (32 nm×32 nm), and (16 nm×16 nm) for 65-nm, 32-nm, and 16-nm gate planar devices, respectively. Then the grain orientation of each part and total gate workfunctionare estimated based on the properties of used metals, as shownin Fig. 3 [18]. Notably, in "atomistic" device simulation,the resolution of individual charges within a conventionaldrift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [15],[12].

The potential becomes too steep with fine mesh, andtherefore, the majority carriers are non physically trapped by ionized impurities, and the mobile carrier density is reduced.Thus, the density-gradient approximation is used to handlediscrete charges by properly introducing related quantum–mechanical effects, and coupled with Poisson equation as wellas electron-hole current continuity equations [29], [13].Fig. 1(j) and (k) illustrates the explored 6T and 8TSRAMcells, respectively. All cell ratios [CR, CR = ((W/L)driver−transistor)/((W/L)access−transistor)] of the SRAM cells inthis paper are first set as unitary. The applied voltages of16 nm and 65 nm devices are 1.0V and 1.2V, respectively,according to the projections of the ITRS roadmap [19].

Due to the nominal value of the SNM with different device setting are different, the absolute value of SNM fluctuation is here normalizedfor a fair comparison purpose. We use the normalized SNM fluctuation (σSNM) to assess the transfer characteristicfluctuation of SRAM. All physical models and accuracy ofsuch large-scale simulation approach are quantitatively calibrated by experimentally measured results [10]. Similarly,we do generate discrete-dopant-fluctuated cases for p-typeMOSFET (PMOS) through the flow of Fig. 1(a)–(f). Then, werandomly select those fluctuated NMOS and PMOS devicesfor the following examinations. In order to estimate SRAM characteristics with ultra small nano scale transistors, insteadof compact model approach [1]–[4], [18], [17], a device circuit coupled simulation [7], [9], [20] is employed. Thecharacteristics of devices of SRAM circuit are first estimatedby solving the 3-D device transport equations, and are usedas initial guesses in the successively coupled device-circuitsimulation. The SRAMs circuit nodal equations are formulated,
according to the current and voltage conservation laws,and directly coupled to the 3-D device transport equations(in the form of a large matrix containing the circuit anddevice equations), which are solved

simultaneously to obtainthe circuit characteristics [7], [9], [20].

H. SRAM cells and SRAM designs

In this section, we first introduce the 6T and 8T SRAM cellsin CMOS technology, and then propose SRAM cell designs and compare the cell performances in terms of access speed, dynamic and static power, and SNM. The parameter variations for SRAM cells are presented as well. A. SRAM Cells SRAM is a major component of digital systems. Fast memoryaccess times and design for density have been two of the mostimportant target design criteria for many years. However, withdevice scaling to achieve even faster designs, power supplyvoltages and device threshold voltages have scaled as well whichleads to degradation of standby power.The 6T static memory cell shown in Fig. 3 has been widely acceptedas the standardmemory cell. It is designed to achieve fastread times with the inclusion of sense amplifiers. The standard6T cell requires that a logic value and its inverse be placed on thebit lines during a write operation. The word line is raised to logic1 and the logic levels on the bit lines are passed into the cross coupled inverter pair. Device sizing for a CMOS-based cell isdriven primarily by area and functional operation constraints;sizing must be carefully performed to enable the correct logicvalues to be transferred into the cell. Reading from the memory cell entails precharging the bit lines and then asserting logic 1on word line.

The complexity of this cell is in arriving at theappropriate device sizes for proper functionality. The transistorsof the cross-coupled inverter must be sized such that the effort to overwrite a previously stored value does not impact the pulseT1 T2T3T4T5T6WNBitWrite-line Read-lineT7T8RBitWBitFig. 2. 8T SRAM Cell. width of the word line. The worst case noise margin for thiscell occurs under the read condition, since a pass gate (eitherT1 or T2) disturbs the “0” storing node by pulling it up aboveground [10].An 8T memory cell is shown in Fig. 2. This 8T SRAM cell has a similar structure as 6T with two additional transistors thatdecouple read and write operations. The read operation is performedby setting the read–word line to logic 1; the additionaltransistors (T7 and T8) discharge the Bit line that has been precharged before the read line is set. The 8T basic cell provides a more orthogonal design; read and write operations areperformed by different transistors. Since the read operation doesnot affect the contents of the cell (the two back-to-back inverters),the worst case SNM is simply that for two cross-coupledinverters.

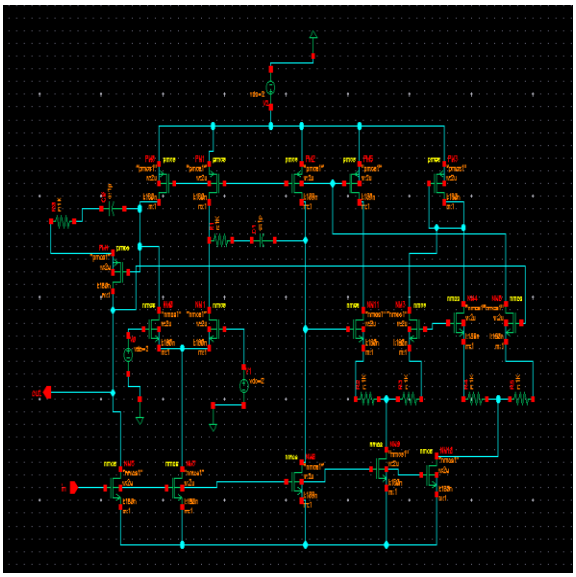

Figure 4.Overall SRAM cell architecture

I. SRAM cells performance

HSPICE simulations have been performed using a Berkeley32-nm PTM HP model [11] and SRAMs parameter modelsby Stanford University’s Nanoelectronics Group [12]–[14].HSPICE is the most accurate circuit simulation that is usedin many semiconductor industry settings. The simulations assumememory arrays with 256 cells to evaluate performancewith significant capacitive loading on the bit lines. The nominalchirality of the CNTs is (19, 0) and a pitch of 20 nm. Thenumber of CNTs per transistor for the 6T SRAM cell is T1(3), T2 (3), T3 (3), T4 (3), T5 (1), and T6 (1). The number of CNTs per transistor for the 8T cell is T1 (6), T2 (6), T3 (1), T4(1), T5 (1), T6 (1), T7 (12), and T8 (12). The number of CNTsper transistor is set to optimize SRAM cell’s performance andfunctionality [15]. The inverter pair in the 8T SRAM cell canbe set to minimum size, since these inverters are needed just to retain the data. Table I shows the performance of the CMOSand SRAM SRAM cells in terms of access delays, energy,power, and SNM. From Table I, the CMOS cells have muchlarger write delays than the SRAM counterparts. The SRAM8T cell has a shorter write delay than the SRAM 6T cell. The 8T cell has minimum-sized inverters that are easier todrive and change the stored data. SRAM 8T cell read delayis significantly smaller than any of the other read delays. Sincethe 6T cells have to discharge either Bit or NBit bus, this makesit difficult to increase current driving capability of the n-typetransistors without greatly affecting write delay. Energy for the SRAM 8T cell is slightly higher than the SRAM 6T cellbut much lower than CMOS cells; these metrics are measured when the RBit line needs to be precharged after reading “0.” If“1” has been previously read, the RBit has not been discharged(it is already at a voltage

close to Vdd); thus, this line does notrequire extra energy to be precharged. This is not the case with6T which needs to precharge either Bit or NBit at every readoperation.

When a read occurs, the precharged bit lines affect either the stored bit or its inverse (the cross-coupled inverter inputs).Although this voltage change is not enough to change thestate of the memory cell, the circuit consumes power to retainthe proper voltage.In a large memory array, static power becomes a dominantfactor in power consumption. It has a multiplicative effect; allcells in the array are drawing this power. The CMOS 8T cellrequires about 60 times more static power than SRAM cells inthis study. The SRAM 8T cell reduces the maximum delay by1.78× compared with CMOS corresponding cell in simulationswith nominal parameter values. In addition, based on the SNMs, the CMOS 6T cell is the least stable, while the SRAM 8T cell has a 13% enhancement over CMOS 8T cell. The comparison shows that SRAM cells perform better than the CMOS cells.A performance comparison of the 6T and 8T SRAM cells(we use data from Table I) reveals that the 8T cell reduces themaximum delay by 3.26 times (29.23ps/8.96ps), decreases thestatic power by 1.68 times, and improves the noise margin by1.126 times. On the other hand, the 8T cell energy is higher by1.129 times.

J. CMOS hybrid memory

Organization of the Hybrid Memory

In this study, we implemented a reduced version, wherethe data directly written by the SFQ inputs are restricted to 8-bit, due to the limitation of the pad number. In contrast withthe previous study, eight-transistor SRAM cells were employedbecause of their fast access time, good stability and largereadout current. The current sensors consist of leveldriven DC/SFQ converters, which detect a small current output with an amplitude of about 100 μA from the memory cell athigh-speed [7].The Josephson-CMOS interface circuits amplify SFQ voltagepulses to CMOS voltage levels by two stages of amplification.

In the first stage, a Josephson latching driver (JLD),which is composed of two parallel connections of 15-junctionstacks of under dumped Josephson junctions, amplifies SFQvoltage pulses to 40 mV-level signals. In the second stage, aCMOS differential amplifier amplifies 40 mV signals to voltlevelsignals, which are processible in CMOS digital circuits.

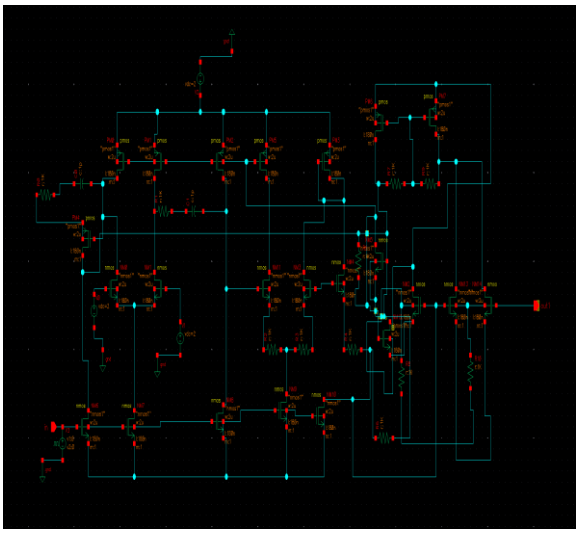

Figure 5. power schedule model

K. CMOS Static RAM

In our previous hybrid memory, three-transistor (3T) DRAMcells were used because they had almost infinite retention timeat cryogenic temperature. However, it turns out that the leakagecurrent of the 0.18 μm CMOS devices or later devices cannot beignored even at cryogenic temperature. The measured retentiontime of 3T DRAM cell using 0.18 μmprocess was about 10 sat 4.2 K while that of the 0.35 μm cell was infinite.Fig. 2 shows a schematic of an eight-transistor (8T) SRAMcell, which was employed in this study. The 8T SRAM cellis composed of a conventional 6T SRAM cell and stacked transistors (M7, M8) to readout the data. The write word line and the write bit line, “WBL” are used in the writeoperation. In the read operation, the transistor M7 is active ifthe node “data_R” stores the charge (state “1”). In this casethe output current is obtained by enabling the read word line,“RWL”. This cell offers a high-speed access-time and goodread/write stability because of the addition of the transistors M7and M8. It can also provide readout current as high as 100 μA,which is enough to drive the following Josephson sensor.A schematic of a CMOS differential amplifier is shown inFig. 3. An important advantage of differential operation oversingle-ended operation is higher immunity to noises. Comparedwith conventional amplifiers, this amplifier is suitable for theinterface circuit in terms of the speed, robustness and powerconsumption [9].Simulated transient characteristics of the 64-kb CMOS staticRAM at 4 K are shown in Fig. 4. In this simulation, we used a cryogenic device model made from experimental data [5].Moreover, the simulation took into account the parasitic capacitanceand resistance, which were extracted from the physicallayout. As shown in the waveforms, datum “1” was written in the phase “Write 1” and read out in the phase “Read 1” in theselected memory cell. Furthermore, datum “0” was written inthe phase “Write 0” and read out in the phase “Read 0”.

Theoutput current only appears in the phase "Read 1". The accesstime of the 64-kb CMOS static RAM with the differential amplifiers was evaluated to be 1.3 ns, which is the sum of thedelay of the CMOS differential amplifier, 0.35 ns and the delayof decoders and a 8T SRAM cell array, 0.95 ns.We also estimated the power consumption of the 64-kbCMOS static RAM, which is listed in Table I. The ratio ofthe power consumption of the decoder and buffer is relativelylarge particularly in the write operation. This is because the full32-bit input buffer is activated in this mode.

V. PERFORMANCE EVALUATION

A. SIMULATION AND RESULTS

The test chip fabricated in UMC 65-nm CMOS technology contains 1-kb (64-word by 16-bit) 9T 4-to-1 bit-interleaved SRAM design with core size 182.25 × 45.46 μm2 using logic design rules. The die photo and block diagram are shown in Fig. 8. The proposed 9T bit-cell size is 1.92× larger than the standard 6T thin cell layout based on the same design rules. Several circuit designs including address decoder, wordline driver, replica column, and read/write pulse controller were presented in [10].

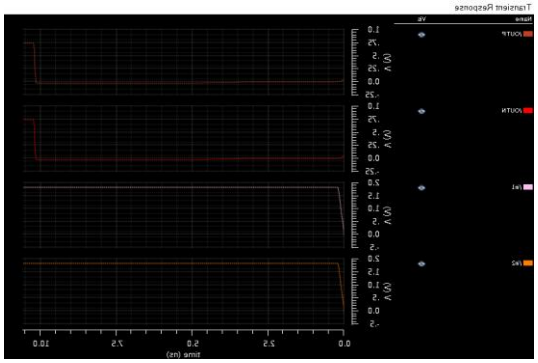

Figure 6. Transient analysis of the SRAM

that a replica column of 9T SRAM anda read pulse controller are implemented to adaptively control the wordline pulse width for process, voltage and temperature (PVT) variation tolerance. The test patterns are generated from logic analyzer 16900A, and the outputs of the test chips are captured by logic analyzer and digital oscilloscope.

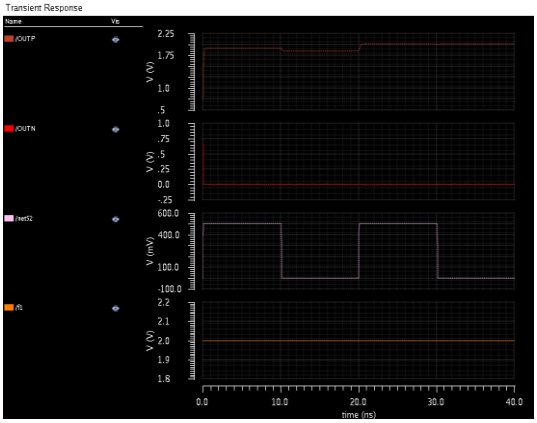

Figure 7. Transient analysis of the SRAM with power schedule

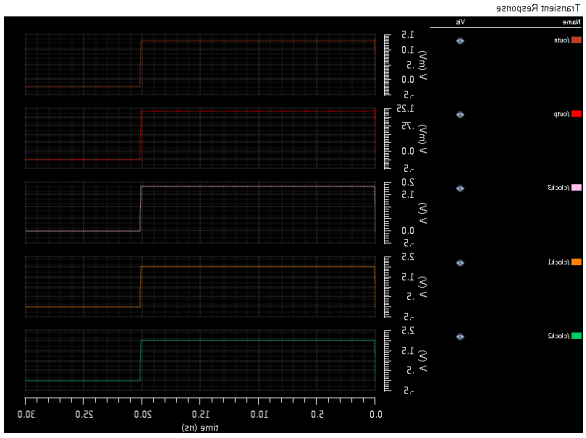

Figure 8. Transient analysis of the SRAM - 1

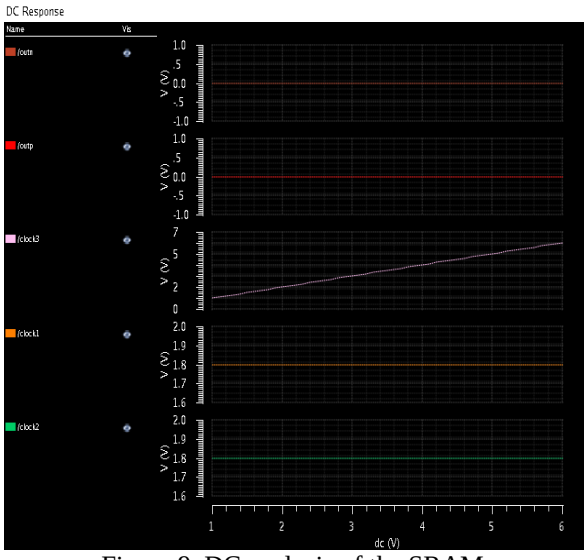

Figure 9. DC analysis of the SRAM

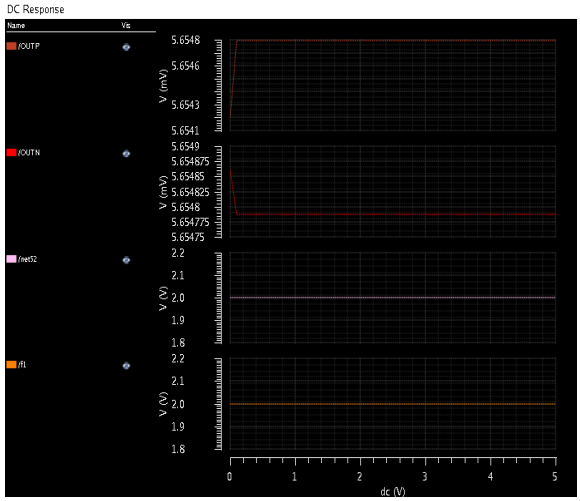

Figure 10. DC response of the SRAM - 1

There are 18 dies being measured, and Table II shows the test chips measurement summary. The chip can successfully operate from 33 MHz at 0.6 V to 0.48 MHz at 0.27 V. The average leakage current of test is 585 nA at 0.3 V. Up to 3.91× energy saving is achieved by scaling supply voltage from 0.6 to 0.3 V. The minimum energy point shown in Fig. 9 is at 0.3-V supply voltage, which takes 3.86 pJ (3.51 μW/909 kHz) energy consumption.

VI. CONCLUSION

In the proposed paper a new SRAM cell using a new algorithm is proposed which will be efficient than the existing methods and the layout of the design shows that it will be more efficient and has the high throughput compared to the other existing methods involved with the older technologies. This be implemented in the Cadence Virtuoso tool of 180nm CMOS process which has the higher throughput which could be operated in the 8T cell, in future same be extended to the 9T cell structure.

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