International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:268
Vol.3, No.2, February 2014 DOI:10.15693/ijaist/2014.v3i2.14-18

Motor current signature analysis of multilevel inverter fed induction motors using wavelets

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Abstract—**This paper deals with fault tolerance capability of three phase induction motor fed by multilevel inverters. This paper provides an analytical tool to quickly analyze and predict the performance of multilevel inverter fed induction motors under fault conditions. Wavelet based fault detection is superior than other spectral methods to depict fault classification in multilevel inverters. Haar wavelet based fault classification in multilevel inverter fed induction motor are tabulated which can be used as reference for diagnosing fault in five level inverters**

Keywords—STFT; MCSA; Wavelets; Fault detection;

I. INTRODUCTION

PWM inverters provide reduced energy consumption, better system efficiency and good performance. For medium voltage grid, connecting one semiconductor switch is not sufficient and hence multilevel inverters are proposed for high power and medium voltage applications such as mills, conveyors, pumps, fans and blowers. Multilevel inverters are also finds low power application in renewable energy sources such as photovoltaic, wind and fuel cells. Multilevel inverters reduces dv/dt stresses on the load and hence advantageous for induction motor fed with inverters.Quality of multilevel inverters is enhanced with the increase in number of levels [3] which leads to large number of semiconductor devices and accompanying gate drive circuits which makes the overall system complex. To detect faults in such a complex system is tedious and time consuming. This paper proposes analytical fault classification using wavelets. Various possible faults are stimulated and analyzed using wavelets.

II. INDUCTION MOTORS

SQUIRREL-CAGE induction machines (IMs) are dedicated for electric drives and play an important role in manufacturing environments. Therefore, this type of machines is generally considered, and several diagnostic procedures are proposed in the literature [2]–[6]

Motor-current signature analysis (MCSA) is one of the most widely used techniques in fault-detection analysis of Induction machines..MCSA focuses its efforts on the spectral analysis of the stator current, measurement.In this paper we consider the stator current outputs for analyzing the fault.

III. WAVELET TRANSFORMS

The Fourier transform is probably the most widely applied signal processing tool in science and engineering. It reveals the frequency composition of a time series by transforming it from the time domain into the frequency domain. To overcome the limitations of the Fourier transform, short-time Fourier transform STFT was introduced. An analysis window of certain length glides through the signal along the time axis to perform a “time-localized” Fourier transform. (STFT). STFT decomposes a time domain signal into a 2D time-frequency representation, and variations of the frequency content of that signal within the window function are revealed. The wavelet transform WT was developed as an alternative to the STFT. Wavelet transform is capable of providing the time and frequency information simultaneously, hence giving a time-frequency representation of the signal. WT s are mathematical means to perform signal analysis when signal frequency varies over time. For certain classes of signals and images, wavelet analysis provides more precise information about signal data than other signal analysis techniques.Continous wavelet analysis is used by choosing HAAR wavelet for fault classification of multilevel inverters.

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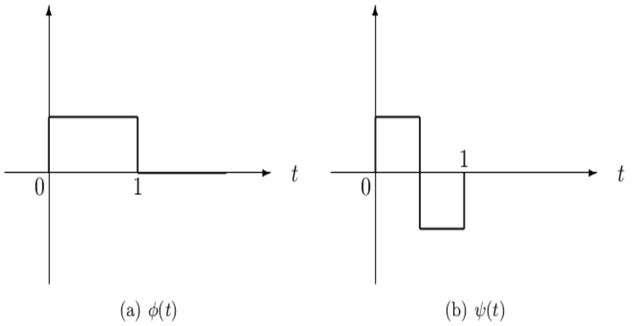
A. *Haar Wavelet*



(a) $\phi(t)$ (b) $\psi(t)$

Fig 1. Haar waveforms

Haar is the first and simplest wavelet.The Haar basis function, better suited than the Fourier basis functions .The Haar basis function can be scaled into different intervals, such as the interval [0, 1] or the intervals [0, 1/2] and [1/2, 1], thereby providing higher precision when modeling a function than that provided by the Fourier basis function, as it can only have one interval [–1, –1].

IV. MULTILEVEL INVERTER

Multilevel converters are mainly utilized to synthesis a desired single- or three-phase voltage waveform. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Cascaded multilevel inverter reaches the higher output voltage and power levels and the higher reliability due to its modular topology [3].For increasing voltage levels the number of switches also will increase in number. Hence the voltage stresses and switching losses will increase and the circuit will become complex. By using the proposed topology number of switches will reduce significantly and hence the efficiency will improve [4].

A.Operation of single phase H bridge inverter

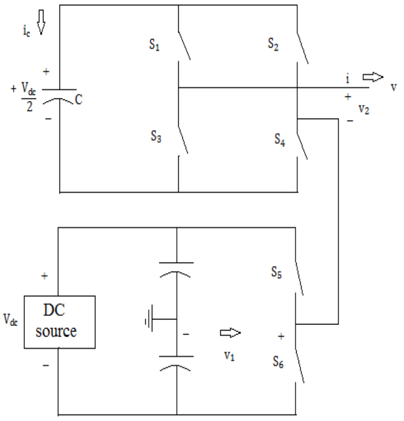


Fig.2.Topology of single phase cascaded H bridge multilevel inverter

To understand the conceptual working of five level inverter topology it is enough to understand how a simple single phase H bridge inverter works. The output voltage v_1 of this leg of the bottom inverter is either $+V_{dc}/2$ (S_5 closed) or $-V_{dc}/2$ (S_6 closed). This leg is connected in series with a full H-bridge.H brige is supplied by a capacitor voltage. If the capacitor is charged to $V_{dc}/2$, then the output voltage of the H-bridge can take on the values $+V_{dc}/2$ (S_1 and S_4 closed), 0 (S_1 and S_2 closed or S_3 and S_4 closed) since this results in short circuit, or $-V_{dc}/2$ (S_2 and S_3 closed). When the output voltage $v = v_1 + v_2$ is required to be zero, we can either set $v_1 = +V_{dc}/2$ and $v_2 = -V_{dc}/2$ or $v_1 = -V_{dc}/2$ and $v_2 = +V_{dc}/2$. During periods of zero voltage output, either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, and S_5 are closed, depending on whether it is necessary to charge or discharge the capacitor. If the capacitor's voltage is higher than $V_{dc}/2$, switches S_5 and S_6 are controlled to output voltage waveform v_1, and the switches S_1, S_2, S_3, and S_4 are controlled to output voltage waveformv_2,. We can observe from the waveform capacitor discharging period, in Fig. 3(b) during which the inverter's output voltage is 0 V.If the capacitor's voltage is lower than $V_{dc}/2$, the switches S_5 and S_6 are controlled to output voltage waveform v_1, and switches S_1, S_2, S_3, and S_4 are controlled to output voltage waveform v_2, shown in Fig. 3(c). We can observe from the waveform in Fig. 3(c) is the capacitor charging period, when the inverter's output voltage is 0 V.Thus we observe five level output produced by the H bridge.

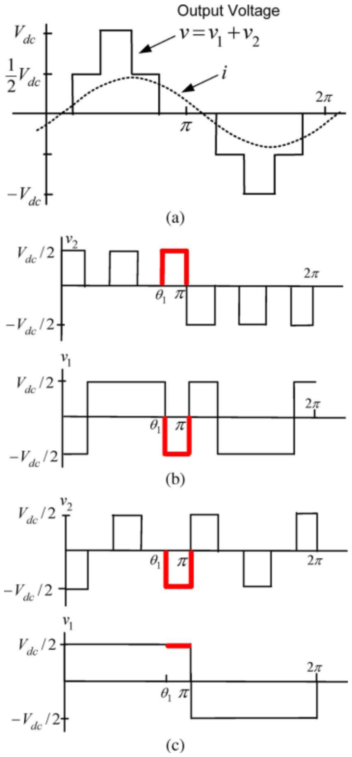


Fig.3.Single phase cascaded H bridge multilevel inverter

B.Three phasecascaded H bridge inverter

With the knowledge of the operation of single phase H bridge inverter we can now Cascade three individual inverters for three phases respectively to obtain three phase five level output. Refer to the topology and the matlab simulink model of three phase five level inverter

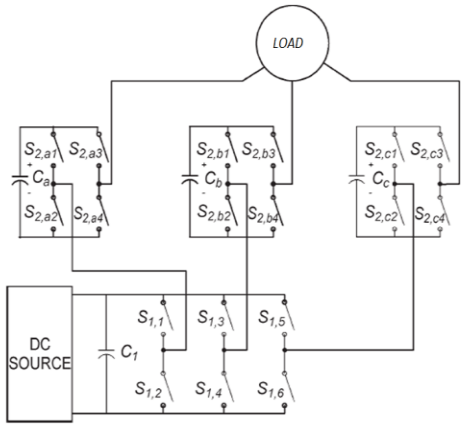


Fig.4.Topology of Three phase cascaded H bridge multilevel inverter

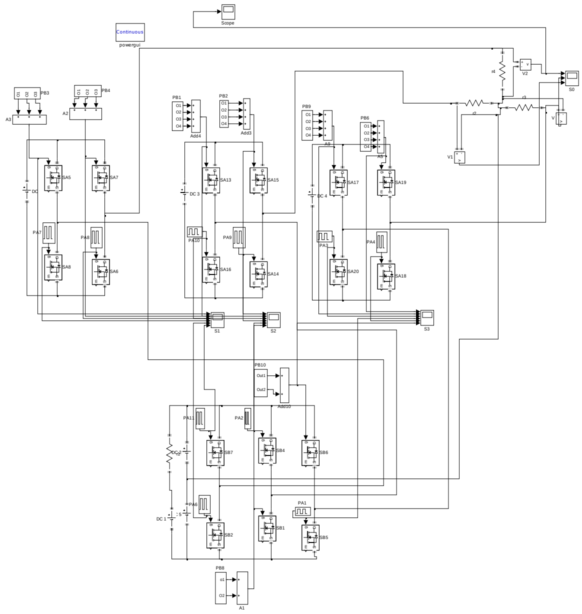


Fig.5.Matlab model of cascaded H bridge multilevel inverter

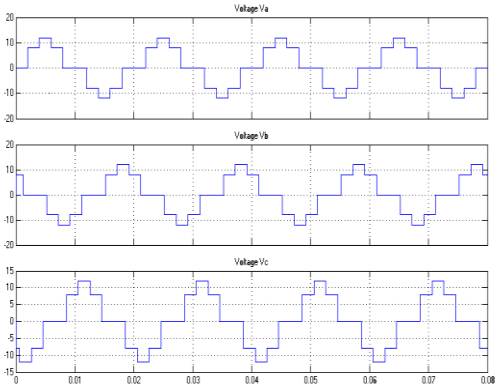


Fig.6.Voltage waveforms of five level inverter

The matlab simulink model of three phase five level inverter connected to resistive load and the corresponding five level output obtained are shown in the Fig.5 and Fig.6

V. MULTILEVEL INVERTER FED INDUCTION MOTOR DRIVE

Multilevel inverters that produced the five level output is now fed to three phase induction motor. The MATLAB Simulink model for the same is shown in the figure 4. The stator current for all three phases are recorded.

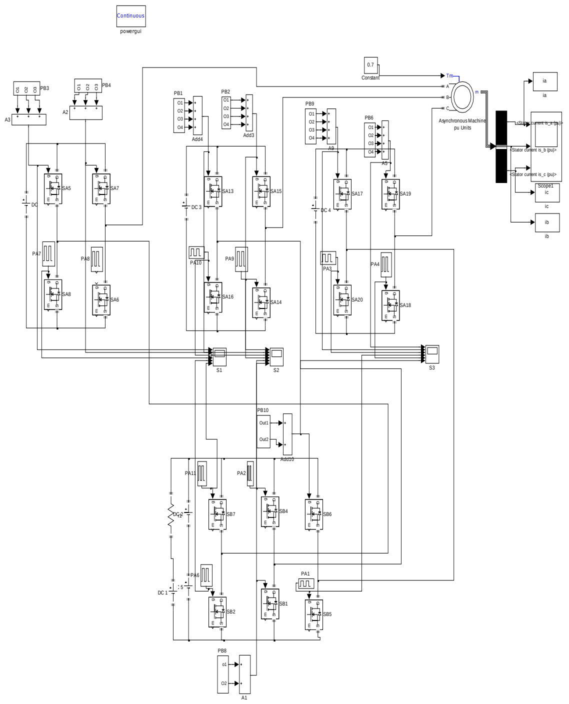


Fig.7.Matlab model of cascaded H bridge multilevel inverter fed induction motor

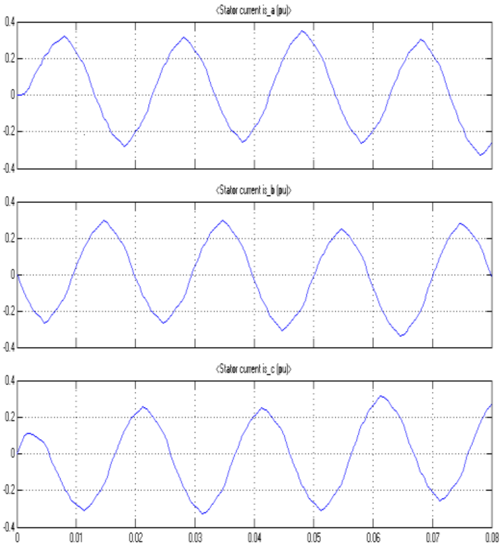


Fig.8.Stator currents of cascaded H bridge multilevel inverter Fed induction motor

VI. FAULT SIMULATION AND WAVEFORMS

The recorded stator currents are further processed using continuous wavelet transforms.Haar wavelet is chosen for decomposition. Initially under normal operating conditions stator currents are decomposed using wavelets.

Further faults are simulated in each phase by terminating pulses to each phase. Stator currents under such fault conditions are decomposed further using wavelets. Waveforms clearly show unusual high frequency components. These components depict fault conditions which can be used as reference for early fault diagnosis[6]

A.Normal and faulty waveforms in phase A

Fault is simulated in phase A by terminating pulses to switches in phase A.

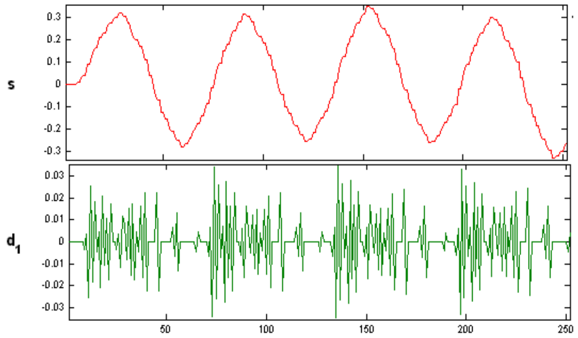


Fig.9(a).Normal stator current ia

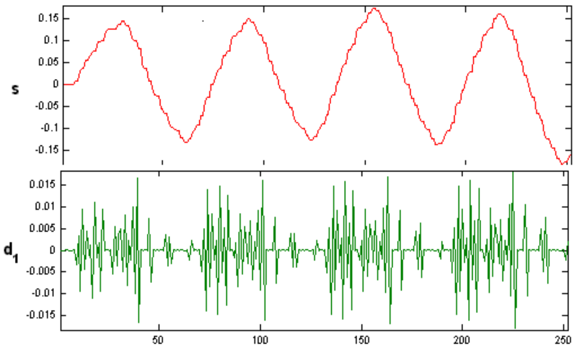


Fig.9(b).Fault 1- stator current ia

From the waveforms, it is inferred that magnitude of stator current ia is reduced. When wavelet decomposition is done, predominating frequency components in the range 95-100 Hz can be observed from the Fig.9(b).

B.Normal and faulty waveforms in phase B

Fault is simulated in phase B by terminating pulses to switches in phase B.

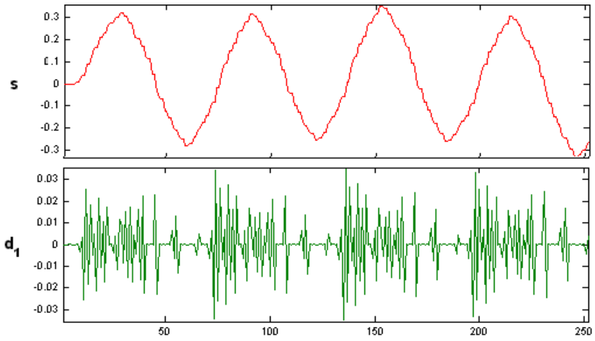


Fig.10(a).Normal stator current ib

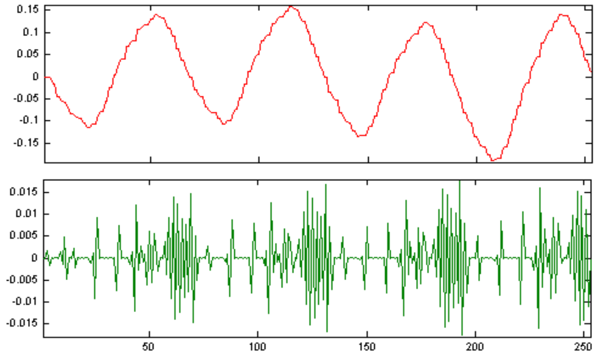


Fig.10(b).Fault 2 stator current ib

From the waveforms, it is inferred that magnitude of stator current ib is reduced. When wavelet decomposition is done, predominating frequency components in the range 55-65 Hz can be observed from the Fig.10(b).

C.Normal and faulty waveforms in phase C

Fault is simulated in phase B by terminating pulses to switches in phase B.

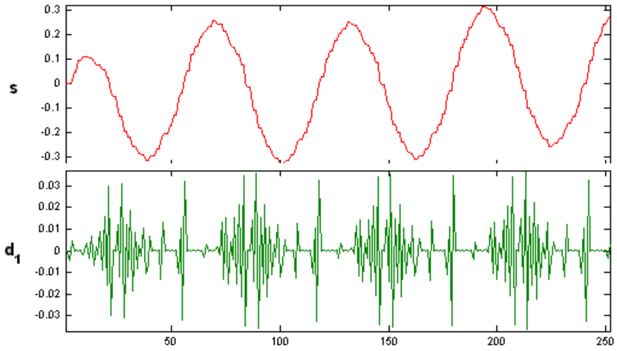


Fig.11(a).Normal stator current ic

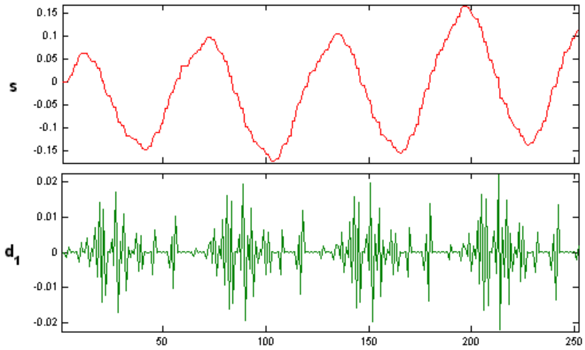


Fig.11(b).Fault 3- stator current ic

From the waveforms, it is infered that magnitude of stator current ic is reduced. When wavelet decomposition is done, predominating frequency components in the range 80-90 Hz can be observed from the fig.11 (b).

VII.RESULTS AND TABULATIONS

Faults thus simulated in each phase and decomposed further clearly show unusual high frequency components. These components depict fault conditions which can be used as reference for early fault diagnosis.

Predominating high frequencies are tabulated for each phase.

S.No	**Stator currents and faulty conditions**		
	Stator current	***Normal high freqrange(Hz)***	***Fault High fre range(Hz)***
1.	Stator current ia	80-90	95-100
2.	Stator current ib	65-75	55-65
3.	Stator current ic	52-54	80-90

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VII. CONCLUSION

A cascaded H-Bridge multi-level inverter fed to drive an induction motor is modeled. Wavelet transform based fault diagnosis method is been implemented in the model described above. The corresponding waveforms are studied and analyzed further. Faulty phases with predominating frequencies are listed. In future work, wavelet neural analysis of the waveforms can be done to study further details and train the switches whose pulses can be changed in accordance with the fault condition and hence assure fault free operating conditions.

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