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Milp Based Fault Free Delay Lines

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Abstract:-A mixed integer linear programming (MILP) technique simultaneously minimizes the leakage and glitch power consumption of a static CMOS circuit for any specified input to output delay. Using dual-threshold devices the number of high-threshold devices is maximized and a minimum number of delay elements are inserted to reduce the differential path delays below the inertial delays of incident gates. The key features of the method are that the constraint set size for the MILP model is linear in the circuit size and power-performance tradeoff is allowed. Experimental results show 96%, 40%, and 70% reductions of leakage power, dynamic power, and total power, respectively, for the benchmark circuit C7552 implemented in the 180 nm CMOS technology using Cadence tool.

Keywords: Dual-Threshold CMOS Circuits, Dynamic Power, Leakage Reduction, Low Power Design, Glitch-Free Design, Mixed Integer Linear Programming (MILP).

1. INTRODUCTION

In the past, the dynamic power has dominated the total power dissipation of CMOS devices. However, with the continuous trend of technology scaling, leakage power is becoming a main contributor to power consumption. To reduce leakage power, several techniques have been pro-posed, including transistor sizing, multi-V_{th}, dual-V_{th}, opti-mal standby input vector selection, stacking transistors, dual V_{dd}, etc. Among these, the dual-V_{th} assignment is an efficient technique for decreasing leakage power. Its basic idea is to utilize the timing slack of non-critical paths to assign high V_{th} to gates on those paths to decrease the leakage. There are heuristic algorithms[8_12_20–24] that search for an optimal solution of dual-V_{th} assignment. For exam-ple, the *backtrace algorithm*[21_22] can determine a dual-V_{th} assignment for a possible solution without guaranteeing an optimal one (see example of Fig. 10). Because the backtrace search direction for non-critical paths is from primary outputs to primary inputs, the gates close to the primary outputs have a higher priority for high V_{th} assign-ment, even though their leakage power savings may be smaller than those of gates close to the primary inputs. Wang et al.[20] treat the dual-V_{th} assignment as a constrained 0-1 programming problem with non-linear constraint func-tions. They use a heuristic algorithm based on circuit graph enumeration to solve this problem. Although their *swapping algorithm* tries to avoid local optimization, aglobal optimization is still not guaranteed.

By describing both the objective function and con-straints as linear functions, linear programming (LP) can easily get a globally optimum solution. Nguyen et al.[11] use LP to minimize the leakage and dynamic power by gate sizing and dual-threshold voltage device assignment. The optimization work is separated into several steps. An LP is first used to distribute slack to gates with the objec-tive of maximizing total power reduction. Then, another independent algorithm resizes gates and assigns threshold levels. This means that the LP still needs the assistance of a heuristic algorithm to complete the optimization.[11]Gao and Hayes[5] use mixed integer linear programming (MILP) to optimize the total power consumption by dual-threshold assignment and gate sizing.

The techniques cited above[5_8_11_12_20_22_23] have not con-sidered the glitch power, which can account for 20%– 70% of the dynamic switching power.[4] To eliminate these unnecessary transitions, a designer can adopt techniques of hazard filter[2_25–28] and path balance.[3_14_29] In Hazard fil-tering, gate sizing or transistor sizing is used to increase a gate inertial delay which can filter the glitches. An obvi-ous disadvantage of hazard filtering, when used alone, is that it may increase the circuit delay due to the increase of the gate delay. Alternatively, any given performance can be maintained by path delay balancing, although the area overhead and additional power consumption of the inserted delay elements can become a major concern.

In the present research, a new MILP model is proposed to minimize leakage power by dual-Vth assignment

and simultaneously eliminate dynamic glitch power by inserting zero-subthreshold delay elements to balance pathdelays. To our knowledge, no previous work on optimizing dynamic and static power has adopted such a combined approach. This MILP method is specifically devised with a set of constraints whose size is linear in the number of gates. Thus, large circuits can be handled. Although theoretical worst-case complexity of MILP is exponential,actual complexity depends on the nature of the problem. A discussion about this point is presented at the end of Subsection 6.1. To deal with the complexities of delay models and leakage calculation, two look up tables for the delay and leakage current for both low and high thresh- old versions are constructed in advance for each cell. This greatly simplifies the optimization procedure. To further reduce power, other approaches such as gate sizing can be easily implemented by extending our cell library and look up tables. However, a dual-Vdd may require additional considerations beyond the delay look up tables for low Vdd and high Vdd.

This paper is organized as follows. Section 2 presentsthe necessary background knowledge about subthresh-old leakage, delay, and glitches. Section 3 proposes themixed integer linear programming for power minimization.Sections 4 and 5 discuss the implementation of delay ele-ments for glitch elimination and the superiority of MILP,respectively. In Section 6, experimental results are pre-sented and discussed. A conclusion is given in Section 7.Some work from this paper has appeared in a recent pre-entation by the authors.9

2. BACKGROUND

2.1. Leakage and Delay

The leakage currentof a transistor ismainly the resultof reverse biased PN junction leakage and subthresholdleakage. Compared to the subthreshold leakage, the reversebias PN junction leakage can be ignored. The subthresholdleakage is the weak inversion current between source anddrain of an MOS transistor when the gate voltage is lessthan the threshold voltage.24 It is given by:7 where _0 is the zero bias electron mobility, n is the sub-hreshold slope coefficient, Vgs and Vds are the gate-to-source voltage and drain-to-source voltage, respectively,VT is the thermal voltage, Vth is the threshold voltage,Cox is the oxide capacitance per unit area, and Weff and Leffare the effective channel width and length, respectively.Due to the exponential relation betweenVth and Isub, anincrease in Vth sharply reduces the subthreshold current

Table I. Leakage currents for low and high V_{th} NAND gates.

Input vector	Low V_{th}	High V_{th}	Reduction (%)
00	1.7360	0.0376	97.8
01	10.323	0.2306	97.8
10	15.111	0.3433	97.7
11	17.648	0.3169	98.2

Our Spice simulation results on the leakage current of a two-input NAND gate are given in Table I for 70 nm BPTM CMOS technology1 (Vdd = 1 V, Low Vth = 0_20 V, High Vth = 0_32 V). The leakage current of a high Vth gate is only about 2% of that of a low Vth gate. If all gates in a CMOS circuit could be assigned the high threshold voltage, the total leakage power consumed in the active and standby modes can be reduced by up to 98%, which is a significant improvement. However, according to the following equation, the gate delay increases with the increase where _ equals 1.3 for short channel devices.17 Table II gives the delays of NAND gates obtained from Spice simulation when the output fans out to varying numbers of inverters. We observe that by increasing Vth form 0.20 V to 0.32 V, the gate delay increases by 30%–40%. We can make tradeoffs between leakage power and performance, leading to a significant reduction in the leakage power while sacrificing only some or none of circuit performance. Such a tradeoff is made in MILP. Results in Section 6.1 show that the leakage power of all ISCAS85 benchmark circuits can be reduced by over 90% if the delay of the critical path is allowed to increase by 25%.

2.2. Glitch Elimination Techniques

When transitions are applied at inputs of a gate, the out put may have multiple transitions before reaching a steady state (Fig. 1 and Fig. 2(a)). Among these, at most one is an essential transition, and all others are unnecessary transitions often called glitches or hazards. Because switching power consumed by the gate is directly proportional to the number of output transitions, glitches reportedly account for 20%–70% dynamic power.4 Agrawal et al.3 prove that a combinational circuit is minimum transient energy design, i.e., there is no glitch at the output of any gate, if the difference of the signal arrival times at every gate's inputs remains smaller

than the inertial delay of the gate. This condition is expressed by the following inequality:

Table II. Delays of low and high V_{th}	NAND gates.		
	Gate delay (ps)		
Number of fanouts	Low V_{th}	High V_{th}	% increase
1	14.947	21.150	41.5
2	22.111	30.214	36.6
3	29.533	39.171	32.6
4	37.073	48.649	31.2
5	44.623	58.466	31.0

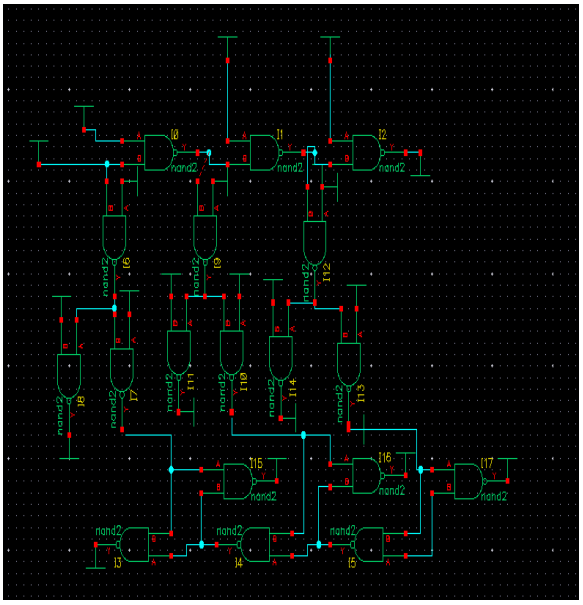

Fig. 1. Output timing window for an n-input NAND gate.

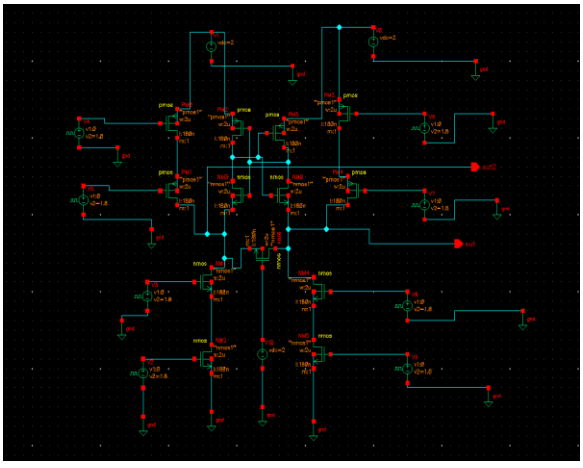

Fig. 2. Glitch elimination methods.

where we assume t_1 is the earliest arrival time at inputs, $t_n$is the most delayed arrival time at another input, and $d_i$is gate's inertial delay, as illustrated in Figure 1. The inter-val$t_n - t_1$ is referred to as the gate output timing window.[14] To satisfy inequality,[4] we can either increase the inertial delay d_i (*hazard filtering*) or decrease the path delay dif-ference$t_n - t_1$ (*path balancing*). Figures 2(b) and (c) illus-trate these procedures for the gate of Figure 2(a). Hazard filtering, when used alone, can increase the overall input to output delay. Path balancing does not increase the delay but requires insertion of delay elements. A combination of the two procedures can give an optimum design.[3_29]

3. AN MILP FOR POWER MINIMIZATION

We use a mixed integer linear programming (MILP) model to determine the optimal assignment of V_{th} while maintain-ing any given performance requirement on the overall cir-cuit delay. To minimize the total leakage the MILP assigns low V_{th} to the largest possible number of gates while controlling the critical path delays. Unlike the heuristic algorithms,[8_12_20_22_23] the MILP gives us a globally opti-mal solution as discussed in Section 5.

To eliminate the glitch power, additional MILP con-straints determine the positions and values of the delay elements to be inserted to balance path delays within the inertial delay of the incident gates. We can easily make a tradeoff between power reduction and performance degra-dation by changing the constraint for the maximum path delay in the MILP model.

3.1. Variables

Each gate is characterized by four variables:

X_i: assignment of low or high$V_{th}$to gate*i*is specified byan integer X_i which can only be 0 or 1. A value 1 means that gate i is assigned low V_{th}, and 0 means that gate i is assigned high V_{th}. Each gate has two possible values of delays, D_{Li} and D_{Hi}, corresponding to low and high thresholds, respectively.

T_i: latest time at which the output of gate*i*can producean event after the occurrence of an input event at primary inputs of the circuit.

t_i: earliest time at which the output of gate*i*can producean event after the occurrence of an input event at primary inputs of the circuit.

$\_d_{i\_j}$: delay of a possible delay element that may beinserted at the input of gate i from gate j.

Thus, an n input gate is characterized by $n + 5$ quanti-ties, i.e., n input buffer delay variables, two inertial

delay constants, one [0, 1] integer variable, and two output tim-ing window variables..

3.2. Objective Function

The objective function for the MILP is minimization of the sum of all gate leakage currents Ileaki and the sum of all inserted delays If we know the leakage currents of all gates, the leakage power can be easily obtained.Therefore, the first term in the objective functions of this MILP minimizes the sum of all gate leakage currents, i.e., ILi and IHi are the leakage currents of gate i with low Vthand high Vth, respectively.Recognizing that the subthresholdcurrent of a gate depends on its input state, we makea leakage current look-up table of ILi and IHi for all gatesi through simulation.These look-up tables are similar to Table I and are used for power estimation by logic simulation as discussed in Section 6.F or the MILP, we need one set of ILi and IHi for each gate and the average values from the look-up tables can be used. Besides the leakage power, we also minimize the glitch power, simultaneously. We insert minimal delays to satisfy the glitch elimination conditions at all gates.This leads to the second term in the objective function.

When implementing these delay elements, we use transmission gates with only the gate leakage.The two terms in the objective function,of benchmark circuits.Therefore, the objective function of Eq.(5) puts greater emphasis on leakage power, assuming it to be the dominant contributor to the total power.Experimental results show that an objective function constant and B = 1 generates the same results as those by the objective function of Eq.(5) in which the terms are left unweighted.In general, suitable weight factors A and B can be used to make tradeoffs between leakage power reduction and glitch power elimination.

3.3. Constraints

Constraints are imposed on each gate i with respect to each of its fanin j, where j refers to the gate providing the fanin:

where DHi and DLi are the delays of gate i with high Vthand low Vth, respectively.With the increase in fanouts, the delay of the gate increases proportionately.Therefore, a look-up table is constructed by simulation and specifies the delays for all gate types for varying fanout numbers. and DHi for gate i are obtained from the look-up table entries are indexed by the gate type and the number fanouts.As discussed in Subsection 2.2, constraints (9–11) ensure that the inertial delay of gate i is always larger than the delay difference of its input paths.This would be done by inserting the minimal number of delay elements while maintaining the critical path delay constraints. We explain constraints (9–11) using the circuit shown in Figure 3.Here the numbers on gates are gate indexes and not the delays.Red (bold) lines show critical paths and two grey shaded triangles are delay elements possibly inserted on the input paths of gate 2.Similar delay elements are placed on all primary inputs and fanout branches throughout the circuit.Let us assume that all primary input (PI) signals on the left arrive at the same time.F or gate 2, one input is from gate 0 and the other input is directly from a PI.Its constraints corresponding to inequalities (9–11) are:

$T2 \geq T0$

Variable T2 that satisfies inequalities (12) and (13) is the latest time at which an event (signal change) could occur at the output of gate 2.V ariable t2 is the earliest time at which an event could occur at the output of gate 2, and it satisfies both inequalities (14) and (15).Constraint (16) means that the difference of T2 and t2, which equals the delay difference between two input paths, is smaller.

6.RESULTS

To study the increasingly dominant effect of leakage power, we use the BPTM 70 nm CMOS technology.1 Low Vth for NMOS and PMOS devices are 0.20 V and−0.22 V, respectively. High Vth for NMOS and PMOS are 0.32 V and −0.34 V, respectively. We regenerated the netlists of ISCAS'85 benchmark circuits using a cell library in which the maximum gate fanin is 5.Two look-up tables for gate delays and leakage currents, respectively, of each type of cell were constructed using Spice simulation. A C program parses the netlist and generates the constraint set (see Section 3) for the CPLEX ILP solver in the AMPL software package.13 CPLEX then give the optimal Vth assignment as well as the value and position of every delay element.The dynamic power is estimated by an event driven logic simulator that incorporates an inertial delay glitch filtering analysis.

6.1. Leakage Power Reduction

The results of the leakage power reduction for ISCAS'85 benchmark circuits are shown in Table III.Here the objective of the MILP was set to minimization of leakage alone. All di j variables were forced to be 0 and constraint 11 was suppressed.The numbers of gates in column 2 are for our gate library

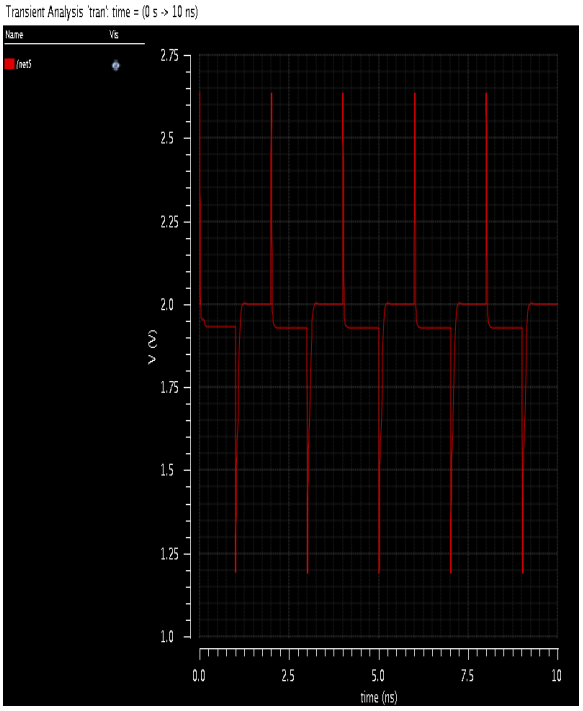

Fig.3. Circuit from the existing with gitches

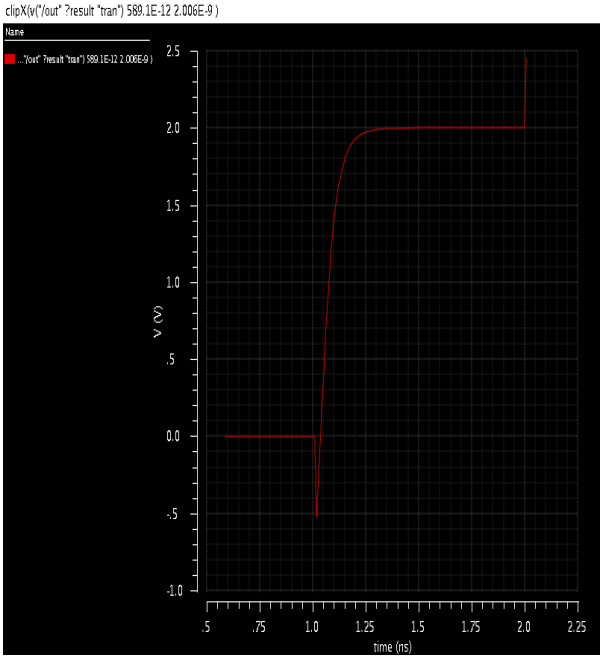

Fig.4. Single transient response showing glitch

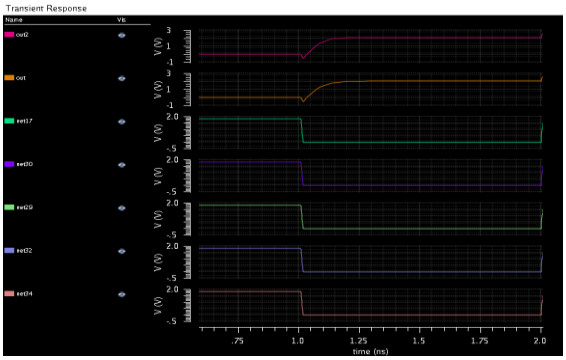

Fig.5. Step input transient response

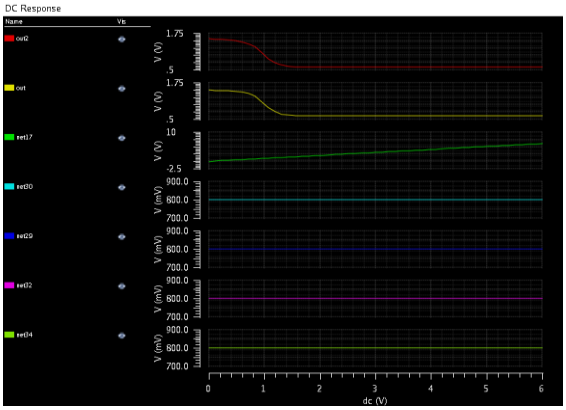

Fig.6. DC response from the different voltage level

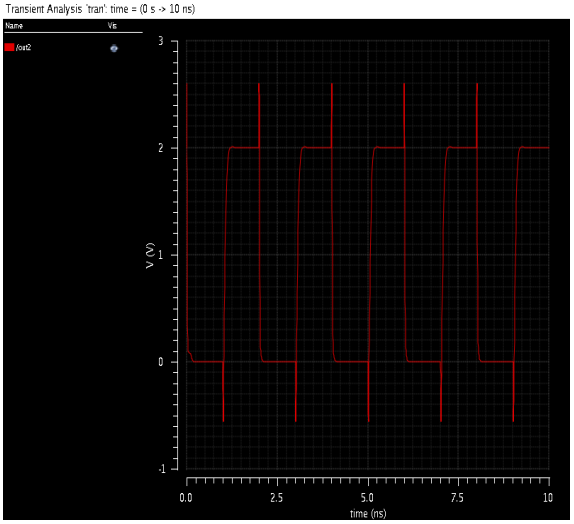

Fig.7. showing the various glitching performsand differ from those in the original benchmark netlists. Tc in column 3 is the minimum delay of the critical path when all gates have low Vth.This was determined by the LP discussed in Subsection 3.3 in the paragraph following Eq.(17).Column 4 shows the total leakage current with all gates assigned low Vth.Column 5 shows the optimized circuit leakage

current with gate Vth reassigned according to the MILP optimization.Column 6 shows the leakage reduction (%) for optimization without sacrificing any performance.Column 9 shows the leakage reduction with 25% performance sacrifice.

criticalpaths.However, for some highly symmetrical circuits, which have many critical paths, such as C499 and C1355, the leakage reduction is less.Column 9 shows that the leakage reduction reaches the highest level, around 98%, with some performance sacrifice. The curves in Figure 6 show the relation between normalized leakage power and normalized critical path delay in a dual-Vthprocess.Unoptimized circuits with all low Vth gates are at point (1, 1) and have the largest leakage power and smallest delay.With optimal Vth assignment, leakage power can be reduced sharply by 60% (from point (1, 1) to point (1, 0.4)) to 90% (from point (1, 1) to point (1, 0.1)), depending on the circuit, without sacrificing any performance. When normalized Tmax becomes greater than 1,i.e., we sacrifice some performance, leakage power further decreases with a slower decreasing trend.When the delay increase is more than 30%, the leakage reduction saturates at about 98%.Thus, Figure 11 provides a guide for making tradeoffs between leakage power and performance.

CONCLUSION

A new technique to reduce the leakage and dynamic glitch power simultaneously in a dual-Vth process is proposed in this paper.A mixed integer linear programming (MILP) model is generated from the circuit netlist and the AMPL CPLEX13 solver determines the optimal Vth assignments for leakage power minimization and the delays and positions for inserting delay elements for glitch power reduction. Experimental results for ISCAS'85 benchmarks show reductions of 20%–96% in leakage, 28%–76% in dynamic (glitch), and 27%–76% in total power.W e believe some of the other techniques, such as gate sizing and dual power supply can also be incorporated in the MILP formulation. Ongoing work incorporating process variation in this power reduction technique will be the topic of a future publication.31 The transmission gate delay elements avoid the comparatively larger capacitive dissipation and subthreshold leakage inherent in the alternative design of twoinverter type of delay elements.However, the gate leakage of the transmission gate delay element could become a concern and will require further investigation.

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