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Low Power Receiver Using Envelope Detector Using Converters

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ABSTRACT–voltage converter is a risky factor that to be operate in the very low power. That to operating it in the very low power is a tedious process. In a proposed model new voltage converter is designed with the radio receivers and transmitters in the case of the wireless modelling of the system. This could be done using the schematic diagram using a Cadence virtuoso tool under 180nm CMOS process. By utilizing the sensor network under the different band modules this be done in the on-off keying modulation. The implementation of power saving sensor censoring strategies on a novel wireless electronic modelling isemployed for achieving the high throughput, reduced sensitivity, and reduced power.

KEYWORDS --power saving, sensor censoring, wireless chemical sensing.

INTRODUCTION

Tapered transmission lines are used extensively in narrowband microwave circuits. Their use as transformers in pulsed circuits, however, introduces additional complexities. For instance, one technique for raising the voltage in a fast pulse involves propagating the pulse along a transmission line with characteristic impedance that increases along the line. To minimize distortion of the propagating pulse, its temporal components must be short compared to the transit time of the tapered transmission line. Thus, a critical design parameter is the determination of the length of the tapered transmission line, or transit time, for a given characteristic impedance ratio taper and input pulse shape. Moreover, it is also instructive to determine which functional forms of taper geometry allow for the shortest transmission line and smallest for a given allowable output pulse distortion.

In trying to optimize the tapered transmission line, the constraints on the source and load impedances need to be noted. Some researchers have incorporated frequency-dependent source and load characteristics to compensate for the drop in the pulse at the load after the initial step rise [1], [2]. Much literature has been devoted to the problem of optimizing such nonuniform, or tapered, transmission line transformers, but for power transmission across a broad band of frequencies such as via a DolphTchebycheff taper [3], [4]. In our problem, the transmission, including phase, is important. A bibliography of some of the older papers is given in [5]. In the present paper, we approach the problem using the modern product-integral approach giving closed-form (product-quadrature) representations [6]–[9]. While initially developed for multiconductor transmission lines, the formulations apply for the present case with giving matrix equations. The following analysis is rigorous and uses normalized transfer functions to investigate the drop in the output pulse of the tapered transmission line pulse transformer with the intention of minimizing it. The early-time/high-frequency gain is known, and the droop is investigated using a response function expanded in terms of the Laplace variable, which is the normalized complex frequency. In expanding the response function, the term leading to droop is identified and can be used to determine the optimum geometry for a tapered transmission line transformer to minimize the drop in the output pulse.

There are mainly two types of transmission line transformers: the one described here and another that uses magnetic cores. More information about the other model is found in Keping [6]. Modern cable technology can handle very high electric field stress and this gives the opportunity to use high-voltage cables as windings [7]. The continuous voltage limit can be exceeded several times when the cable is used in pulsed applications. However, the insulation strength of the cable is strongly dependent on the pulse duration. The aim of the investigation was to enhance the performance of the pulse conditioning system by the introduction of a step-up pulse transformer. The storage inductor was replaced with the primary circuit of the transformer. The standard pulse system is equipped with a 3.5- H energy storage inductor, and the transmission line transformer was designed with an equal primary inductance.

The high-voltage cable has a construction similar to [1] with crimp hose outside the outer conductor. The crimp hose is not optimal concerning electrical breakdown prevention;

however, it allows for a relatively straightforward experimental design. In order to increase the dielectric strength on the primary winding, the crimp hose was complemented by thin discs of polyethylene between each spiral layer in the transformer.

TRANSMISSION-LINE TRANSFORMERS

Constructions

A transmission-line transformer consists of a coaxial cable where the inner and outer conductors act as windings. The step-up transformer is made from a coaxial cable where the inner conductor is used as the secondary winding and the screen is the primary winding. Fig. 1 shows the Tuned receiver circuit step-up configuration and its corresponding circuit diagram with an equivalent winding ratio of 4. The inductance of the secondary winding of the transformer can be calculated with the Wheeler formulas [9] for single layer coils with the inductance, resistors.

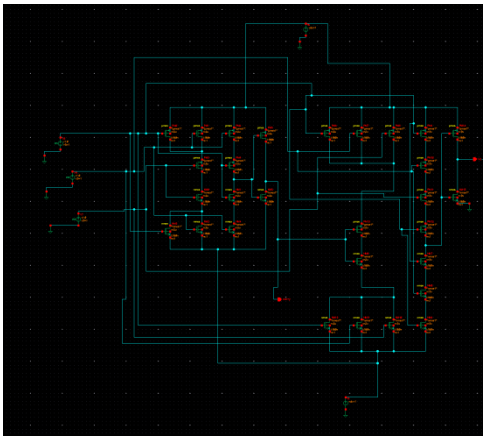

Fig.1. Tuned receiver circuit with functional block of the transmission line

For this formulation, the tapered transmission line is assumed lossless with$Z = sL'$, where is the inductance per unit length, and similarly, $Z = kL + Mn'$ and $Y = sL$ isthe capacitance per unit length. Assume the tapered transmission line consists of nearly perfect conductors in an insulating medium characterized by its permittivity$E$, permeability, and wave velocity 0 . A transmission-line transformer can be simulated quite accurately with distributed inductance, capacitance, and resistance in an equivalent electric circuit network. Fig. 2 shows how the different components are arranged with Narrow band circuit model and distributed for a transformer with a winding ratio of four. The primary inductance consists of four inductors coupled in parallel and the secondary inductance $L1$ is coupled in series. Since $K'1$ and $L'1$share a common magnetic flux the input parameters to the circuit model becomes

$$K'1 = L'1$$

The two-dimensional magnetic field solver Ace [5] was used to calculate the primary, secondary, and mutual inductance of the transformer. The energy of the magnetic field is calculated as a volume integral (3.1) and the calculation use static magnetic analysis and constant permeability. The simulation is made in the frequency domain and a solution is calculated at each frequency step. The calculation at each frequency step requires a lot of time for the relatively large structure and mesh. The total energy of the magnetic field in a volume.

An ideal TLT generally has the ability of transforming a high voltage pulse into hundreds of kilovolts, depending upon the maximum voltage that the coaxial transmission lines can withstand, as well as its stage number. However, an unwanted effect of pulse droop induced by the parasitic secondary transmission lines, i.e., the short circuit paths illustrated in Fig. 1, into which must be put into serious consideration.

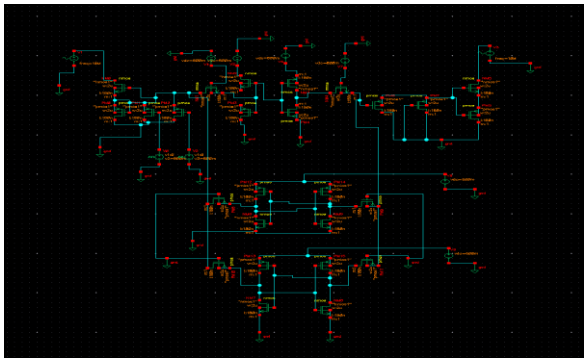

Fig.2. Narrow band circuit model

There are mainly two methods for weakening this influence, i.e., increasing the impedance of secondary lines and lengthening the primary lines. The magnetic rings with high permeability can effectively increase the impedance of the secondary lines to suppress the output pulse droop. On the contrary, lengthening the primary lines is effective only when the pulse has a width less than twice the propagation time along the secondary lines. To avoid having to use an excessive length of transmission lines for longer pulses, the method of adding magnetic rings to the transformer
is the better way for suppressing the pulse droop. Two well-known means of introducing the magnetic rings are the rings covering transmission lines [10] and winding the lines onto the rings [11], respectively. These can effectively reduce the pulse propagation in the parasitic secondary lines by raising their practical impedances. Graneau et al. Reported an approach to evaluate the performance of this type oftransformer such as in Fig. 1 (four-stage) by using a referral method [12]. The established expression for predicting theoutput pulse voltage of the n-stage transformer of this

type, when ignoring stray capacitance, is found to be

$$\mathrm{Vt}^{n} = nV - \sum_{k=0}^{n-1} \left(\mathrm{K}\binom{n}{k}\right) Nf^{1f}\,\mathrm{nL}^{n-0}$$

Where$V$ is the amplitude of the input pulse voltage source, and t is the pulse duration; L is the inductance of each secondary line produced by its winding onto the magnetic rings, and Zo is the characteristic impedance of each transmission line. This original expression can only be used for predicting the case of all secondary lines having the same induced inductances L. However, this is not the optimal arrangement to use the magnetic rings. To achieve an optimal arrangement, we first replace L with Lk, and a modified expression from (1) is obtained as

$$\mathrm{Vt}^{n} = nV - \sum_{k=0}^{n-1} \left(\mathrm{K}\binom{n}{k}\right) Mf^{1f}\,\mathrm{K}^{n-0}$$

where k is the ordinal stage number of each primary line. When the total inductive isolation $L2 + L3 + \cdots + Ln$ is fixed as a constant, the goal of the optimization is, therefore, making the following expression be the smallest:

$$\left(1 + \sum k\,x\right)^{\mathrm{k}} = 1 + \frac{nMf}{L!} + \frac{M(m-1)x^{2}}{2L!} + \cdots$$

The transverse voltage and the longitudinal EMF induced on a dc line by a parallel ac line in close proximity are calculated with the electromagnetic transient program (EMTP). In order to simulate the parallel ac/dc transmission lines system as shown in Fig. 1, a multi conductor overhead transmission line voltage.

OSCILLATOR FREE ARCHITECTURE

TheWake-Up radio has the single purpose to recognize a predetermined ID-code bit pattern in the air and the chosen architectureis focused on simplicity. It uses no oscillators, and nocontrol or calibration loops as phased locked loops or super regenerativesolutions. This enables short startup time and avoidanceof lock-in processes adding to overall power consumption[20].As much as possible of the radio functionality should behandled over to the interrogator or reader (the term "reader"emanates from the RFID community and is a bit misleadinghere since we only use downlink communication). A very smallamount of data will be sent at each wake up session, only a fewhundred bits long ID-code. We use on–off keying modulationof the carrier; although this is spectral inefficient it is motivatedby the short transmission bursts and the simplification of thereceiver design. A carrier frequency of 2450 MHz (ISM) offersa good compromise between size and range, and an ability tobaseband output voltage from the envelope detector is proportional to the square of the input amplitude of the RF carrier see "around" obstacles.

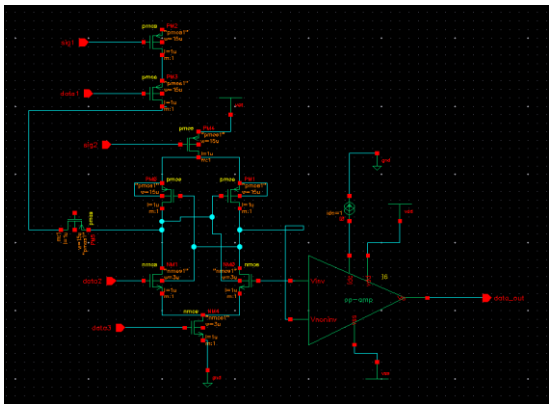

Fig.3. Magnetically coupled transformer circuit with distributed inductance

Envelope Detection

The incoming RF carrier drives a diode, or other rectifyingcomponent. The envelope detector self mixing efficiency fallsoff as the carrier power decrease. Thus, the sensitivity for atuned RF receiver ismoderate compared to the super heterodynewith a mixer always being driven by a strong LO signal. However,the typical application for theWake-Up receivers requiresonly rather short transmission range, up to about 10 m [12]. Areduction in active power achieved by excluding the local oscillatoris well motivated.The envelope detector folds the modulated spectrum aroundthe carrier down to baseband frequency. Theend, the line is terminated by impedance. This means that only a group of turns can be examined and the other turns of the transformer winding can be represented by equivalent impedance. As the equivalent impedance has a significant influence,it must be calculated accurately for each frequency. In [17], a method is proposed for estimating this impedance accurately. Hybrid modelling gives a good approximation for layer-type windings. The transformer is therefore modelled on a layer-to-layer basis instead of a turn-to-turn basis.

Transformer Description

To calculate the voltage transients in transformer windings, it is important to determine the transformer parameters with higher accuracy. These parameters are the inductances, the capacitances, and the frequency-dependent losses. The modelling approach depends heavily on the transformer construction and the type of windings. The test transformer in this case is a single phase layer-type oil transformer. Fig. 2 shows the transformer during production in the factory. The

primary transformer winding consists of layers with a certain number of turns; the secondary winding is made of foiltype layers. The transformer is equipped with special measuringpoints in the middle and at the end of the first layer of the transformerhigh-voltage side, and also at the end of the second layer.All measuring points can be reached from the outside of thetransformer and measurements can be performed directly at thelayers. Table shows the transformer data.

Determination of the Transformer Parameters

Capacitance:

Fig. 3 shows the magnetically coupled transformer circuit with distributed inductance that are necessary for the computation of the fast transients inside the windings. These were calculated by using the basic formulas for plate and cylindrical capacitors. This is allowed because the layers and turns are so close to each other that the influence of the edges is negligible. The capacitances between the turns are important for the computation of transients in the turns. However, since the very large dimensions of the matrix prevent the voltages in each turn from being solved at one and the same time, a matrix reduction can be applied [11], [12] so that the order of matrices corresponds not to a single turn but to a group of turns. In this way, the voltages at the end of the observed group of turns remain unchanged. Later, these voltages can be used for the computation of the voltage transients inside a group of turns. Capacitances between layers and capacitance between the primary and the secondary winding were calculated straightforwardly by treating the layers as a cylindrical capacitor.

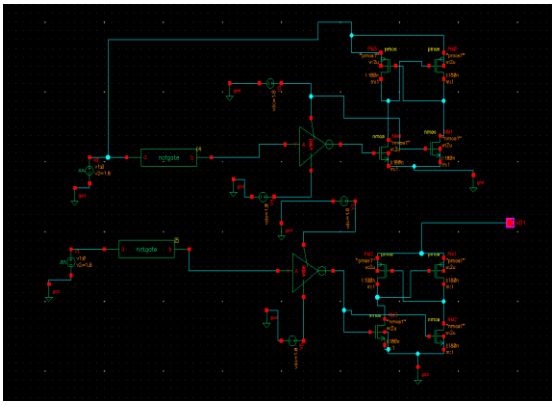

Fig.4. Baseband circuit for the converter operation

The capacitances to the ground are small in this case and are estimated at less than 1 pF. These are the capacitances from the layers to the core.We can see in Fig. 2 that only a part of the surface of the layers is at a short distance from the core and that it is mostly the geometry of the surface that influences the valueof . This is explained in Appendix B. Another method is based on the extension of the width of the layer halfway into the barrier on either side of the layer [4]. The capacitances to ground are the capacitances that govern the static voltage distribution. Fig. 5 shows the calculated static voltage distribution of eachlayer for a unit input voltage. When the ground capacitance is between 1 and 100 pF, the voltage distribution is more or less linear. The equivalent input capacitance in Fig. 4 is Baseband circuit for the converter operation approximately the same as the terminal phase-to-ground capacitance. The fact that the ground capacitances have a small value means that the phase-to-ground capacitance at the high-voltage side can be calculated as a series connection of the interlayer capacitances. Table shows the calculated interlayer capacitances.

Theequivalent value that results from these capacitances is 1.21 nF. The value of the phase-to-ground capacitance at the high voltage side is measured in two ways. An average value of 1.25 nF is measured by an impedance analyzer. The other method is the voltage divider method described in [13]. The transformerhigh-voltage winding is connected in series with a capacitor ofa known capacitance. A square impulse voltage is injected at theinput and the voltage is measured at both sides. The transformerphase-to-ground capacitance is determined with a voltage divisionformula. Applying this method, an average value of 1.14 nFwas measured.

Direct Current Component

To obtain the direct current component flowing into the converting transformer induced from the ac line, the total impedance of dc line circuit should be computed firstly, which includes the pole conductor self-impedance of dc line, the impedances of smoothing reactors at both ends of the dc line
and the internal impedance of converting equipment. Compared with the pole conductor self-impedance of dc line and the impedances of smoothing reactors, the internal impedance of converting equipment is very small and can be neglected. Therefore, the total impedance of dc line circuit can be approximated to the summation of the pole conductor self-impedanceof dc line and the impedances of smoothing reactors. For overhead pole conductor of the dc line, the per-unitlengthself-impedance can be calculated by Carson's model [9] accurately, but Carson's model is given by expressions withcomplex infinite integrals, which are very time-consuming to evaluate.

High-Voltage System

Thecurrent pulse from the left through the storageinductor and the fuse opening switch. As the

switch opens, avoltage is built up across the spark gap. A dielectric breakdownof the spark gap occurs and the voltage pulse (across theload) is sharpened. Before the pulse is dissipated in the dummyload, it passes a section where the voltage is measured. The primaryenergy storage was a 30-kJ pulsed power supply (PPS)having a capacitance of 67 F with a maximum voltage outputof 30 kV. The intermediate storage inductor was made of an8 mm copper tubing wound around a plastic core and has an inductanceof 3.5 H.

The opening switch in the vertical sectionconsists of several thin copper wires in parallel (electrically explodingopening switch, fuse switch). The spark gap containsan SF /air-mixture and is used as a closing switch. It consistsof two hemispherical rod ends with a 12.5-mm radius and a gapdistance of 4 mm. The load used during the power conditioningexperiments is a glass tube filled with a copper sulphate watersolution giving a resistance of 15 5. Polycarbonate discsseparate the different sections of the system.The typical performance of the system is shown in Fig. 3,where the storage inductor current and the load voltage are displayed[2]. For this case, the pulsed-power supply was chargedto 17 kV and the maximum load voltage was about 130 kV. Themaximum voltage that can be reached with the system is about150 kV and the voltage limit is constrained by flashover at thesection-separating discs in the T-shaped section.The transformer was introduced into the system accordingto Fig. 8. The connection to the capacitor bank was moved to other base band section.

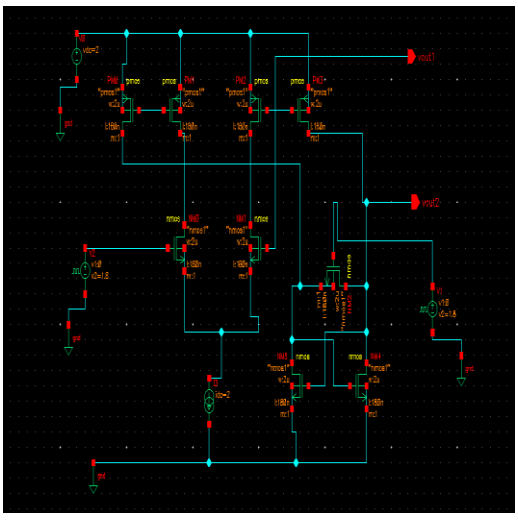

Fig.5. Narrow band circuit

Baseband Amplifier

The resulting baseband signal voltage over the output capacitance must be amplified and further filtered for secure level switching at the digitizer. This is performed by two amplifier stages connected in series (see Fig. 4). The stages are based on differential feedback cascode stages. Each stage amplifies about 30 dB (see Fig. 5) and they are not optimized for linearity. The output voltage dc-level from the last stage can be controlled by and may in turn control the bias point of a following digitizer.

SIMULATION AND RESULTS

The receiver was designed in a 180-nm CMOS process in Cadence virtuoso tool, with capacitors. No external components are used other than anetched transformer in the FR4 carrier PCB. The integrated circuitry is fitted within an area of around 20 mm^2 mand is hence suited to be used as an IP-block being placed ina die corner, or near the die edge, of a general ASIC. The totalcurrent consumption of the detector and baseband amplifier is2.3 A.Demodulation of the baseband signal is realized in Cadence for bit error rate (BER) measurement. Baseband sampling frequencyis 800 kHz and data is processed in sequences with alength of bits. For better precision several sequences areused. After being digitized the signal is normalized between 0and 1 and passed to a Schmitt-trigger. A following monostablemultivibrator secures a pulse-width of four samples.

Input Matching

The input matching of theWake-Up of radio was measured atthe transformer input terminal (see Fig. 5). Compared to simulationsthe frequency response was shifted 60 MHz upwards.

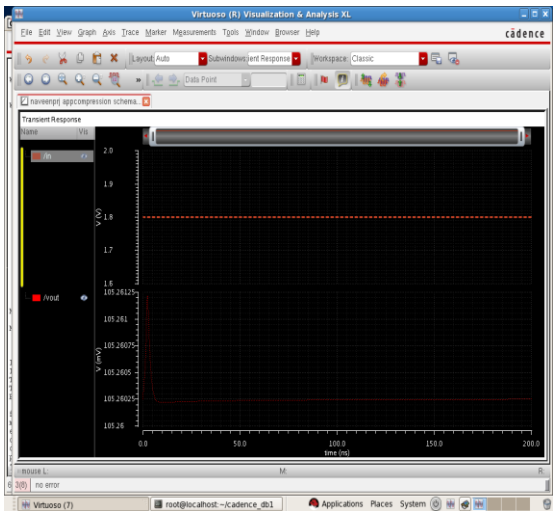

Fig.6. Transient response

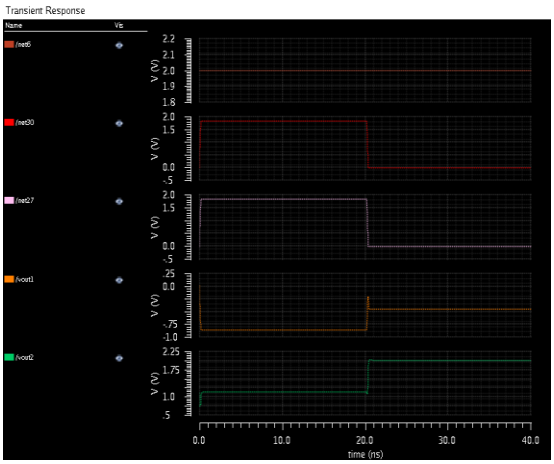

Fig.7. Transient response

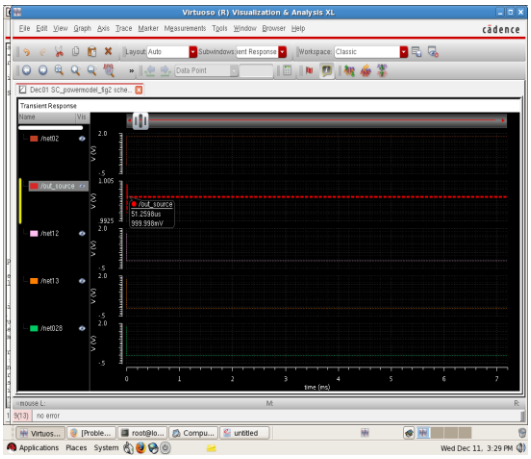

Fig.8. Transient response

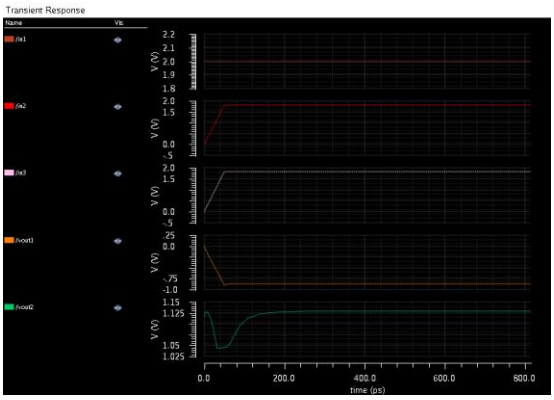

Fig.9. Transient response

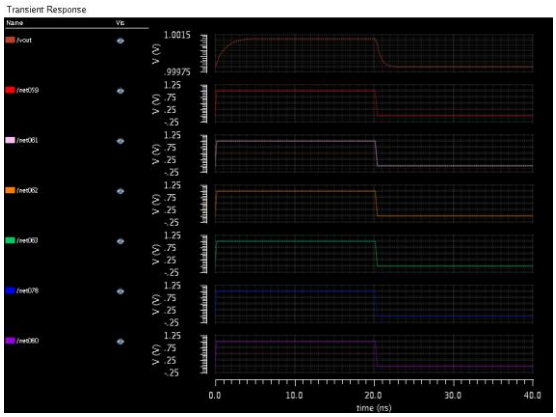

Fig.10. Transient response

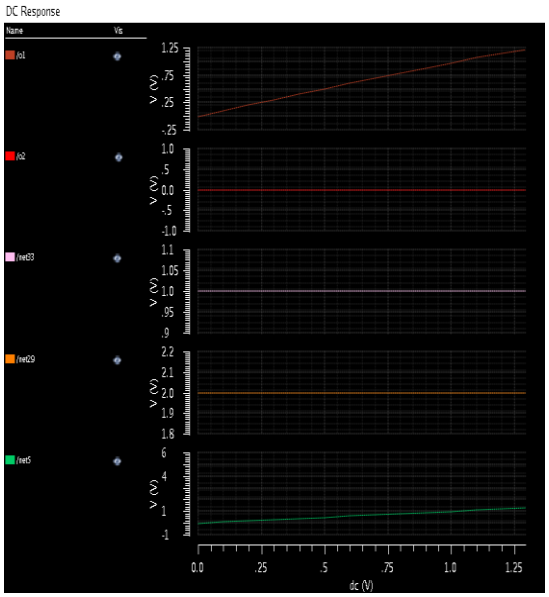

Fig.11. DC response

Aiming for a better sensitivity would require higher voltagetransformation ratio, higher detector transconductance (and currentconsumption), or the addition of an LNA between the transformerand the detector (also increasing current consumption).Higher voltage transformation ratio is difficult to achieve dueto limitations set by transformer and materials.Higher detector transconductance is very expensive in powerconsumption, as the transconductance needed is proportional tothe inverse square of power sensitivity and the currentconsumption is proportional to the transconductance. The additionof an LNA between the voltage transformer and the detectorcan be expected to improve the sensitivity with limitedpower consumption increase but at the cost of lower immunityto blockers (briefly discussed in [20]).In Table we compare the present design with recently publishedimplemented designswith power consumption below 400W. This comparison is not perfect; in some cases (includingthe present one), the digital power consumption is not included,and in others it is included. Still, we believe that the combinationof

dBm sensitivity and 2.3 W power consumption isthe best achieved until date. Designs with better sensitivity allconsume more than 20 times the power of the present one.

CONCLUSION

This modelling is appropriate for a design of the new envelope detector which we operate in the high efficient region. It is more efficient than the other process designs and to be operating in the very low power regions. The proposed design offers a robust and trim-free solution easily implemented in 180nm CMOS process designed in a Cadence Virtuoso tool.

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