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Low Power Consumption Of Full Adder Using A New Hybrid Cmos Logic

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ABSTRACT:

The design of full adder using a new hybrid-CMOS logic style is proposed. To achieve the low energy consumption, the new hybrid-CMOS logic style is used. The full adders are designed in an 180nm CMOS technology. The new Hybrid-CMOS logic style gives the desired performance. And we are classified the hybrid-CMOS logic full adders into three categories based on their structures. The many of the previously reported full adders suffered from the problems of low swing when operated at low supply voltages. The proposed New Hybrid CMOS full adder is operated at low supply voltage. The energy consumption is low compared to the conventional hybrid adders and provides better performance.

Keywords: Adders, Hybrid-CMOS logic style, low power, PDP.

I. INTRODUCTION

The necessity for portable electronics is driving designers to endeavour for smaller area, speed, battery life and more reliability. Digital circuits have power consumption dependent on process data that is, even small changes in the circuit switching can reveal the key data by measuring current consumption over repeated computations. Power and delay are important for the designer tries to save when designing a system. The most fundamental unit in circuits is full adder [1]. The data path consumes roughly 30% of the total power of the system [2] [3]. Adders are commonly used component in data path and hence design and analysis are required. The adders designed using several logic styles. Each design has its own performance. One example of such design is the static CMOS full adder [4]. The main drawback of static CMOS circuits is the existence of the PMOS transistors, because of its low mobility compared to the NMOS transistors. The large power dissipation occurs due to the presence of internal nodes and static inverters. The dynamic CMOS logic style provides a high speed and it has some problems such as charge sharing and lower noise immunity. In this paper we propose a new hybrid CMOS logic circuit to minimize the power. Power optimization for low power applications can be achieved at different levels such as system level, Architecture, and circuit level [5]. The main idea is to reduce the numbers of transistors in the adders and reduce the number of power dissipating nodes. This can be achieved by utilizing intrinsically low power consuming logic styles such as TFA or TGA or pass transistors. Their performance as a single unit is good but when we design a cascaded circuits, their performance degrades drastically [6], [7]. These problems can be overcome by inserting buffers in between stages to enhance the delay characteristics [8]. In this article, we propose new hybrid-CMOS full adder logic style.

The design of full adder circuits using conventional logic styles are summarized in sections II. The section III explains the new hybrid logic style. The simulation results of full adder design using conventional logic styles and proposed logic style are compared in section IV and finally it is concluded in section VI.

II. CONVENTIONAL FULL ADDERS

The different types of full adders are there. In this section we design the full adder circuits using static full adder, Complementary Pass transistor logic, 9-Tansistor hybrid CMOS logic, and Existing Hybrid CMOS logic. The static complementary CMOS logic is shown in figure.1. The output is connected to either Vdd or Gnd via low resistance path. It has high noise margin and low output impedance and high input impedance. The figure.2 shows the complementary CPL logic style Full adder circuit. This circuit consists of transistors that based on NMOS pass transistor network. This causes low input capacitance and high speed operation. CPL consumes less power that the static full adder.

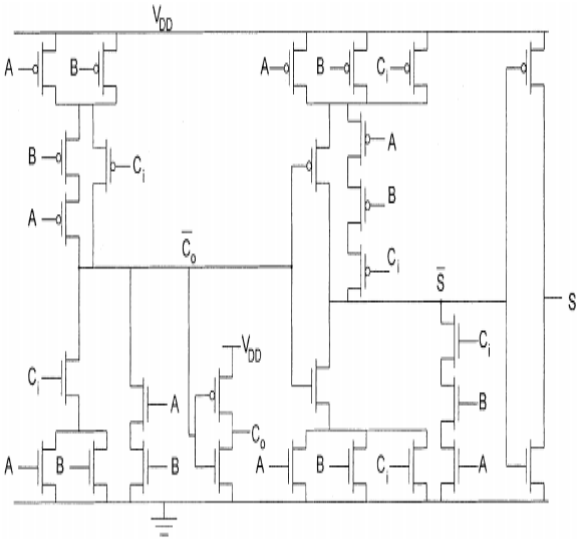

Figure.1 Static Full Adder

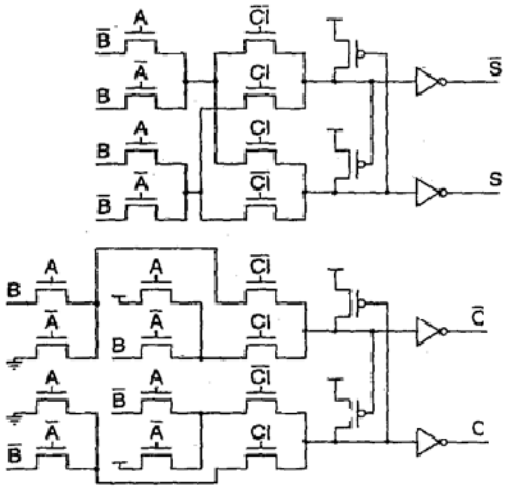

Figure.2 CPL Full Adder

The figure.3 shows the 9-Transistors Hybrid CMOS logic style Full adder circuit. The 9T Hybrid CMOS adder with 9 transistors consumes considerably less power in order of power and has speed. The 9T adder reduces the power compared to the static and CPL adders. The figure.4 shows the existing Hybrid CMOS logic style Full adder circuit. The circuit is consisting of 3 modules. The module1 is based on CPL. the module is fast due to the high mobility of NMOS transistors. The module2 consists of transmission gates and static logic to create SUM output. The module3 consists of XOR gate and an inverter.

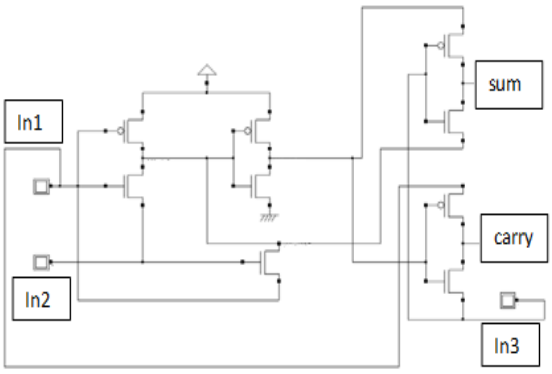

Figure.3 9T Hybrid CMOS Full Adder

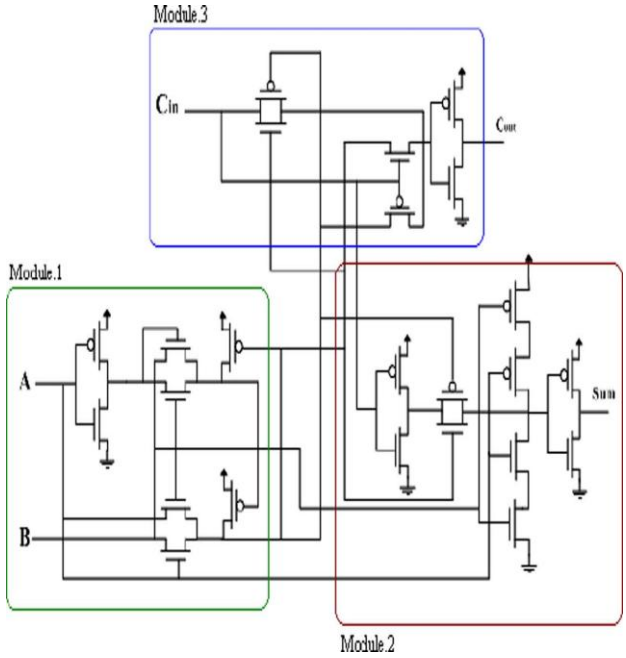

Figure.4 Existing Hybrid CMOS Full Adder

III. A NEW HYBRID CMOS LOGIC

The Figure.5 show the new Hybrid CMOS Full Adder circuit, in order to give the full-swing voltage at Sum and Cout, we are using ULPD (Ultra Low Power Diode) level restorer in the structure of the new hybrid full adder cell. The novel hybrid adder cell minimizes the static power consumption by eliminating any possible direct path between Vdd and the ground due to the use of NMOS and PMOS transistors in a complementary passion. By using this logic, when each part of the circuit is in the conducting mode, the other part is in the off situation, so there is no short-circuit current. And by using ULPD level restorer not only the leakage current is eliminated but also this capable device provides good

driving capability which is essential when this circuit is used in a cascaded or a more complex situation. Using ULPD as level restorer eliminates the need of output buffers which are the main source of static power consumption. This design uses 20transistors, due to the low switching capacitance, power dissipation of new hybrid CMOS logic is minimized. In terms of the power, speed, the new hybrid CMOS logic circuit is superior to the conventional full adder circuits.

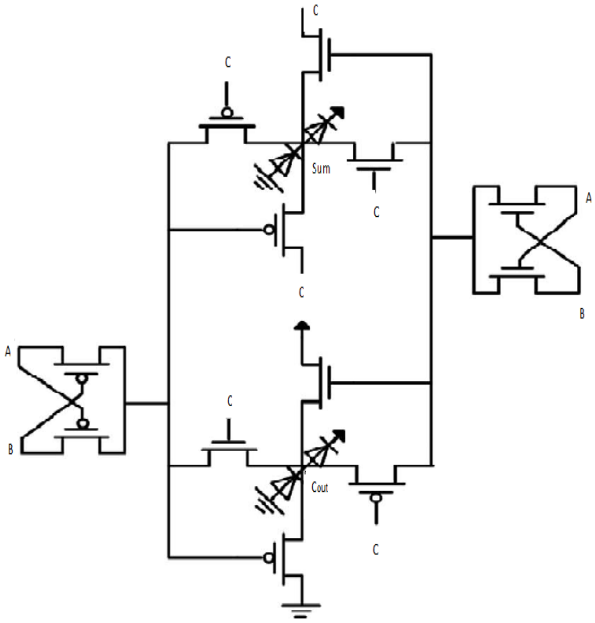

Figure.5 A New Hybrid CMOS Full Adder

IV. SIMULATION RESULTS

To assess the performance of the new hybrid CMOS Logic style, full adders are designed using the conventional and proposed logic styles in a 0.18-μm CMOS technology. The propagation delay, power consumption, and power-delay product of full adders are obtained at the supply voltage of 1.8 V. The conventional logic styles, such as static CMOS, and CPL, have an increasing delay as the supply voltage approaches the device threshold. The 9T hybrid CMOS logic, and existing hybrid logic provide not so much improvement on speed at low supply voltages. The new hybrid logic style has a significantly reduced propagation delay compared to the conventional logic styles. As for energy consumption, the new hybrid logic shows the better performance. Let V (A), V (B) and V(C) be the input V (sum) and V (carry) are output signals for the full adder. The simulated output waveform for full adder circuit using new hybrid CMOS logic style is shown in figure 6. Figure.7 and figure.8 show the comparison results of power and Power-Delay Product (PDP) respectively. The obtained simulation results for conventional and new Hybrid CMOS Logic Styles are summarized in Table.1.

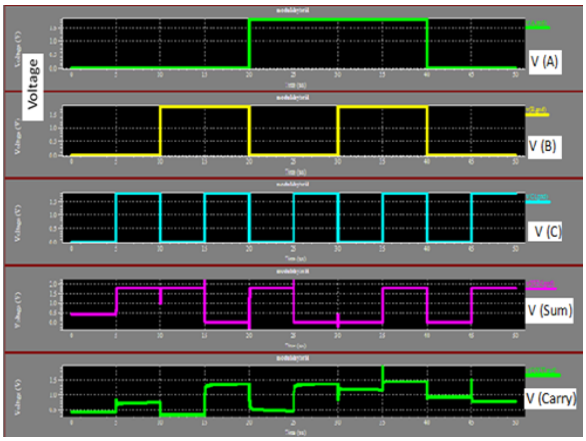

Figure.6 Full Adder waveform for new Hybrid CMOS Logic

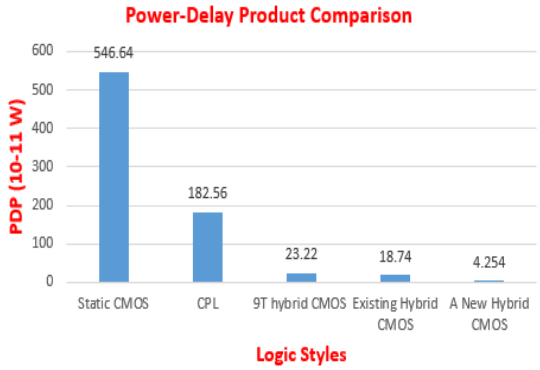

Figure.7 Power Comparison of various Logic

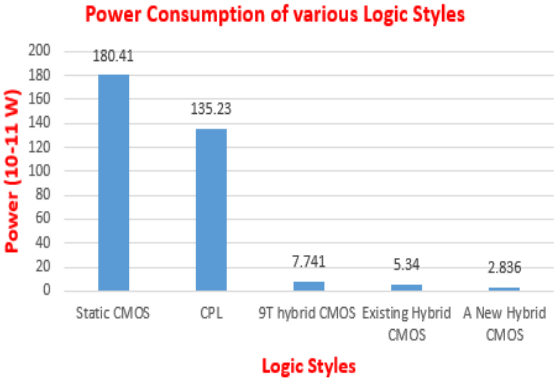

Figure.8 PDP Comparison of various Logic

Table.1 Comparison Results of Full Adder Using Conventional and New Hybrid Logic Styles

Parameters	Static CMOS	CPL	9T hybrid CMOS	Existing Hybrid CMOS	A New Hybrid CMOS
Power (10^{-11} W)	180.41	135.23	7.741	5.34	2.836
Delay(10^{-5} s)	3.03	1.35	3.0	3.51	1.5
PDP (10^{-16} Ws)	546.64	182.56	23.22	18.74	4.254

V. CONCLUSION

The full adder is designed using the conventional and new Hybrid CMOS logic styles. The simulated values of these logic styles are obtained using 0.18 µm CMOS process. The comparison results reveal that the power-delay product of new Hybrid CMOS logic style improved than the conventional, which indicates that the proposed logic family is well suited for applications in which speed performance must be maintained at low supply voltages. As for energy consumption, the new hybrid logic shows the better performance.

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