International Journal of Advanced Information Science and Technology (IJAIST) ISSN: 2319:2682
Vol.4, No.11, November 2015 DOI:10.15693/ijaist/2015.v4i2.442-445

Leakage Power Control Using Subclock Power Gating Technique

R.Parthasarathi[1], N.S. Nandhini[2], D.Ornica[3], S.Rajasurya[4]

[1] *Asst.prof Department of ECE, KLN College of Information Technology, Sivagangai Dt, Tamilnadu.*

[2, 3, 4] *Department of ECE, KLN College of Information Technology, Sivagangai Dt, Tamilnadu.*

Abstract**:** *In order to reduce the leakage power dissipation using an Nmos and Pmos at the header and footer to reduce the power and to improve the energy efficiency by using sub clock power gating technology. The proposed technique achieves power reduction through two mechanisms: 1) static power gating and 2) dynamic power gating technique. In this technique to achieve this reduced voltage, a pair of NMOS and PMOS transistors is used head and foot of the power gated logic. The sub clock power gating technique has been implemented full adder circuit, which was the fabrication process in 65 -nm. Two sets of experiments are done: the first experimentally validates all combinational logic gates in tanner and the second investigates the utility of the proposed technique in the example application. Measured results from the implementing adder shows 47% power saving during in active mode for all wireless sensor node applications.*

Keywords: *Active mode, leakage control, low power, power gating, subthreshold*

I.INTRODUCTION

LEAKAGE power can be as dominant as dynamic power below 65nm and poses a large source of power Consumption in digital circuits during active mode. When the digital circuit is doing useful work. A number of techniques have been processed for reducing active leakage power dissipation.

In this paper aim to reducing the active leakage power using some logic gates. The logic gate plays that the important role for all digital components. These include dual sub threshold logic. This uses high threshold voltage logic gates on non-critical timing paths and adaptive body biasing. This raises or lowers the threshold voltage of transistor for active power management. The effectiveness of power gating to Reduce leakage power has been demonstrated during active mode.We used a technique, called sub clock power gating (SCPG), targeted reach applications that demand low power Performance is not a primary concern.

This results from low performance operation at a fixed bed. Power reduction is achieved by power gating within the clock period to reduce leakage power during active mode. To generate this voltage, Dynamic power gating of both the power (Vdd) and ground (Vss) supplies is proposed and can be achieved through the use of both an **nMOS** and **pMOS** transistor at the head and foot of the power gated logic.It has implemented in full adder circuit, application oriented see to Full adder in carry look a head adder, ripple carry adder, carry select adder. In this works only the full adder using the combination of XNOR and XOR gates.

A. Related work

To use a dual threshold technique to reduce the power dissipation in Active mode power gating. This technique is only used for the CMOS Inverter. To connect the head and foot of the transistor to reduce the power[1]-[4]. A finer granularity power gating has been proposed in disabling executional units during active mode. A method of power gating part of multiplier depending on the data width during run time was proposed in. a guanularity akin to clock gating use the clock enable signal to power gate an integer execution core, in other hand to use the fan in logic. Rather than power gating the proposed technique provides a less than Vth voltage across the combinational logic to minimize power mode transition energy overheads.[5-9]. Therefore, development of power and efficient dual sub clock approaches which can work under such relaxed power constraints is highly desirable.

B .Proposed work

To achieve leakage power dissipation, there are two main tasks to be followed: our first technique is a static power gating and second technique is dynamic power gating using logic gates. In static method, the pair of nMOS and pMOS transistors is connected at the head of the circuit.This process is also called as reverse body bias. Body biasing has been londed considered as an effect and relatively easy way to compensate for some the process variations.

Not only does it leads to a tighter performance distribution and better yield, but also mitigating the guard band

requirements for process corners and temperature variation, it leads to better performance and faster design cycle.In the dynamic power gating method, a pair of nMOS and pMOS transistors are connected at the footer of the circuit. This process is known as a negative feedback method. Negative feedback occurs when some function of the output of a system, process, or mechanism is fed back in a manner that tends to reduce the fluctuations in the output, whether caused by changes in the input or by other disturbances.

C.Process

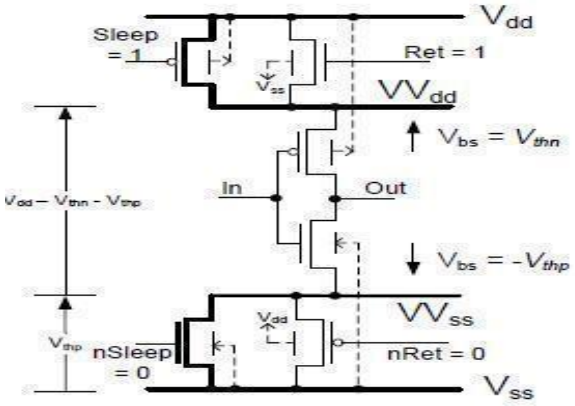

Fig. 1 CMOS inverter using Static and dynamic power gating

The CMOS Inverter circuit is designed by using of static and dynamic power gating .In this circuit,When it is in *Sleep* and *Ret* are logic 1 (and thus *n Sleep* and *n Ret* are logic 0) the *VV*dd is clamped to *V* dd − *V*thn and the *VV*ss is clamped to *V*ss + *V* thp. The result is a much more aggressive reduction in voltage across the power gated logic,but also has three advantages over single rail clamping.

When the clock is logic 1, ISOLATE is driven to logic 1, thereby isolating the combinational outputs. When the clock is logic 0, ISOLATE is held at logic 1 while the *VV*dd input remains at logic 0 (clamped) . This ensures the combinational outputs remain isolated until the supply rail is charged to an equivalent logic 1, eliminating short-circuit currents during wake-up. The use of a *VV*ss is unnecessary as the pairs of nMOS and pMOS transistors are assumed to be balanced to ensure equal voltage drop and charge/discharge times. The n-Override signal ensures that if the SCPG technique is disabled, additional dynamic power is not consumed by the isolation being activated in every clock cycle.

II. SCPG TECHNIQUE FOR UNIVERSAL GATES

A NAND gate circuit is designed by using Tanner EDA tool. In S-edit, the schematic for nand is to be drawn. This circuit is designed using a pair of nMOS transistor connected at the header.

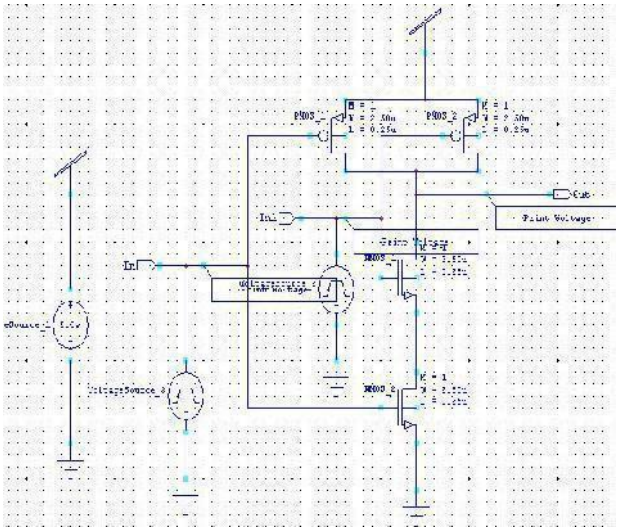

Fig. 2 NAND gate using static and dynamic logic

It will act as a reverse body biasing and to eliminate the leakage power. And a pair of pMOS connects at the footer to avoid negative feedback, these negative feedback current no sent the power in main circuit. So the unwanted leakage problem can be reduced. This process is fabricated in 65nm technology so area is not exceed.

The waveforms for NAND gates are found in W-edit and the power results are found in the T-spice, it displays the output measures of power.

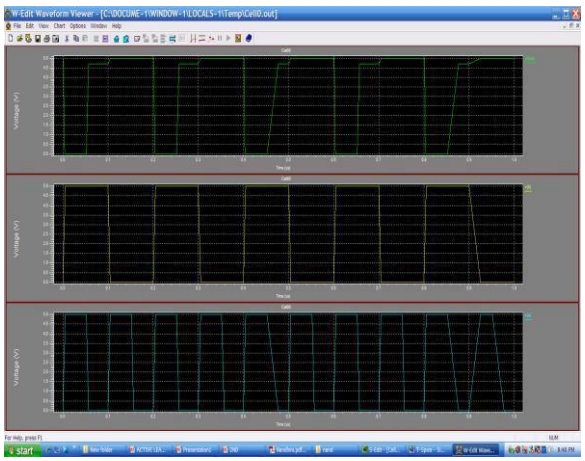

Fig. 3 NAND gate for static and dynamic logic waveform

We saw the output as leakage power reduction in high percentage. Therefore, we use the technique static and dynamic power gating to reduce the power and to increase the efficiency of the circuit.

III. COMPARISON TABLE FOR INVERTER and UNIVERSAL GATE POWER OUTPUT

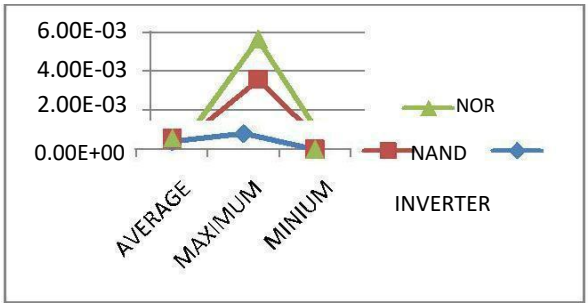

Fig. 4 Static Power Consumption

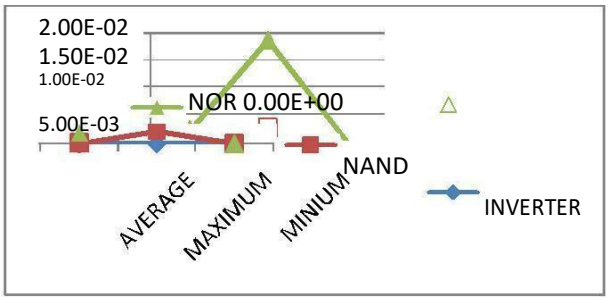

Fig. 5 Dynamic Power Consumption

IV. IMPLEMENTATION

The proposed dual SCPG technique has been proven by implementing the full adder circuit within a chip. The full adder circuit use in all digital circuits. The mostly used in circuit carry look ahead adder. In these circuits used high power and low performance. So reduce the power using this technique, the Parallel multipliers are well known building blocks used in digital carry look ahead adder. However, every multiplication can be replaced by shift and add operations. There are many types of adders but generally they can be divided into two main classes.

- Ripple carry adders (RCA)
- Carry look-ahead adders (CLA)

To connect the transistor in parallel and series order, final output shows that the pair of nMOS at the vdd and pair of pMOS connects at the Vss. In the formation of circuit used voltage is very low. In normal circuit, it consumes 5v-10v, but using of these techniques our required voltage is reduced to 2v-5v. so, we can achieve minimum leakage power and less power consumption and it also produces the output as more efficient manner.

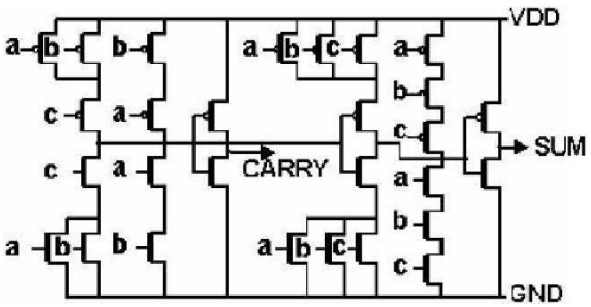

Fig. 6 CMOS Transistor using full adder

In a multiplier we are using parallel-series connections of full-adders. In the carry look ahead adder, that every full-adder is loaded with another full -adder.To connect the full adder in series from one full adder circuit output goes the next full adder and soon on.when choose for ripple carry adders means consists of power efficiency and compared to the other adder.A n bit ripple carry adder from 1 bit adders yields a propagation of the CARRY signal through the adder. Because the CARRY ripples through the stages, the SUM of the last bit is performed only when the CARRY of the previous section has been evaluated. Rippling will give some extra power overhead and speed reduction, but not changed, the ripple carry adders are the best in terms of power consumption. Hence, we get the total energy as a function of mean values of the basic energies of a full-adder FA.

SCPG with shutdown power gating has lower power consumption than without power gating but is higher than the proposed symmetric virtual rail clamping. This can be attributed to the high wake- up energy cost associated with the signal glitching that occurs when restoring the virtual rail in shutdown power gating. This high wake-up energy cost causes the energy overhead of shutdown, power gating to exceed the energy saving at all frequency points above 1 kHz, resulting in higher power consumption in comparison with no power gating. The increasing power trend of the shutdown, power gating mode is reversed after 20 kHz because the virtual rail does not discharge fully during shut down due to the shorter idle time within the clock period. However, despite the *VV*dd rail remaining partially charged at these frequency points, it still dissipates more power than the proposed symmetric virtual rail clamping technique and is a result of the combination of asymmetric Reverse body biasing of the logic gates and lack of charge recycling discuss, to reduce wake-up energy cost and improve the energy efficiency of the SCPG technique.We envisage the proposed SCPG with symmetric virtual rail clamping technique being applicable in a range of general purpose, low performance, energy-constrained application. The sub clock power gating thechnology used carry look ahead adder add one to nine, to exceed nine not work on this paper,so in this implementation only the one digit number, to add the two numbers result less than or equal to nine.

V. CONCLUSION

This paper has proposed a power gating technique that reduces leakage power during the active mode for low performance, energy-constrained applications with power gating combinational logic within the clock period. Rather than shutting down completely, symmetric virtual rail clamping was proposed to reduce wake-up power mode transition energy cost. The proposed SCPG with symmetric virtual rail clamping technique has been implemented full adder circuits, fabricated in 65-nm technology. To reduce the average power by up to 67% during the active mode, SCPG can achieve a 47% reduction in power and improvements in energy efficiency. It avoids increased design complexity, making it fully compatible with standard EDA tool.

ACKNOWLEDGEMENT

The authors would like to thank the anonymous reviewers for their valuable comments and helpful suggestions.

REFERENCES

[1] A. Agarwal, S. Mukhopadhyay, A. Raychowdhury, K. Roy, and C. Kim,"Leakage power analysis and reduction for nanoscale circuits," *IEEEMicro*, vol. 26, no. 2, pp. 68–80, Mar./Apr. 2006.

[2] L. Wei, Z. Chen, K. Roy, M. Johnson, Y. Ye, and V. De, "Design and optimization of dual-threshold circuits for low-voltage low-power application0s," *IEEE Trans.* vol. 7, no. 1, pp. 16–24, Mar. 1999.

[3] N. Mehta and B. Amrutur, "Dynamic supply and threshold voltage scaling for CMOS digital circuits using in-situ power monitor," *IEEE Trans.* vol. 20, no. 5, pp. 892–901,May 2012.

[4] Z. Hu, A. Buyuktosunoglu, V. Srinivasan, V. Zyuban, H. Jacobson, and P. Bose, "Microarchitectural techniques for power gating of execution units," in *Proc. ISLPED*, Aug. 2004, pp. 32–37.

[5] K. Usami, M. Nakata, T. Shirai, S. Takeda, N. Seki, H. Amano, and H. Nakamura, "Implementation and evaluation of fine-grain run-time power gating for a multiplier," in *Proc. IEEE ICICDT*, May 2009,pp. 7–10.

[6] J. W. Tschanz, S. G. Narendra, Y. Ye, B. A. Bloechel, S. Borkar, and V. De, "Dynamic sleep transistor and body bias for active leakage power control of microprocessors," *IEEE J. Solid-State Circuits*, vol. 38, no. 11, pp. 1838– 1845, Nov. 2003.

[7] J. Seomun, I. Shin, and Y. Shin, "Synthesis of active-mode powergating Circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 31, no. 3, pp. 391–403, Mar. 2012.

[8] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. Das, W. Haensch, E. Nowak, and D. Sylvester, "Ultralow -voltage minimum-energy CMOS," *IBM J. Res. Develop.*, vol. 50, nos. 4–5,pp. 469–490, Jul. 2006.