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Leakage Current Reduction on Different SRAM Cells Used Adaptive Voltage Level Technique

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Abstract: In this paper, a novel 8T and 9T cells compared to conventional Schmitt trigger SRAM cell is proposed that reduces the gate leakagepower. To reduce the sub-threshold leakagepower further, an adaptive voltage level (AVL) circuit is added to this cell, which controls the effective voltage across the SRAM cell in inactive mode. High leakage currents in deepsubmicron regimes are becoming a major provider to total power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled.The channel length of the MOSFET reduces the leakage current in the SRAM increases. To reduce the sub-threshold leakage power further, an adaptive voltage level (AVL) circuit is added to this cell, which controls the effective voltage across the SRAM cell in inactive mode. Two schemes are employed; one in which the supply voltage is reduced and the other in which the ground potential is increased. Cadencevirtuoso are performed with 180nm CMOS technology process file and the leakage currents of all the cells are measured and compared. Results revealed that there is a significant reduction in leakage current for this proposed cell with the AVL circuit reducing the supply voltage.

Key words: Leakage power, SRAM, leakage reduction techniques.

I. INTRODUCTION

The supply voltage must be reduced such that leakage current can be kept at reasonable levels and power delivery can still be performed within the functional requirements. Though, as a result of scaling, power dissipation due to leakage currents has also increased dramatically and is a major source of concern especially for low power applications. This paper introduces how to control the leakage current in SRAM cell and optimizes the power.

The principal of leakage mechanism has been due to drain source sub-threshold current. With scaling of power and delay also needs to be scaled to maintain proper operation of MOS transistor. Assuming this leakage mechanism, a number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-VDD scheme, Dual-Vth SRAM etc. The magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than the sub-threshold leakage for future CMOS devices[1]. Of the several techniques which have been proposed to reduce sub-threshold leakage in SRAM cells, use of a Adaptive Voltage Level (AVL) which allows full supply voltage to be applied in active mode and reduced supply voltage in inactive mode appears to be particularly promising for reducing gate leakage currents as well. An AVL can be used either to reduce the leakage current to the SRAM cell. while a technique similar to use of AVL for raising the ground potential has already been reported to yield significant reduction in gate leakage currents. So, in this work, in order to suppress the leakage further, the proposed SA cell combined with adaptive voltage level (AVL) circuit either at the ground node (referred as AVLG) or the supply node (referred as AVLS) is simulated and its leakage characteristics are analyzed.

The paper is organized as follows. Section II describes the conventional basicSRAM cell. Section III describes the SRAM cell and its working. and its effect on leakage reduction. Section IV describes the AVLG circuit in SRAM cell and its effect on leakage reduction. Section V describes the AVLS circuit in SRAM cell and its effect on leakage reduction. Section VI gives the simulation results and discussion. Section VII gives the conclusion.

II. Basic SRAM Cell

A basic SRAM cell has 6 transistors as shown in Figure. Transistors M1, M2, M3 and M4 comprise apair of cross-coupled CMOS inverters that use positive feedback to store a value. Transistors M5 and M6 are two pass transistors that allow access to the storage nodes for reading and writing. To write a value into an SRAM cell, the new value and its complement are driven on the bit lines, and then the word line is raised. The new value will overwrite the old value, since the bit lines are actively driven by write circuitry[2] [3]. To

read a value from an SRAM cell, the bit lines are pre-charged high and then the word line is raised turning on the pass transistors. Because one of the internal storage nodes is low, one of the bit lines starts discharging[8].

A sense amplifier which is connected to the bit lines senses which of the bit lines is discharging and reads the stored value. The sizing of the transistors in SRAM cell should be done carefully for proper operation of SRAM. The leakage currents in SRAM vary within a clock cycle depending on the phase of the operation being performed, since different transistors would be in off state during different operations

III.WORKING OF SRAM CELLS

A.8T SRAM CELL

Fig 1 shows the architecture of new 8T SRAM cell. It consists of two extra transistors MNLL and MNWL as compared to conventional 6T SRAM cell.

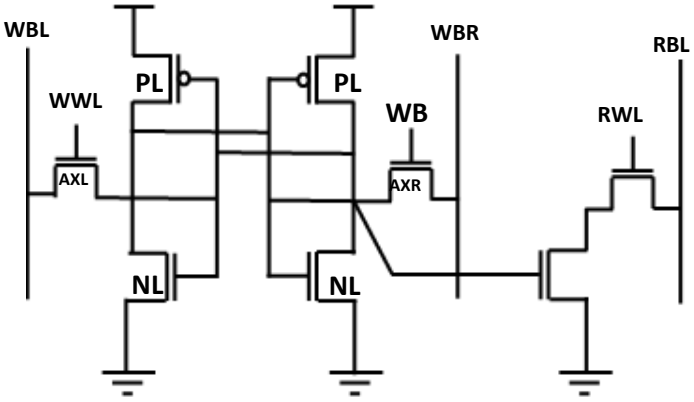


Fig .1. Schematic of 8T SRAM cell

Transistor MNLL is used to reduce gate leakage while transistor MNWL is used to make cell SNM free in the zero state. Interestingly, transistor MNLL also helps in improving SNM when cell holds logic '1'. The signal WLB is the complement of word line (WL) signal. 8T transistor consist of 8 transistor-2 PMOS and 6 NMOS. In this work, the basic read/write operations of 8T SRAM cell are performed using single ended sense amplifier.

In write '0' operation, the bit-line BT is pulled down to logic '0'.As soon as the signal WL rises from logic '0'to logic '1', transistor MNWL is turned off. The node XT starts discharging which turns on bit-line BB is pulled down to-VTN, where VTN is the threshold voltage of transistor MN4 [4]. The node XB starts discharging which turns on transistor MP1. Once transistor MP1 is turned on, the node XT is at logic '1' and hence logic '1' is written into the cell. In read operation, the bit-lines BT and BB are held at logic '1' by the pre-charged circuitry. In read'0' operation, the bit-line BT starts discharging through transistors MN3 and MN1. The single ended sense amplifier [4] gives output as logic '0' when bit-line BT falls below a certain threshold voltage from logic '1'. In read '1' operation, the bit-line BT remains at logic '1' because storage node XT is at logic '1' and hence single ended sense amplifier output remains at logic '1'. During read '1' operation, transistors MNWL and MP2 are turned off. For this scenario, the retention time for holding logic '0' at node XB is calculated given by equation t=C.dV/I, Where C is the total capacitance at node XB, dV is the threshold voltage of transistor MN1 and I is the leakagecurrent through transistor MP2 respectively.

In standby mode, where the cell is in zero state, the transistor MNLL enters cut-off as its source voltage is at VDD-VT, resulting in reduced direct tunnelling leakage through transistor MN1. The voltage at the storage node is not affected by the design in zero state. However, the trans-conductance of transistor MN1 has been reduced which may affect the performance of the cell as discussed in section simulation results [5]. When cell is holding logic '1' in the standby mode, the transistor MNLL serves as a good conductor of logic'0'[5]. Since transistor MNWL is on in standby mode, for this case the functioning of cell is same as the conventional 6T SRAM cell except transistor MNWL and MNLL. In this case where cell holds logic '1', both the transistors MNLL and MNWL are the extra sources of direct tunneling leakage.

B.9T SRAM CELL

9T-SRAM cell is shown in Fig.2.To save the power during write operation, a tail nMOS transistor N7 is connected in the pull-down path of one of the inverter. Our proposed circuit is similar to ZA cell with some difference. The main difference is that in the proposed circuit, gate of tail transistor N7 is connected to bit line BL instead of extra signal WS as in case of ZA cell .This arrangement saves area on the chip as well as timing conflict in between WS and

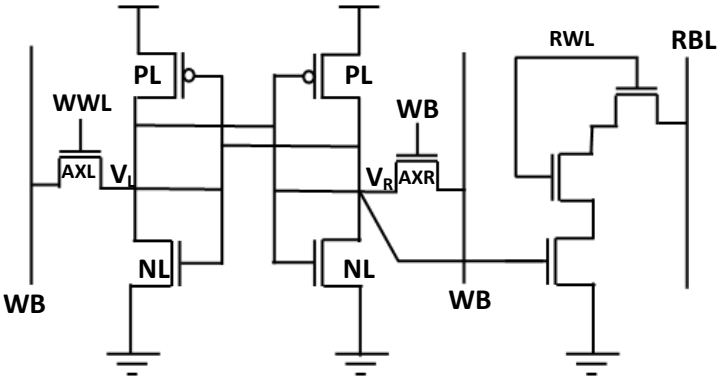


Fig .2. Schematic of 9T SRAM cell

write-word line (WWL). An extra nMOS transistor N6 is connected in between two inverters so that during read operation cell behaves as conventional 6T SRAM cell. Switching activity of this transistor is controlled by read word line (RWL). Due to transistor N6, effective resistance of the pull down path of inverter is reduced compared to ZA cell and results in lower read power consumption. Read operation is performed through access transistor N5 and RBL bar. Now we will explain write/read operation in detail

C.ST-1 Bitcell

Fig. 3 shows the schematics of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-

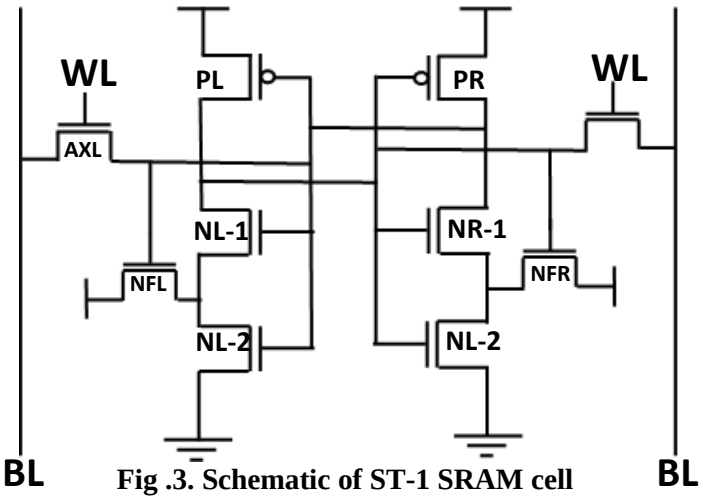


Fig .3. Schematic of ST-1 SRAM cell

line (WL), and two bitlines (BL/BR). Transistors PL-NL1-NL2- NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the input transition giving the ST action. Detailed operation of the ST-1 bitcell can be found in [10].

D.ST-2 Bitcell

Fig. 4 shows the schematics of the ST-2 bitcell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bitlines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF . In the ST-2 bitcell, feedback is provided by separate control signal (WL) unlike the ST-1 bitcell, where in feedback is provided by the internal nodes. In

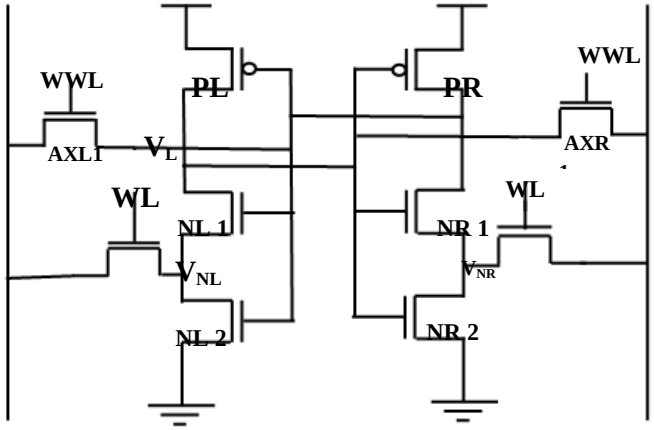


Fig .4. Schematic of ST-2 SRAM cell

the ST-1 bitcell, the feedback mechanism is effective as long as the storage node voltages are maintained.

The storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Detailed operation of the ST-2 bitcell is explained in our earlier work .

An Adaptive Voltage Level (AVL) Control Circuit

An adaptive voltage level control circuit can be used either at the upper end of the cell to reduce supply voltage (AVLS scheme) or at the lower end of the cell to raise the potential of the ground node (AVLG scheme). The impact of these two techniques on leakage currents is described in this section.

VI. LEAKAGE CONTROL USING AVLG

A.8T SRAM CELL

Fig. 5 represents the schematic of 8T SRAM cell using AVLG technique. The switch provides 0 Volt at the ground node during the active mode and a raised ground level (virtual ground) during the inactive mode [7]. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M1 and also the gate drain voltage of transistor M2, which results in a sharp reduction in gate leakage currents of

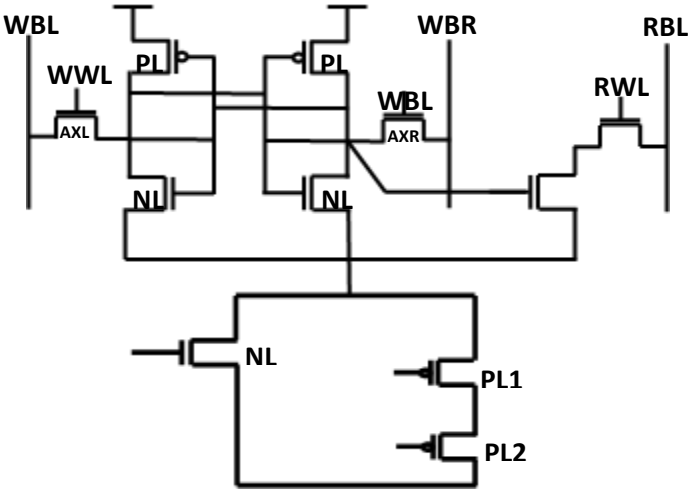


Fig .5. Schematic of 8T SRAM cell with AVLG

these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to increase in drain voltage of M1.

Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the AVLG switch. Although only one transistor is normally used for one bank of SRAM cells, leakage current through it is not necessarily negligible because its size has to be much larger than NMOS transistors within the SRAM cell to avoid performance degradation in the active state. As far as sub-threshold leakage currents are concerned, AVLG approach is successful in reducing currents through M3, M2 and M5 as wel [9] [10]l. To summarize, all sub-threshold currents are reduced using AVLG approach, it is only partially successful in reducing gate leakage currents.

B.9T SRAM CELL

Fig.6. is the schematic of 9T SRAM cellusing AVLG technique. The switch provides zero Volts at the ground node during the active mode and a raised ground level during the inactive mode. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M1 and also the gate

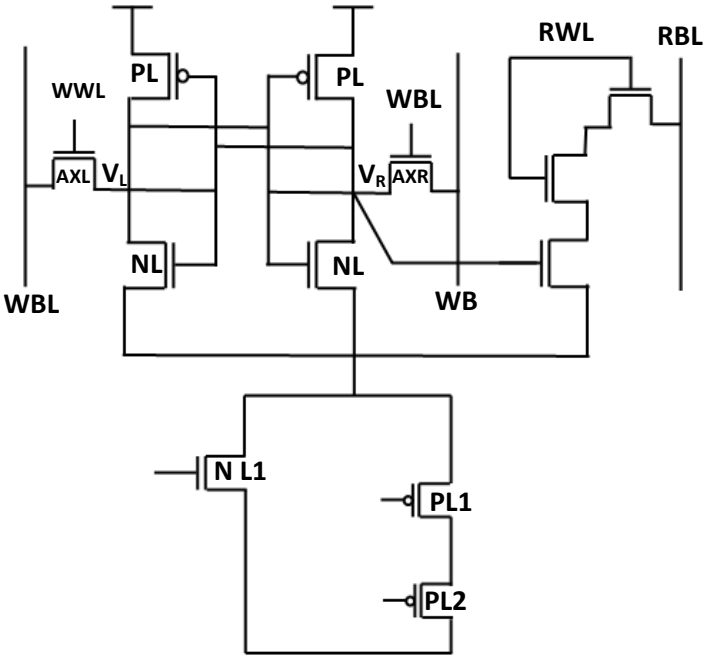


Fig .6. Schematic of 9T SRAM cell with AVLG

drain voltage of transistorM2, which results in a sharp reduction in gate leakage currents of these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to increase in drain voltage of M1. SRAM cells, leakage current through it is not necessarily negligible because its size has to be much larger than NMOS transistors within the SRAM cell to avoid performance degradation in the active state. As far as sub-threshold leakage currents are concerned, AVLG approach is successful in reducing currents through M3, M2 and M5 as well. Again M7 and M8 some improvement of the leakage current , M9 to use cross couple method its work on ultra low voltage. To summarize, all sub-threshold currents are reduced using AVLG approach, it is only partially successful in reducing gate leakage currents.

C.ST-1 Bitcell

Fig.7. is the schematic of ST-1 SRAM cell using AVLG technique. The switch provides zero Volts at the

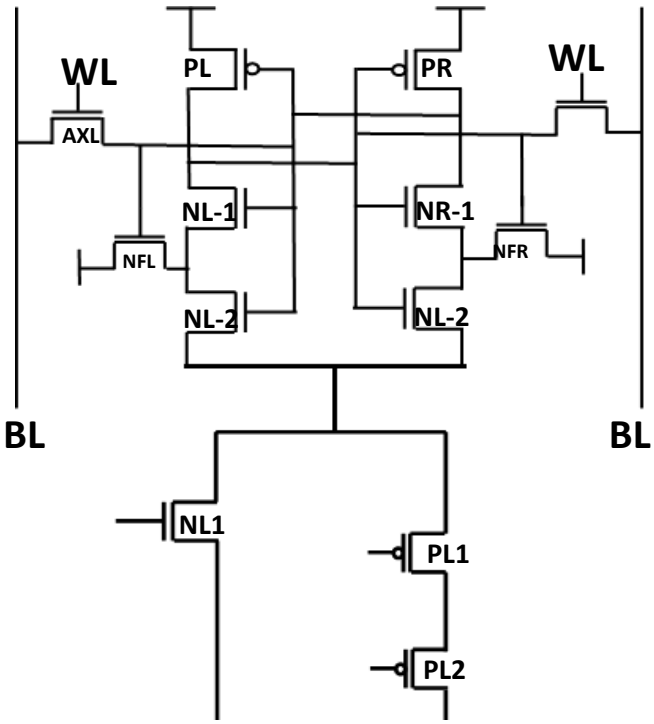


Fig .7. Schematic of 9T SRAM cell with AVLG

ground node during the active mode and a raised ground level during the inactive mode. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M1 and also the gate drain voltage of transistor M2, which results in a sharp reduction in gate leakage currents of these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to increase in drain voltage of M1. As far as sub-threshold leakage currents are concerned,AVLG approach is successful in reducing currents through M3, M2 and M5 as well. Again M7 and M8 some improvement of the leakage current, M9 to use cross couple method its work on ultra lowvoltage. To summarize, all sub-threshold currents are reduced using AVLG approach, it is only partially successful in reducing gate leakage currents.

D.ST-2 Bitcell

Fig.8. is the schematic of ST-2 SRAM cell using AVLG technique. The switch provides zero Volts at the ground node during the active mode and a raised ground level during the inactive mode. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor M1 and also the gate drain voltage of transistor M2, which results in a sharp reduction in gate leakage currents of these two transistors. There is no improvement in gate leakage currents of transistors M5 and M6. But an additional gate leakage appears in transistor M5 due to increase in drain voltage of M1. As far as sub-threshold leakage currents are concerned, AVLG approach is successful in reducing currents through M3, M2 and M5 as well. Again M7 and M8 some improvement of the leakage current, M9 to use cross couple method its work on ultra low voltage. To summarize, all sub-threshold currents are reduced using AVLG approach, it is only partially successful in reducing gate leakage currents.

V. LEAKAGE CURRENT USING AVLS

A.8T SRAM CELL, 9T SRAM CELL

An 8T SRAM cell incorporating AVLS scheme is shown in Figure 8. In this scheme, a full supply voltage of VDD is applied to SRAM in active mode while a reduced supply voltage of VD is applied in inactive mode. Since transistor M4 is in ON state, the drain voltages of transistors M2 and M1 are also at V_D. As a result of a decrease in gate voltage of transistor M1, gate leakage current through it is sharply reduced.

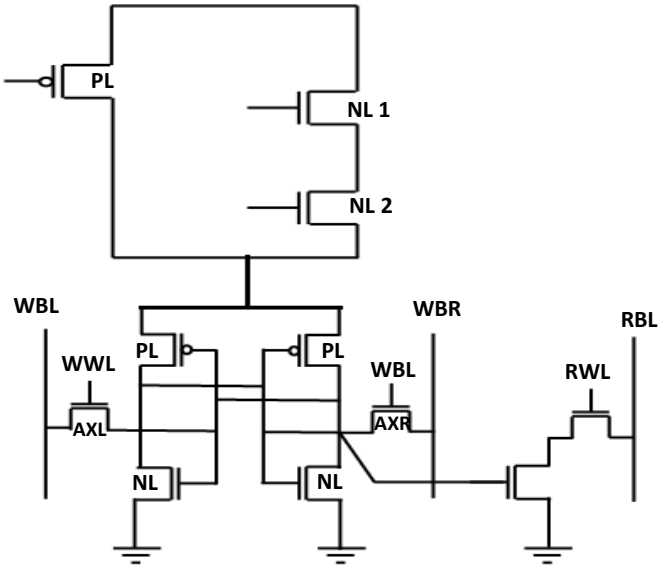


Fig .8. Schematic of 8T SRAM cell with AVLS

A decrease in drain voltage of transistor M2 results in lower gate-drain voltage across it and thus gate leakage current through it is also reduced. The gate

leakage through transistor M5 remains unchanged. As far as the subthreshold leakage currents are concerned, they are reduced in transistors M2 and M3 but remain unaltered in M3.

A decrease in source voltage of M6 results in a decrease in one component of EDT leakage across it while leaving the other unchanged. Gate leakage across transistor M5 remains unchanged. Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in AVLS circuit. One thus sees that AVLS scheme has a better impact on gate leakage current reduction than the AVLG scheme. To summarize, the AVLS approach, while more successful in reducing gate leakage current, still leaves two gate leakage current components in access transistors unaltered. It also leaves one sub-

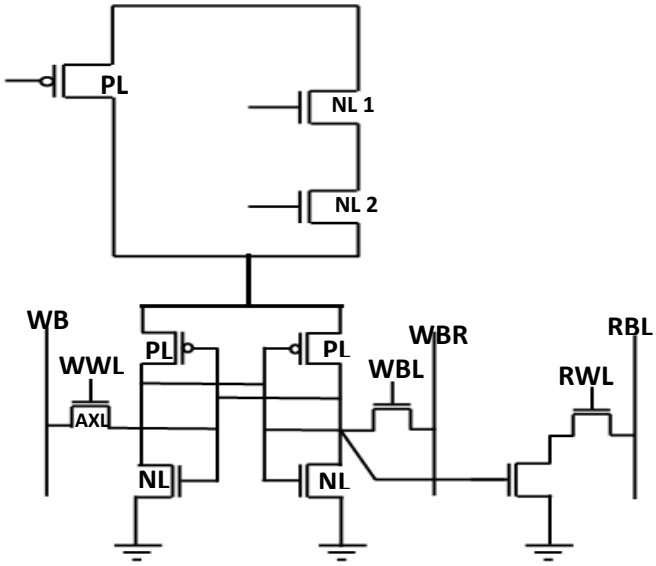


Fig .9. Schematic of 9T SRAM cell with AVLG

threshold current component in access transistor unchanged and results in an additional sub-threshold leakage current across the other access transistor.

B.ST-1 Bitcell& ST-2 Bitcell

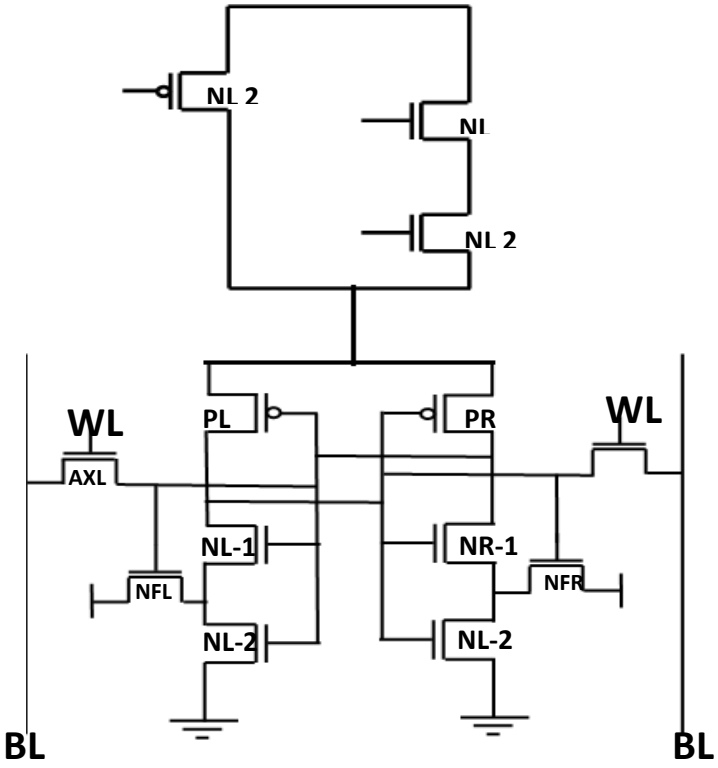


Fig .11. Schematic of ST-1 SRAM cell with AVLS

An ST-1 SRAM cell incorporating AVLS scheme is shown in Figure 4. In this scheme, a full supply voltage of V_{DD} is applied to SRAM in active mode while a reduced supply voltage of V_D is applied in inactive mode. Since transistor M4 is in ON state, the drain voltages of transistors M2 and M1 are also at V_D. The gate leakage currents of transistors M1 and M2 get reduced due to the decrease in their gate-source and gate-drain voltages respectively.

A decrease in source voltage of transistor M6 results in a decrease in gate leakage through it. The gate leakage through transistor M5 remains unchanged. As far as the subthreshold leakage currents are concerned, they are reduced in transistors M2 and M3 but remain unaltered in M3.

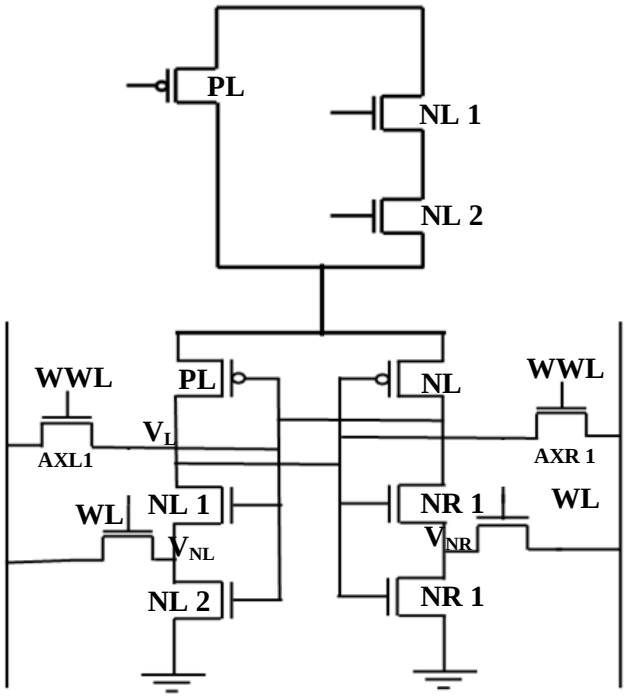


Fig .12. Schematic of 9T SRAM cell with AVLG

VI. SIMULATION RESULT

The leakage currents in the conventional and the schemes suggested in this section. Simulation results are simulated on the 180nm CADENCE tool with a nominal supply voltage 2 volt. The gate leakage being the only dominant

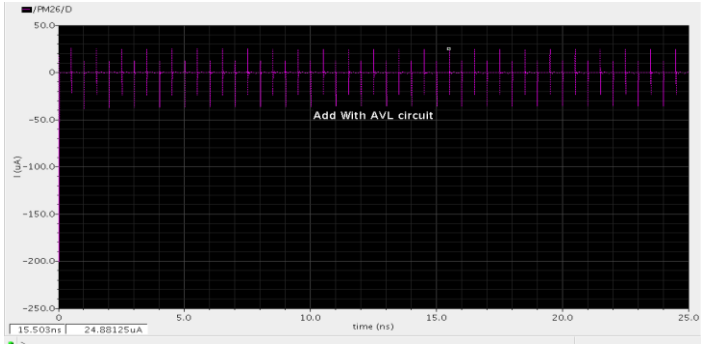
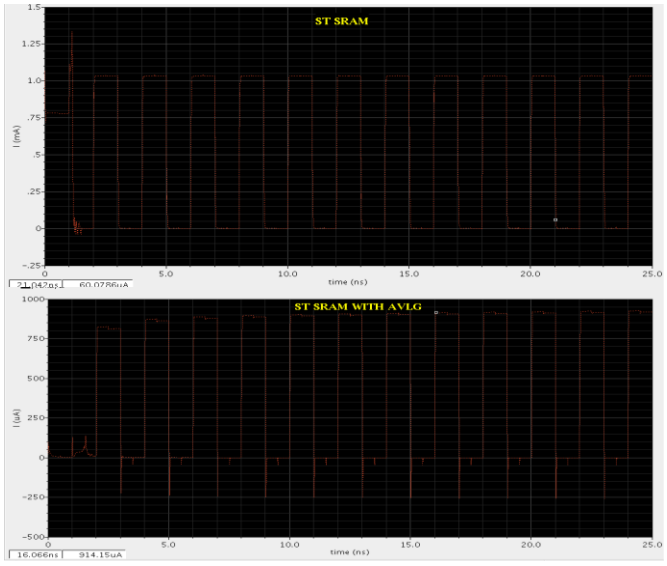


Fig .13. Simulation output 9T SRAM cells

It was observed that the scheme using supply voltage reduction is more efficient than the one raising the ground potential. 96% reduction in the leakage current was achieved without significant performance loss in ST cell with AVLS compared to 8T & 9T, but with a little area overhead. By making the bit lines floating in the cell 8T& 9T with AVLS. Mechanism at room temperature, AVLG scheme suppresses the total leakage of 9T by 14%, while AVLS scheme without changing bit-line voltages provides a leakage reduction of 15% Where as total leakage of 8T reduces by 13% in AVLG scheme, while AVLS scheme without changing bit-line voltages provides a leakage reduction of 22%.



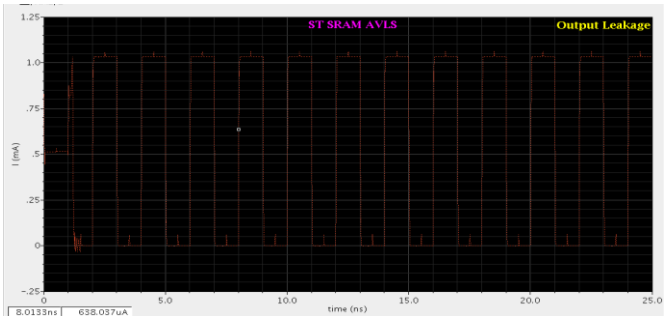


Fig .14.Simulation output ST

TABLE I: Leakage current of 8T SRAM

Reduction Technique	Voltage	Leakage current
8T SRAM Cell	2v	113.3µA
AVLG	2v	88.762 µA
AVLS	2v	22.881 µA

TABLE II: Leakage current of 9T SRAM

Reduction Technique	Voltage	Leakage current
9T SRAM Cell	2v	125.326µA
AVLG	2v	73.132µA
AVLS	2v	24.881 µA

TABLE III: Leakage current of ST-1 SRAM

Reduction Technique	Voltage	Leakage current
ST-1 SRAM Cell	2v	956.326µA
AVLG	2v	814.15µA
AVLS	2v	638.03µA

TABLE IV: Leakage current of ST-2 SRAM

Reduction Technique	Voltage	Leakage current
ST-2 SRAM Cell	2v	656.58µA
AVLG	2v	563.99 µA
AVLS	2v	335.70 µA

VII. CONCLUSION

A novel SRAM cell was proposed that offers reduced gate leakage currents in caches. The novel SRAM design exploits the fact that most of the bits stored in caches are zeroes. Simulation results show that 61% reduction in the total leakage currents was achieved at 27°C with marginal degradation in the performance compared to the conventional 8T cell. Two schemes: a) raising the ground level and b) decreasing the supply voltage to the SRAM cell during inactive mode to suppress its leakage currents were also examined in detail. It was observed that the scheme using supply voltage reduction is more efficient than the one raising theground potential.

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