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Implementation Of 64x64 Vedic Multiplier Using Urdhva Tiryagbhyam Technique

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ABSTRACT:

This paper deals with 64X64 bit multiplier using "URDHVA TIRYAGBHYAM"sutra multiplication technique.Multiplier plays a major role in digital signal processing systems.To achieve high speed operation ,Vedic method has been adopted in VLSI technology.Multipliers using vedic mathematics produces high evaluation results in terms of speed and device utilization as compared with earlier multiplier architecture.This multiplier was implemented using 32X32 bit vedic multiplier.The 32x32 vedic multiplier module using urdhva tiryagbhyam sutra uses four 32X32 vedic multiplier modules, three 64 bit ripple carry adder . the 32X32 vedic multiplier is coded in verilog HDL,synthesized and simulated using Xilinx ISE 10.1 software .This multiplier is implemented on spartan3 FPGA device XCS4000L-5pq208.

keywords: Urdhva tiryagbhyam,vedic multiplier,vedic maths.

INTRODUCTION:

Vedic Mathematics is the name given to the ancient Indian system of calculations. .

The meaning of the Sanskrit word„Veda" is knowledge [2]. Vedic mathematics is based this sixteen principles or formulas known as Sutras. Vedic Sutrascan be applied to almost every field of mathematics [3]. Thebeauty of Vedic mathematics is that its algorithms are designed in the same way as a human mind works. It can be used to transform the tedious calculations into simpler and orally manageable operation without much help of pen and paper.The Vedic system is interrelated and unified so that the simple multiplication methods can easily be reversed to allowone-line divisions, and the basic squaring method can easily bereversed to get one-line square roots.

Vedic mathematics or ancient mathematics is a unique technique of calculations based on 16 sutras.These Sutras along with their brief meanings are enlisted below alphabetically.

1) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2) Chalana-Kalanabyham – Differences and Similarities.
3) Ekadhikina Purvena – By one more than the previous one.
4) Ekanyunena Purvena – By one less than the previous one.
5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6) Gunitasamuchyah – The product of the sum is equal to the sum of the product

7) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
8) Paraavartya Yojayet – Transpose and adjust.
9) Puranapuranabyham – By the completion or noncompletion.
10) Sankalana-vyavakalanabhyam – By addition and by subtraction.
11) Shesanyankena Charamena – The remainders by the last digit.
12) Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14) Urdhva-Tiryagbyham – Vertically and crosswise.

15) Vyashtisamanstih – Part and Whole.

16) Yaavadunam – Whatever the extent of its deficiency.

In the field of engineering most of the researcher are using following sutras, we will describe them briefly:
i) Nikhilam navata charanam Dashatah,
ii) Urdhva-tiryakbyham.

Vedic multiplication using Vedic multiplier:

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit Of the final product. The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier . Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier‟s efficiency. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier.

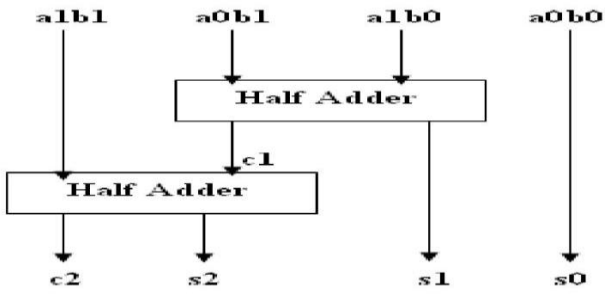


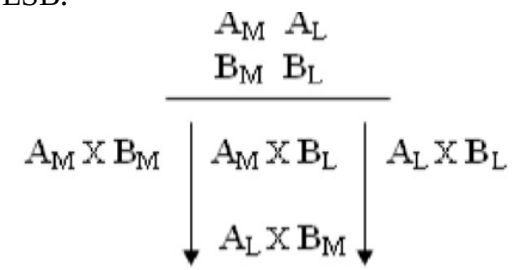
fig 2:Gate level diagram for 2 bit using using Urdhva tiryagbhyam technique

fig 1:two bit number vedic multiplication

Generalized Algorithm for N x N bit Vedic Multiplier We can generalize the method as discussed in the previous sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2N) *A* and *B* where A = AN.....A3 A2 A1 and B = BN….B3 B2 B1. The

final multiplication result will be of (N + N) bits as S = S(N + N)....S3 S2 S1.

Step 1: Divide the multiplicand A and multiplier B into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.



general representation for vedic multiplication

PROPOSED VEDIC MULTIPLIER:

The concept of Urdhava tiryagbhayam sutra is the generation of all partial products can be obtained with the concurrent addition of partial products and their summation.Since the partial products and their sums are calculated in parallel,The multiplier is independent of the clock frequency of the processor.The net advantage is that its and Cout.LET us divide A and B into two parts say the 64 bit multiplicand A can be divided into two parts MSB2 and LSB2.Similarly,B is divided into 2 parts namely MSB1 and LSB1.Using the fundamental of vedic multiplication ,taking 32 bits at a time and using 32 bit vedic multiplier .The output of 32X32 bit multiplierare added accordingly to obtain the the original product,Here total three 64 bit ripple carry adders are required.

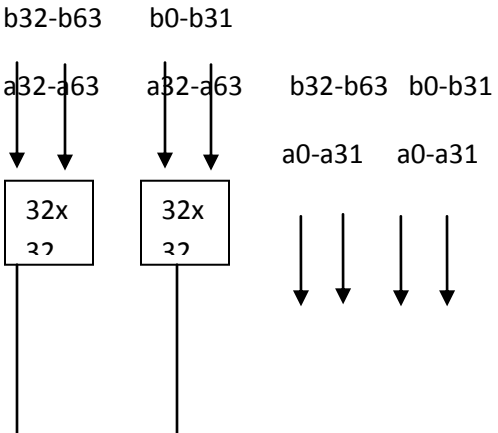
Step 2: Represent the parts of A as AM and AL, and parts of B as BM and BL. Now represent A and B as AM AL and BM BL respectively.

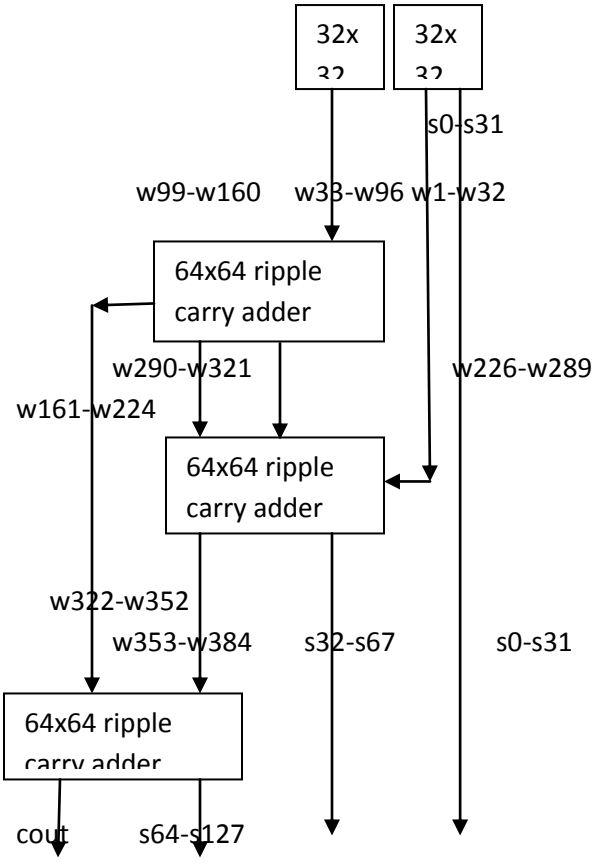
Step 3: For A X B, we have general format as shown in fig.

reduces the need of processors to operate at increasingly high clock frequencies ,This also reduces the power dissipation in Urdhva tiryagbhyam.

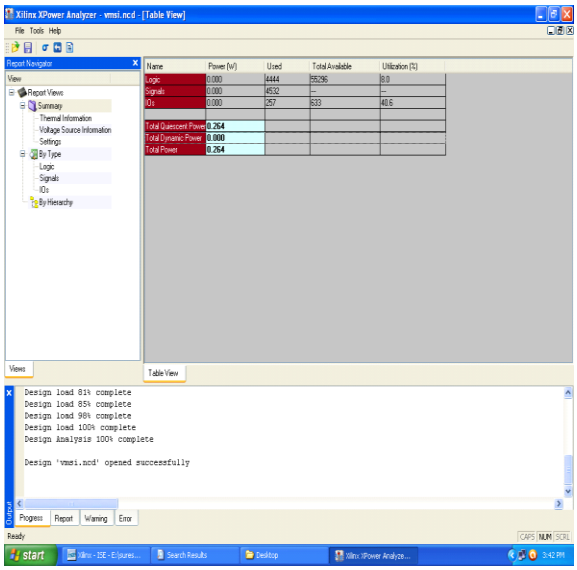
Vedic multiplier for 64X64 bit module is shown in the below diagram.It can be easily implemented by using the 32X32 bit vedic multiplier.Let us consider 64X64 multiplication say A=A63,A62,A61,……A0,and B=B63,B62,B61,…..B0.The output will be S=S63,S62,…….S0

64X64 bit vedic multiplier using Urdhava tirbhagyam technique




32x 32
32x 32
s0-s31
w99-w160
w33-w96
w1-w32
64x64 ripple carry adder
w290-w321
w226-w289
w161-w224
64x64 ripple carry adder
w322-w352
w353-w384
s32-s67
s0-s31
64x64 ripple carry adder
cout
s64-s127

SYNTHESIS REPORT:



Device utilization summary:

Selected Device : 3s4000lfg900-4

Number of Slices: 2548 out of 27648 9%

Number of 4 input LUTs: 4444 out of 55296 8%

Number of IOs: 257

Number of bonded IOBs: 257 out of 633 40%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 84.924ns

Timing Detail:

All values displayed in nanoseconds (ns)

Timing constraint: Default path analysis

Total number of paths / destination ports: 22204330556 / 101

Delay: 84.924ns (Levels of Logic = 48)

Source: a24 (PAD)

Destination: s105 (PAD)

CONCLUSION:

The proposed vedic multiplier proves to be highly efficient in terms of speed.The time taken for the multiplication operation is heavily reduced by adopting the vedic algorithms.The algorithms based on conventional mathematics can be simplified and even optimized by the use of vedic sutras.It is concluded that the

computer architectures designed based on Vedic mathematics are proved to be better than the conventional architecture in terms of computation speed, power utilisation and silicon area. It is proved to have less power,lower area and faster speed when these techniques are adopted.

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