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Image filtering vlsi processor for high speed and low power image processing system using logic in memory Architecture

[a] S.RAGHUPATHI., [b] J.MAGDALENEMILAN.,

a-Assistant Professor & Head, Shivani Institute of Technology, Trichy -9

b- II year - M.E. (VLSI), Shivani Institute of Technology, Trichy -9

ABSTRACT: In the era of information and multimedia, the real time IP (image processing) becomes most important in massive applications such as robotics control, surveillance and image recoginition. In such case at present, VLSI expertise focus on high speed processing of image rather considering power consumption and memory module.Even though the performance of the microprocessor and one dimentional(1-D) VLSI processors array are much efficient in speed but it is unable to enhance the low power processing and memory bandwidth. Ultimately, a new VLSI Paradigm is in demand to realise an efficient execution of image processing is image filtering processor.Hence This work evaluates that the proposed approach which outmatches the existing IP algorithms and processors.From the comparison and simulation result it is proved that the proposed architecture overcomes the demerits produced by the existing algorithms and processors.

Keywords*: processor, image filtering, LIM, memorybandwidth.*

I. Introduction:

Nowadays, engineers have used computers to manipulate and transform digital Representations of images. This discipline, called IP, employs five fundamental classes of operation such as Image enhancement, restoration, analysis, compression, and synthesis. IP then consists of "applying digital techniques to digital images to form digital results, such as a new image or a list of extracted data". Representing an image requires a large amount of data. As IP algorithms get more sophisticated and more complex, the performance needs of IP exceed the capability of general-purpose computers. Though IP algorithms and distinct processor arrays are constructed for the improvement of power, memory bandwidth and latency due to processor complexity, those schemes are unable to root in a proper way. The proposed approach is focused on the problem of improving memory bandwidth and power consumption.

II.1. SimPil Processor:

Researchers constructed Various IP algorithms for one dimensional (1-D) and two dimensional (2-D) data, and all the algorithms pointed out the speed rather considering memory bandwidth and power processing. The novel approach is tried to give the solution to the problem of memory upgradation and power efficiency.

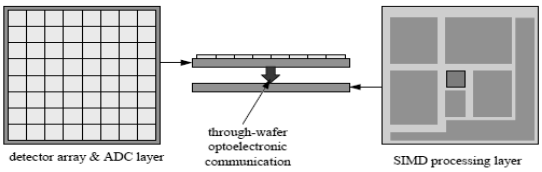

Figure 1. stacked Focal Plane Processor.

The SIMPil system presented in this paper which combines the features from both focal plane systems and image processing architectures processing plane, shown in Figure 1. By reducing the image transfer bottleneck found in decoupled detector processor systems, high frame rates are possible without constraining processing power. Processing area does not impact detector array fill factor.

II.2. Pipelining and parallelism in SIMPil processor:

Parallel architectures are well suited for image processing applications because of their ability to exploit inherent data parallelism in images. Parallel architectures can be structured in two ways. They can operate on an entire image or subimage in parallel or it operates on the image data in a pipelined model. The SIMD Pixel Processor (SIMPil) architecture maps a subarray of pixels to each processor.

II.3. Processor Architecture:

The structure of single SIMPil node is displayed in Figure 2. It illustrates how a single node interfaces to a sub array of detectors through sample and hold circuitry (S&H) and analog-to digital converters (ADC), and how each node is

connected to each other in a mesh network to operate in SIMPil mode. Each node includes a traditional RISC load/store datapath plus an interface to the detector array via an OE data channel. , a 16-bit multiply-accumulator (MACC), and 64-word local memory. It has a memory size (128 to 256 words). Keeping the silicon area devoted to memory in balance with area devoted to processing is a design goal of this architecture in order to maximize the efficiency of the system implementation.

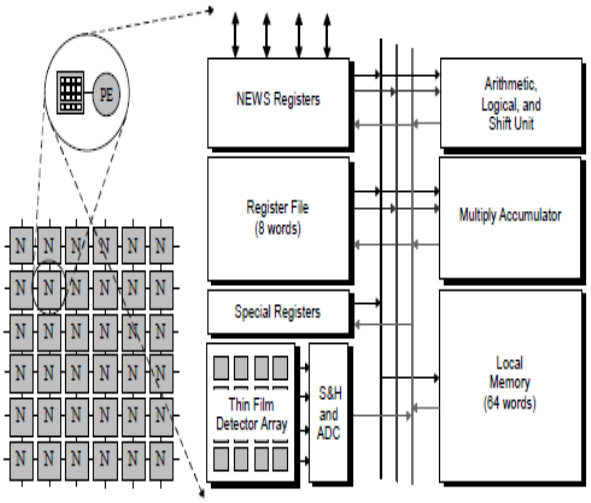

Figure 2. SIMPil Microarchitecture

II.4. Processor Communication:
SIMPil nodes communicate through a nearest neighbour NEWS (north, east, west, and south) network using NEWS registers in the datapath. The NEWS registers are addressable as general purpose registers making the register file a total of 12 words. To communicate to a node's neighbour, an appropriate NEWS register is specified as a destination in any instruction. Reading a NEWS register accesses the locally stored value for that communicated operand.

II.5. System configuration:
The SIMPil system is an embedded, programmable, focal-plane image processing system. Simulations of image processing application ssuggest a good balance of 36 to 64 pixels per SIMPil node (with 50 MHz node frequencies). Our prototype target is 64 pixels per SIMPil node. Using current VLSI technology, between 16 and 64 SIMPil nodes can be fabricated on a single Si VLSI chip. By tiling an array of 16 chips each containing 16 nodes, a 128×128 pixel resolution is achieved. The aggregate total for this system is 16,384 pixels and 256 SIMPil nodes. Operating at 50 MHz, SIMPil can perform 781 Kops/sec for each pixel. Eight bits is the minimum datapath width for pixels supporting 256 gray scale levels. This system can be scaled in two ways to meet different needs. More chips can be tiled to achieve higher resolution for operation on an entire image at the same processing rate. For example, with 64 SIMPil nodes on a single VLSI chip, an 8×8 array of chips fits on a 4" square MCM, yielding a 4096 SIMPil nodes system with a resolution of 512×512 pixels. Scanned arrays can delivery higher resolutions at slower frame rates.

III.1. Memory System Performance and Bandwidth:
Caches are small and fast memory elements which are used between the processor and DRAM. This memory acts as a low-latency high-bandwidth storage. If a piece of data is repeatedly used, the effective latency of this memory system can be reduced by the cache. The fraction of data references satisfied by the cache is called the cache *hit ratio* of the computation on the system. Cache hit ratio achieved by a code on a memory system often determines its performance. Repeated references to the same data item correspond to temporal locality. Data reuse is critical for cache performance. Memory bandwidth is determined by the bandwidth of the memory bus as well as the memory units. Memory bandwidth can be improved by increasing the size of memory blocks.
Consider the following code fragment:

```
for (i = 0; i < 1000; i++)
 column_sum[i] = 0.0;
 for (j = 0; j > 1000; j++)
column_sum[i] += b[j];
```

The code fragment sums columns of the matrix b into a vector column_sum.

III.2. Digital Test Results:

The prototype was digitally tested using a Tektronix LV500 chip tester.. The LV500 provides stimulus to 27 digital control signals for the SIMPil node, emulating the instruction unit by executing SIMPil programs. It is also used to read and write to the 8 bit data bus. Functional tests were performed on each functional unit using test programs simulated on the simulator. The register file can be loaded with values from the off-chip bus. The ALU, barrel shifter, and multiply-accumulate unit were stimulated with operands from the register file, and its results were written back to the register file. The results are then read from the register file to the off-chip bus for evaluation. The memory was tested using a similar technique. The fragment is part of a convolution program.

```
loadi r0, 12
load r1, r0
loadi r0, 24
load r2, r0
macc r3, re, r7
c11 = (36) = r3
loadi r0, 36
add r3, r3
store r0, r3
```

III.3. Area Efficiency Comparison:

These results assume an effective throughput of 0.67 instructions per cycle for SIMPil. These numbers express the efficiency of the SIMPil architecture for the targeted set of applications.

Processor	Technol-ogy (μm)	Vdd (V)	Area (mm^2)	Clock Freq. (MHz)	Mop/s mm^2
Alpha 21164a[1]	0.35	3.3	209	417	**2.4**
Pentium P54[1]	0.35	3.3	90	150	**2.0**
PowerPC 603ev[1]	0.35	2.5	81	166	**2.0**
SIMPil	0.8	5.0	2	50	**16.8**
SIMPil (scaled)	0.35	3.3	.38	176	**310.0**

Table 1. Area Efficiency Comparison

III.4. Receiver Amplifier Interface Circuitry:

The receiver amplifier provides low noise amplification of the optical detector output current. For through wafer comparator can generate a digital output from the signal. For CMOS this means we would like about 10 – 100 mV of output signal meaning the receiver should have a gain of 1 – 20 MΩ. In addition the receiver must have a differential front end to prevent pickup of digital noise from the processor located on the same chip. Simulations indicate that gains of 1 – 20 MΩ at 10 – 100 Mbps are possible with 0.6 μm CMOS.

IV. Experimental Results

At present the receiver is not designed to meet for all the design goals which may run at 100 Mbps. A receiver that runs at 155 Mbps and has a gain of 1 KΩ is designed Figure 3. Shows the fabricated and tested design before integration with the SIMPil node.

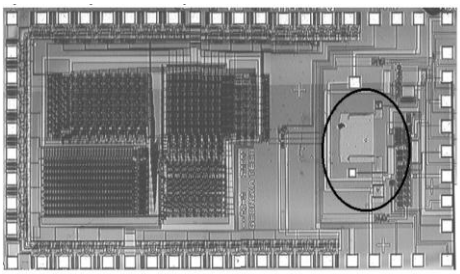

Figure 3: Micrograph of a Receiver Amplifier, Integrated MSM Detector and SIMPil Node,

The receiver die photo and measured performance are presented in Figure 4 and Figure 5.

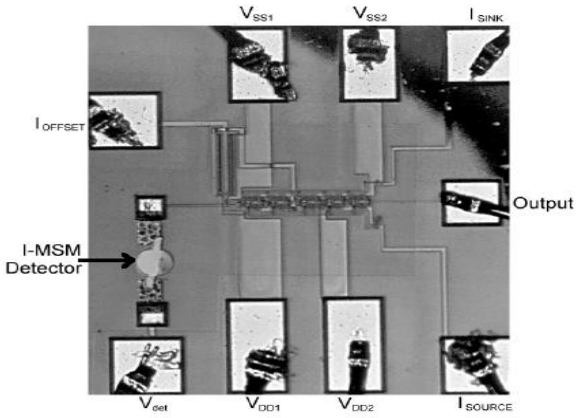

Figure 4: Digital CMOS Receiver 0.8 μm:

It is the move to design a higher gain receiver which also works on making the input signal specification less severe. This photoreceiver has been fully characterized with an integrated 50 μm square thin film InP- based I-MSM, and exhibited excellent characteristics, matching the SONET OC-3 SR specifications. In order to test the receiver, a commercial 1 mW CW 1300 nm laser diode was directly modulated by a current source and the pseudorandom data was fed through a bias tee to test the integrated circuit A digital 0.8 μm CMOS transimpedance amplifier was designed to meet SONET OC-3 SR specifications, with a target bandwidth of 155 Mb/s.

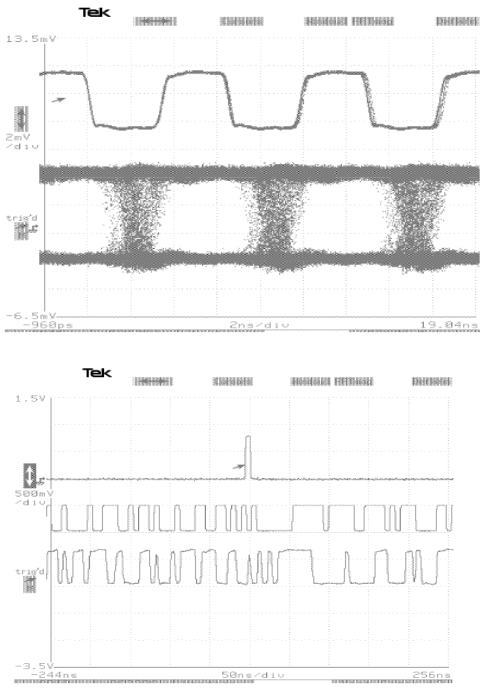

Figure 5a & b. Performance of Receiver at 155 Mbps

Figure 5 (a) represents a 155 Mb/s wide open eye diagram measured at –19 dBm. Figure 5(b) refers the

derived operation at 200 Mb/s with 27−1 NRZ optical pseudorandom data at −18 dBm.

V. Conclusion:

The integration of a thin film detector to a programmable SIMPil processor is proposed. The presented structure eradicate the existing problem of power efficiency and memory uprooting. Area efficiency comparison and the experimental results are shown to prove the throughput which results in operating at high speed. Hence it is observed that the programmable SIMPil processor provides the better power consumption and memory bandwidth.

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