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Hybrid Low Power Design for Adders Using SP-D3L

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Abstract— ***These include new full adder circuits usingcombination of the recently proposed split-path data driven dynamic logic and data driven dynamic logic. Based on the logic function realized, the adders were characterized for performance and power consumption. The adders were then further deployed to evaluate the impact of sum and carry propagation delays on the performance, power of these systems. In this way, the number of series-connected pre charging transistors and the gate input capacitance are minimized with remarkable benefits in terms of dynamic energy dissipation and computation speed. Thus the PDP is evaluated.***

IndexTerms—**D3L-Data Driven Dynamic logic, SP-D3L-Split Path Data Driven Dynamic Logic, PDN-Pull Down Network**

I. INTRODUCTION

Very-large-scale integrated circuits is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. These include three new fulladder circuits using the recently proposed split-path data driven dynamic logic. Based on the logic function realized, the adders were characterized for performance and power consumption. The adders and multiplier to evaluate the impact of sum and carry propagation delays on the performance, power of these systems. Split-path data driven dynamic logic is a new technique is here proposed that emphasizes the advantages of the conventional D3L. Split Path Data Driven Dynamic Logic (SP-D3L) achieves a considerably energy saving, over conventional Domino Logic, by removing the clock signal: the control of the precharge and evaluation phases is managed only by input data. Unfortunately, this advantage is typically obtained at the expense of speed performances. These include three new fulladder circuits using the recently proposed split-path data driven dynamic logic.

Based on the logic function realized, the adders were characterized for performance and power consumption Each of the adders was also classified according to the logic function realized. Using this approach we have presented an analysis of the possible impact of logic function choice and not just circuit choice on the performance of the final adder. Three different adder functions were also realized using the recently proposed data driven dynamic logic (D3L) and split-precharge data driven dynamic logic (SP-D3L) The

performance of a full adder circuit depends to a great extent on the type of design style used for implementation as well as the logic function realized using the particular design style

II. LOW-POWER DATA-DRIVEN DYNAMIC LOGIC (D3L)

A new family of low-power dynamic logic called Data-Driven Dynamic Logic (D3L) is introduced. In this logic family, the synchronization clock has been eliminated, and correct sequencing is maintained by appropriate use of data instances. Then, it is shown that replacement of the clock with input data implies less power dissipation without speed degradation compared to conventional dynamic logic.

In conventional CMOS circuits, for each n-type device there is a corresponding p-type device. In fact, the required logic function is implemented twice, both in a PDN (Pull-Down Network) and a PUN (Pull-Up Network). For increasing speed, in dynamic logic, the PUN is often replaced with a single transistor that is controlled by a global clock signal . Correspondingly, circuit operation is divided into distinctive precharge and evaluate phases. In the precharge phase, the output node is precharged to a particular level (usually high for a PUN) while the current path to the other level (GND for a PDN) is turned off. Upon completion of the precharge phase (CLK='1'), the path to the high level is turned off by the clock and the path to ground is turned on. Therefore, depending on the state of the inputs, the output node will either float at the high level or will be pulled down.

A clear advantage of a dynamic CMOS gate is its reduced silicon area. Typically, there are 2n transistors in a conventional n-input CMOS gate, while the dynamic configuration needs only n+2 transistors. Also, due to the smaller area and consequently smaller parasitic capacitance, power dissipation and speed are, in principle, improved by the dynamic approach. Compared to static CMOS logic, the input capacitance of every dynamic gate can be reduced, but due to the presence of an additional transistor (the clocking transistor) that must be cascaded with the main block, the speed generally does not double. Moreover, the excessive loading of the clock signal that must be connected to every dynamic gate and the corresponding routing problems reduce the benefits of dynamic logic. Correspondingly, as well, the increasing frequency of todays circuits results in greater power consumption when implemented in dynamic fashion.

III. Low Power Split-Path Data Driven Dynamic Logic (SP-D3L)

Data Driven Dynamic Logic (D3L) achieves a considerably energy saving, over conventional Domino Logic, by removing the clock signal the control of the precharge and evaluation phases is managed only by input data. Unfortunately, this advantage is typically obtained at the expense of speed performances and consequently affecting the Energy-Delay Product (EDP). This paper presents a novel technique to design D3L parallel prefix adders considerably reducing speed penalties. Moreover, a new design style, named Splith-Path D3L, is introduced to overcome the limits of standard D3L.

When applied to a 4-bit adder realized the proposed technique leads to an EDP 25% and 20% lower than the standard Domino Logic and the conventional D3L counterparts, respectively The objective of this project is to control the speed of the Permanent magnet DC motor through microcontroller with help fuzzy logic. Today's every industry become automated industry. To make the industry automation the equipment and machineries should be controlled automatically. In this project we control the PMDC motor automatically through microcontroller with help of fuzzy logic. So we can control the machineries which involving this motor accurately. By making the industrial automation we can increase the production rate.

Split-path gate level implementation of the dot operators, however, D3L does not eliminate the need for two series-connected PMOS devices in the PUN which is the main reason of a slow precharge propagation path. To this aim, an optimized gate level implementation of the dot operators is here presented. The proposed design style, named split-path D3L, consists in splitting the PDN of the D3L gate into sub-networks. In this way, the number of series-connected precharging transistors and the gate input capacitance are minimized with remarkable benefits in terms of dynamic energy dissipation and computation speed. As a further advantage, the split of the PDN also causes the split of the parasitic capacitance of the dynamic node, thus increasing the gate speed. The new split-path D3L grouped-generate gate of a even dot operator.

In order to correctly evaluate the logic function, a static 2-input NAND gate replaces the final static inverter used in Domino and D3L gates. Also the keeper transistor is split in to two keeper PMOS devices, each of them related to one evaluating sub-network.Since there is only one leakage path for each PDN, the width of each keeper can be scaled down by a factor of two. The DC contention between the keeper and the related PDN during the gate switching is mitigated and the energy dissipation and delay are further reduced. The only drawback of the proposed split-path D3L gate is the two series-connected NMOS devices of the final static NAND. The width of these transistors is doubled with respect to the single NMOS device of the final static inverter in Domino and D3L implementation, leading to an increase of the parasitic capacitance of the two dynamic nodes D1 and D2.
However, this negative effect is well counterbalanced by the reduced parasitic capacitances of the smaller keepers and of the smaller PMOSs in the PUNs. For what it concerns about the grouped-propagate gate of the dot operator, the new design style is inapplicable since there is only one path in the PDN. It is worth noting that the proposed split-path D3L design style is completely compatible with the new optimized carry-propagation tree structure described they both concur to decrease the width of the pre-charging PMOS transistors. Unfortunately, the split-path design style cannot be applied also to the grouped generate gate of odd dot operators. Above figure depicts the split-path D3L version of an odd dot operator. It can be easily verified that the following case may occur.

For such a reason, the odd dot operators of the proposed adder were implemented in standard D3L. Finally, the proposed split-path D3L style can be applied to the design of the XOR gates of the pre-processing stage. The new gate computing the propagate signals depicted.

As a further advantage, the split of the PDN also causes the split of the parasitic capacitance of the dynamic node, thus increasing the gate speed. . The width of these transistors is doubled with respect to the single NMOS device of the final static inverter in Domino and D3L implementation, leading to an increase of the parasitic capacitance of the two dynamic nodes D1 and D2. However, this negative effect is well counterbalanced by the reduced parasitic capacitances of the smaller keepers and of the smaller PMOSs in the PUNs. For what it concerns about the grouped-propagate gate of the dot operator, the new design style is inapplicable since there is only one path in the PDN. It is worth noting that the proposed split-path D3L design style is completely compatible with the new optimized carry-propagation tree structure described they both concur to decrease the width of the pre-charging PMOS transistors.

These include three new full adder circuits using the recently proposed split-path data driven dynamic logic. Based on the logic function realized, the adders were characterized for performance and power consumption. The adders and multiplier to evaluate the impact of sum and carry propagation delays on the performance, power of these systems. Split-path data driven dynamic logic is a new technique is here proposed that emphasizes the advantages of the conventional D3L over Domino Logic, avoiding the energy-related drawbacks coming from the high input capacitance driven by the pre-charge inputs. The proposed design style, named split-path D3L, consists in splitting the PDN of the D3L gate into sub-networks. In this way, the number of series-connected pre-charging transistors and the gate input capacitance are minimized with remarkable benefits in terms of dynamic energy dissipation and computation speed. As a further advantage, the split of the PDN also causes the split of the parasitic capacitance of the dynamic node, thus increasing the gate speed.

The full adder functions characterized using the SP-D3L methodology provide the lowest delay with the SP-D3L

propagation adder working almost twice as fast as the standard adders selected in the study. The drawback of these adders is of course the high power consumption, due to the large number of transistors as well as the multiple paths to ground present in the sp-D3L implementations. With respect to the choice of logic function to implement, the full adder was observed to perform the best when implemented using the propagate and generate signals. This can be attributed to the fact that this function allows for smaller number of transistors stacked in series and shows the lowest capacitance at the output node. This shows that the capacitance at the output node forms the most critical component of the adder speed irrespective of the number of stages of circuits before getting the sum and carry outputs. Power consumption in CMOS circuits has always been one of the primary concerns of the designer especially when designing for applications with strict power constraints. To facilitate the ideal choice of adder topology for scaled voltage or power-constrained applications, it is necessary to analyze adder performance.

On a functional level, it can be observed that once again the adders based on the propagate, generate signals fare the best. Especially in the D3L and SP-D3L implementations of this function, this performance advantage can be attributed to the periodic refreshing of voltage levels between the intermediate adder stages. These adders however continue to suffer from high power dissipation, most possibly due to the large number of switching nodes, and increased short-circuit power dissipation with increased loading. The new split-path implementation of the full adder function was found to be a strong contender in terms of both performance-power efficiency as well as strong drivability. Functionally, the full adders realized using the propagate and generate functions were found the most optimum solutions from a performance and process-variability point of view due to the reduced capacitance at critical nodes. Data Driven Dynamic Logic (D3L) achieves a considerably energy saving, over conventional Domino Logic, by removing the clock signal the control of the pre charge and evaluation phases is managed only by input data. Unfortunately, this advantage is typically obtained at the expense of speed performances and consequently affecting the PDP. This paper presents a novel technique to design D3L parallel prefix adders considerably reducing speed penalties. All the simulations were setup so as to drive the adder inputs through buffers and have the adder outputs drive buffers.

This setup is based on the one used by us in and helps simulate realistic loading at the input and output of the adders. The table reports the average power consumption when executing the set of all possible input combinations to the adders. The delays reported correspond to the worst case delays observed in every adder. It can be seen that the hybrid adder provides the best PDP amongst all the adders when simulated standalone.

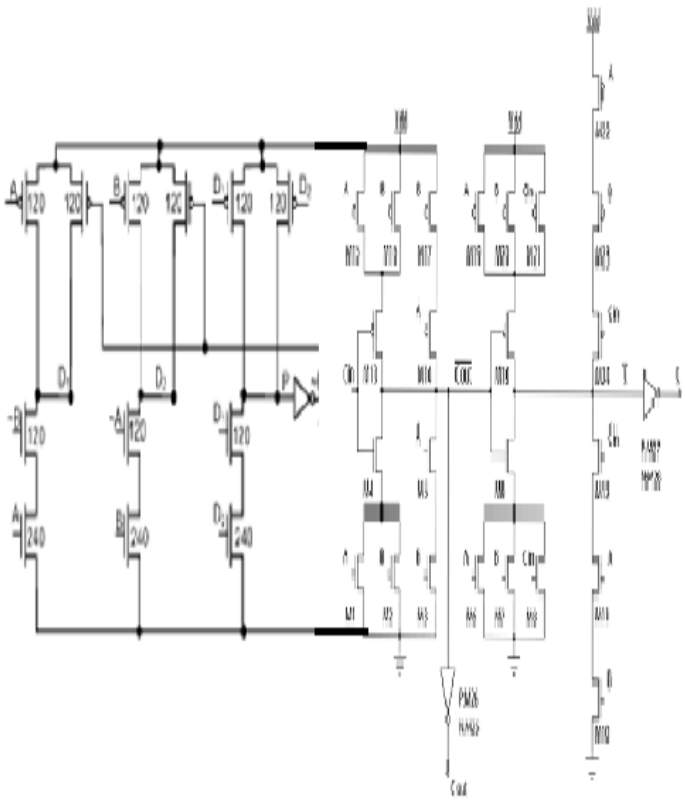

Fig 1: Hybrid Full adder circuits

The full adder in figure 1 functions characterized using the sp-D3L methodology provide the lowest delay with the adder working almost twice as fast as the standard adders selected in the study. The drawback of these adders is of course the high power consumption, due to the large number of transistors as well as the multiple paths to ground present in the sp-D3L implementations. With respect to the choice of logic function to implement, the full adder was observed to perform the best when implemented using the data driven dynamic logic as a combination with split path data driven dynamic logic. This can be attributed to the fact that this function allows for smaller number of transistors stacked in series and shows the lowest capacitance at the output node. This shows that the most critical component of the adder speed irrespective of the number of stages of circuits before getting the sum and carry outputs. Moreover, a new design style, named hybrid full adder using combination of split path data driven dynamic logic and data driven dynamic logic, is introduced to overcome the limits of standard full adder which uses only split path data driven dynamic logic.

IV. SIMULATION RESULTS

The proposed full adders are implemented using split path data driven dynamic logic and simulated the output for various full adders using combined split path data driven dynamic logic and data driven dynamic logic. Cadence's product offerings are targeted at various types of design and

verification tasks. The output is simulated using cadence and the output obtained is given below.

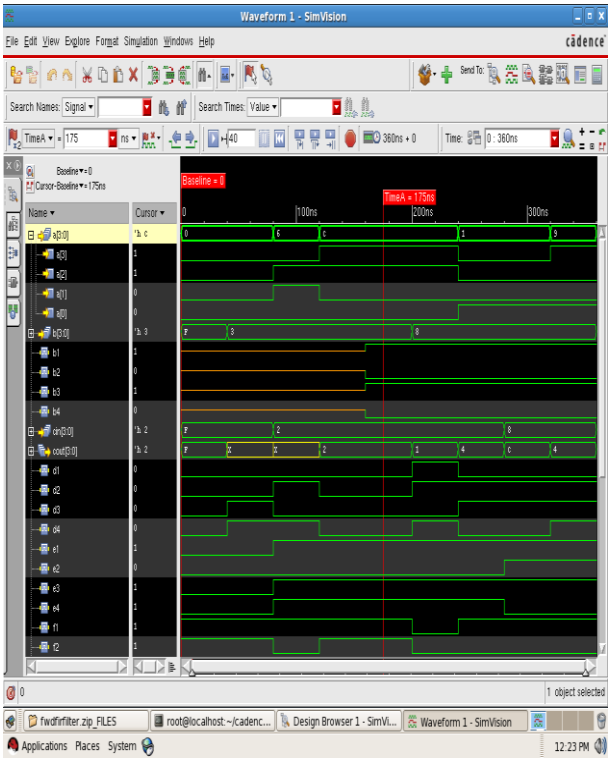

Fig 2: The output of hybrid full adder

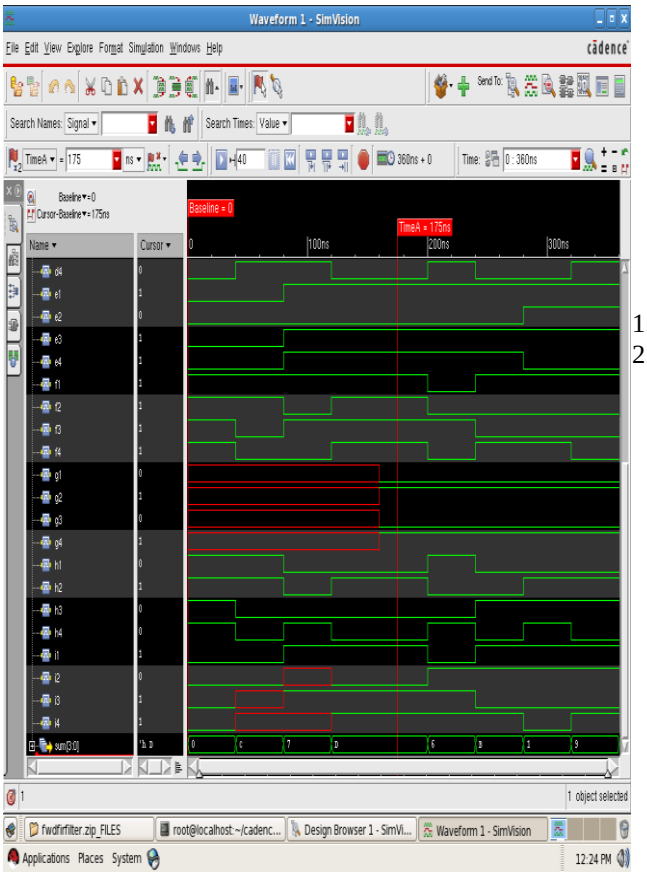

Fig 3: The output of hybrid full adder

1.
2.

VI RESULTS AND DISCUSSION

	DELAY (ps)	POWER (µw)	PDP
SUM	35	37	1295
CARRY	35	34	1190
PROPAGATION	40	35	1400

Table I. Power and Delay obtained for hybrid full adder using SP-D3L

V. CONCLUSION

The new split-path implementation of the full adder function was found to be a strong contender in terms of both performance-power efficiency as well as strong drivability. Functionally, the full adders realized using the propagate functions were found the most optimum solutions from a performance and process-variability point of view due to high drivability and robustness to process and voltage variations due to the use of small, identically loaded gates. In future the full adder circuit can be designed with fir filter to make the device with more drivability and high speed may be the result. Overall, this proposed low cost conversion topology is cost effective for high speed full adders. The PDP is also reduced than before.

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